High Definition Nozzle Architecture Inkjet Printhead for Commercial/Industrial Markets

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Abstract

Over 100 million silicon die have been built into HP Thermal Inkjet printheads and shipped to customers in the HP Scalable Printing Technology (HP SPT) platform since 2005. All these HP SPT printheads have a common attribute: the nozzle density and underlying power transistors are at 1200 nozzles per slot inch (NPSI). By re-engineering firing FET topology, simplifying nozzle logic and other circuit improvements, a new silicon platform has been developed that doubles the density of the underlying power transistors, resulting in 2400 NPSI on HP SPT in the new High Definition Nozzle Architecture (HDNA) platform. To address the increased demand for print data, the data rate between the print system and printhead silicon has been improved by a factor of three. The new printhead, the HP A53 Printhead, is form-factor compatible with the existing HP A51 Printhead and existing HP Inkjet Web Presses can be field-upgraded to use it. Its versatile nozzle configuration allows it to be reconfigured to exactly suit each application.

Introduction

HP's 4.25-inch and 0.88-inch printhead platforms have been instrumental in making HP a premier supplier of Commercial/Industrial presses and printers in the General Commercial, Large Format Graphics, Large Format Design and Large Format Signage printing markets. The 4.25-inch printhead (for example: the HP A51) uses five HP SPT die designed to support both pagewide and scanning printing while the 0.88-inch printhead (i.e. the HP88) has a single HP SPT die and used for scanning multi-pass printing. "FLN" is the HP SPT silicon die at the heart of both these printheads as shown in ***Figure 1***.

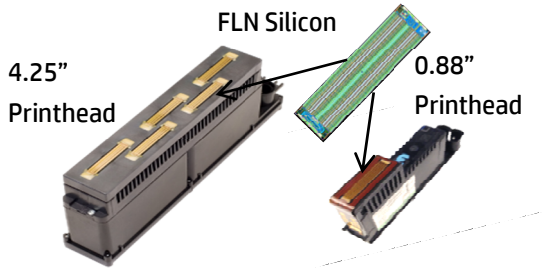

Figure 1 *– FLN Silicon as used in two HP printheads*

FLN is comprised of circuit elements that interface to the printer electronics, circuits that control firing resistors, and micro-fluidic channels that eject the ink onto the paper. More than 20 unique fluidic design variants of FLN are being produced by HP, each of which have been tuned to differing ink requirements, application needs, and reliability goals of a given market segment. Originally introduced in 2006 and deployed broadly since then, the platform has been updated several times but now faces competitive challenges. In order to leverage the wide variety of printing platforms HP has established around FLN die, an improved performance, form-factor compatible silicon solution was developed.

HP's SPT Technology and Drivers for Improvement

FLN silicon die are manufactured in HP's proprietary SPT process. Unlike many competitive ink jet technologies, no micro assembly of components (i.e. attaching a separate orifice plate or electronics) is required to integrate the drive electronics and fluidic elements of the drop ejector. This brings the precision and batch processing cost advantages of integrated circuit manufacturing to key elements of printhead manufacturing. HP SPT consists of three major modules: the circuit portion that receives and routes input signals, the resistor module that generates the ink jet drive bubble, and the fluidics portion that routes ink into the firing chamber and provides the nozzle for drop ejection.

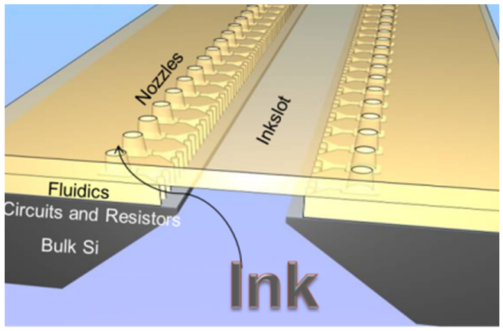

Figure 2 illustrates the process modules that comprise HP SPT silicon die.

Figure 2 *– HP SPT Elements*

SEM images of various aspects of the microfluidics portion are shown in ***Figure 3***.

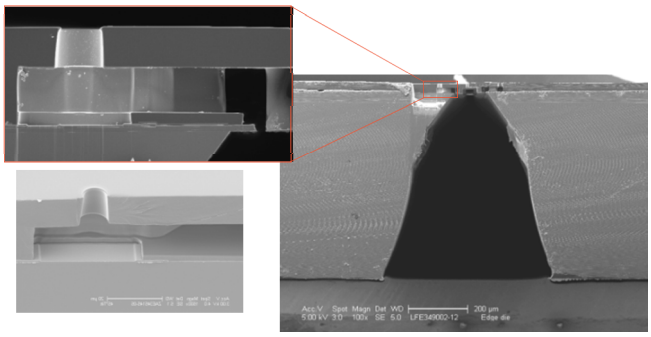

Figure 3*– HP SPT Resistors and micro fluidics*

The breadth of applications that FLN serves represents a special challenge when considering updates to the silicon die. At the high end, very high speed single pass web press printing with image quality (IQ) adequate for the General Commercial Print market—predominately text based, with a desire to include more graphics—needs to be supported. Key desired improvements are to extend printing speeds and improve IQ without a substantial re-design of system hardware, such as adding additional printbars to support light inks. Adding dual drop weights (low and high) and higher drop frequency for greater ink flux capability to the 4.25-inch printhead serves both these needs.

For Large Format applications, very high IQ graphic and technical printing using multi-pass print modes are also critical to support. While some platforms do not require dual drop weight capability, having a single printhead platform to serve HP's diverse inkjet product portfolio is desirable because technology and design elements developed for one product can be leveraged into others thereby speeding development time and reducing overhead to keep printhead costs low. To serve these diverse markets with common technology a printhead capable of multiple nozzle configurations is desirable and this flexibility enables future innovations. Higher ink fluxes enable productivity improvements by reducing print passes, but only if uniformity across the printhead is improved to keep images free from banding artifacts.

In summary, the key requirements for the new design were determined to be:

- Higher frequency and ink flux capability
- Dual drop weight capability
- Flexible nozzle architecture (i.e., drop weights and NPSI)
- Improved area-fill uniformity and image quality
- Same form factor (including backend assembly providing ink interconnect and pressure regulation, mechanical registration, and electrical interface)

Summary of the HDNA Design

The HDNA platform has delivered on these requirements by doubling the density of firing transistors in the silicon substrate, adding a redesigned data path to address nozzles at even higher speeds, making changes to support multiple nozzle densities, and adding thermal uniformity circuits for improved drop weight uniformity. Image quality is improved while retaining the same form factor and physical interfaces. These design elements were synthesized on the HDNA silicon in same die size and pad count as FLN silicon, but with twice the firing transistor density and 3x the electrical frequency supported.

A flexible nozzle arrangement is at the heart of the HDNA value proposition. Both the traditional 1200 NPSI and the new 2400 NPSI nozzle densities are supported in the platform with the same underlying silicon circuits. Other configurations are also possible and will be pursued on future products as HDNA printheads cover a wide range of application spaces in packaging, signage, design, and graphic printing markets.

Elements of the HDNA Silicon Platform

Engineering of the Data Pipeline for Efficiency and Flexibility

Integral to the HP SPT HDNA printing platform is an innovative data path engineered to maximize the efficiency of every element of the data pipe, from front-end image pipeline in the printer to the drop-ejector circuits on the printhead. Many elements of the nozzle data pipeline were re-designed to attain the 3X speed improvement over FLN in the same process technology. The CMOS technology utilized on HP SPT silicon die is engineered for efficient power delivery, low cost and robustness to corrosive inks, resulting in a circuit technology optimized for HP Thermal Inkjet nozzle operation with compromises in computational efficiency and bandwidth. State of the art CMOS technology on the other hand, as utilized on printer ASICs, use 22 nm feature size and up to 8 levels of interconnect and offer computational density orders of magnitude greater than HP SPT's older CMOS and interconnect technology.

In HDNA print platforms, computationally expensive tasks are completed in printer ASICs and/or FPGAs, in technologies optimized for such tasks. Some of these tasks, such as image densitometers used to identify areas of peak power consumption and thermal limits, have necessarily always resided in the front end ASICs/FPGAs, due to prohibitive memory requirements on HP SPT's CMOS technology. Other functions that have historically resided on the printhead now reside, entirely or in part, on printer ASICs and FPGAs where they can be accomplished in a much more cost-effective manner. Nozzle addressing and compensation for printhead location error is an example of such a function.

Figure 4 shows the FLN printhead arrangement with 44 primitives of 12 nozzles each on each side of the ink slot.

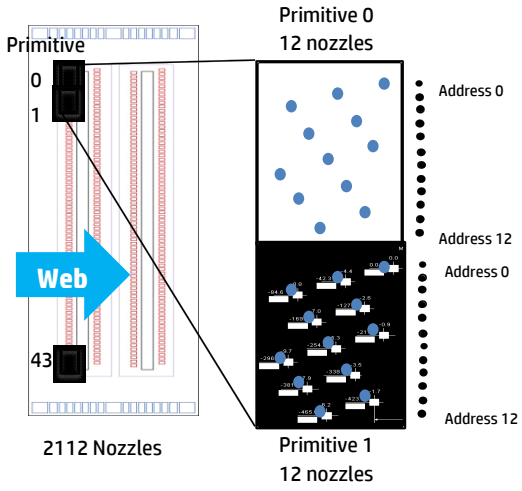

Figure 4 – FLN primitive arrangement

One address (nozzle) in each primitive can fire simultaneously. Previously, a print system sent an entire column's worth of print data to a printhead, and then—based on printhead placement calibration algorithms executed in the printer—that column data was shifted in time and space to match the

primitive/address structure on the printhead to compensate for placement error and to reduce peak power demands. Notice that within each primitive, nozzles are staggered along the scan/web direction to account for timing delays.

In the HDNA data path, instead of sending a full print column of nozzle data at a time, nozzle data is re-ordered in the printer and the data for one time slice (i.e. the data for one address in all primitives) is sent to the printhead as a Fire Pulse Group. Consequently, the requirements for nozzle data memory on the printhead are reduced by an order of magnitude and state machines for address manipulation on the printhead are eliminated entirely. The cost for the added computations to the printer FPGA is minimal where digital logic, relative to the CMOS technology on the printhead, is essentially free.

The 2X density increase in drop generator firing FETs is made possible by reducing the primitive and nozzle logic area through the efficient logical topology as described above and by novel *laterally-defused metal oxide semiconductor* (LDMOS) device development and layout resulting in higher densities. Silicon processing improvements have also lowered the area required for ink slotting—the physical channel through the die that feeds ink from the backside of the die to the drop generator arrays depicted in **Figures 2** and **3**. This enables a single front-end CMOS mask set, which can be coupled with a multitude of MEMS and fluidic architecture masks, to meet the needs of the broad product space addressed by the HDNA platform.

Increasing Data Rates in HP SPT CMOS

Compared to previous platforms, the HDNA platforms allows for twice the number of nozzles fired at 1.5X the frequency, or 3X the frequency for the same number of nozzles, while employing the same physical footprint and data lanes. This required a fully re-engineered front end Low Voltage Differential Signal (LVDS) receiver and deserializer on the printhead to receive inputs and parse header information from data. Achieving high data rates in the HP SPT process is challenging because it is optimized for high-voltage power delivery and cost with trade-offs affecting low-voltage device speed.

The new LVDS receiver is a moderately complex analog circuit block described by over a hundred unique design parameters. The performance requirements for the HP SPT data path and the sheer number of parameters made manual tuning methods impractical. Designers identified a subset of the parameters as critical to receiver operation and collated them into 22 independent groups. This broad and complex parameter space exhibits discontinuities and many local maxima, features that thwart traditional optimization algorithms. Consequently, HP's engineers developed a library of algorithms that mimic genetic evolution found in nature. These successfully optimized the design by determining how variation and selection were performed.

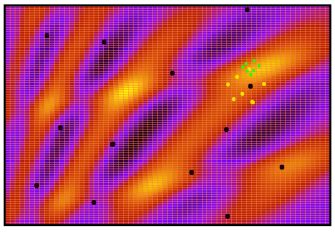

Figure 5 *– Multi-Maxima Surface*

The parameter space is envisioned to be a topological surface, as shown in ***Figure 5*** with local optimums (lightest colors) for critical parameters such as setup and hold time for data which vary as a function of circuit design choices. This figure is dramatically simplified from the actual 22 dimensional space being optimized.

Against a pre-defined performance metric, a group of randomly distributed initial candidates (black dots) are evaluated and higher performers (yellow dots) are re-populated into more narrowly-distributed colonies that serve as starting points for subsequent phases of optimization (green dots). The evaluator is comprised of a SPICE test bench harnessed in a library of Perl modules that evaluate every candidate's performance against the appropriate figures of merit, running thousands of simulations a day on a HP Z800 workstation. Comparison of front-end bus speed of the optimized result vs. technology nodes for the HDNA de-serializer and other commercially available data links (see **Figure 6**) demonstrates the extent to which this approach was able to push the HP SPT process technology beyond conventional approaches.

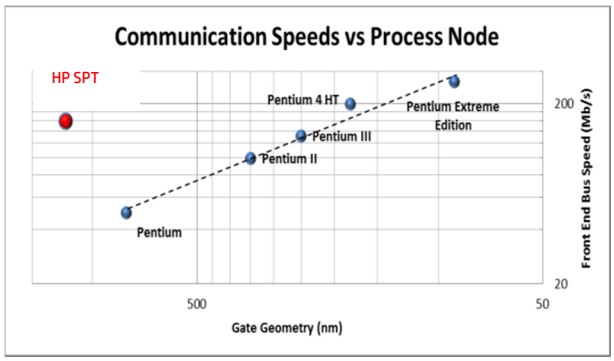

Figure 6 *– Comparison of LVDS receiver performance vs. process technology node*

Addressing Peak Power Demands and Energy Regulation

With 4224 nozzles per die and up to 45mA per nozzle, power management is a critical feature of the HDNA platform. Without a properly engineered power management solution, the cost of print system power supplies and energy variation due to system parasitics—such as power bus resistance—will place prohibitive restraints on operating specifications. The data path, nozzle circuits and print masks have all been engineered to minimize peak power demands of the printhead die with minimal compromises to maximum firing frequency or per-nozzle energy requirements. Furthermore, the power delivery system has been designed to be robust to parasitic losses so that per-nozzle energy delivery stays constant over all print modes.

With the increased data rates made available through the re-design of the front-end LVDS receiver and deserializer, the printhead can load data and fire nozzles electrically at 2-4X (depending on nozzle configuration) the maximum fluidic frequency. By managing the nozzle data path with this capability, high density print events can be spread over time to minimize peak power using multiple virtual print columns, to print a single actual print column. Furthermore, the firing events on the printhead initiated by each Fire Pulse Group are spread in time through an on-die fire delay distribution network.

Even with an electrical firing frequency 2-4X that of the fluidic nozzle frequency and on-die temporal distribution of fire events, per-nozzle energy regulation is required so that parasitic effects do not cause image quality degradation during peak print

densities. The LDMOS firing FET is configured in a source follower configuration (High Side Switch, or HSS), allowing the gate voltage of the firing FET to establish firing power independent of voltage variation of the main power supply (tied to the drain of the firing FET). A high-voltage logic supply, independent of the main power supply, is used for gate control of the HSS. While the main power supply voltage will vary across the die due to parasitics (such as power supply resistances) as a function of power demands and high print densities, the high-voltage logic supply is much more stable over all print modes. Consequently the energy delivered to each nozzle can maintain a constant level across a large range of print modes and data.

Controlling Thermal Gradients

The drop weight ejected by an inkjet nozzle is a strong function of ink temperature. If temperature varies across the ink slot of a printhead, the resulting variation in drop weight can lead to ink density differences—typically called "banding"—that degrade image quality. Variations in temperature along an ink slot can easily occur because nozzles in the center of the ink slot have neighboring nozzles that add heat to the substrate, whereas end nozzles have fewer (or no) neighbors on one side. This effect is further compounded by silicon area outside the nozzle region: it acts as a heat sink to the ink slot, further lowering the temperature at the end nozzles resulting in measurable temperature variation. These gradients may create an objectionable print artifact called *light area banding* that typically requires extra print passes to disguise, thereby lowering system throughput. End warming control circuitry was implemented on HDNA to address this issue. Temperature sensors and control circuitry are added that modulate heater circuits until a uniform temperature is achieved across the entire nozzle array.

Figure 7 shows thermal imaging of the HDNA die under typical operating conditions with and without correction for this effect.

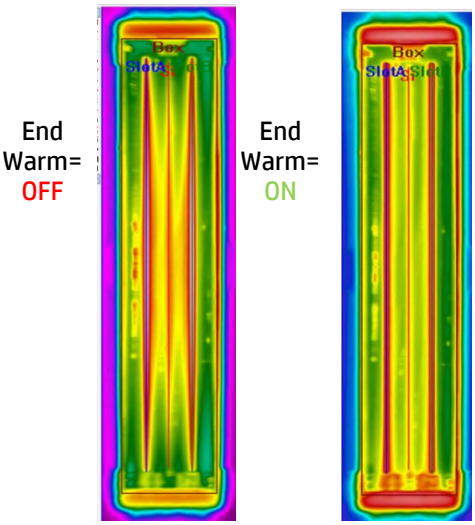

Figure 7 *– Thermal images showing heat gradients across the print swath with and without end warming on the HDNA die*

Note the color variation towards the center of the die in the left image. The higher temperatures there increase these nozzles ejected drop weights relative to end nozzles. The right image shows the same silicon die with identical firing conditions with end warming turned on. Note that the die temperature is much more uniform.

The corresponding printed image densities in a light area fill is shown in ***Figure 8*** for the two end warming conditions**,** where light regions in the vicinity of swath boundaries are clearly visible. The positions of the swath boundaries are made deliberately evident by the slight non-overlap of the pattern. A HDNA die image is added to illustrate the die orientation when printing: scanning left-to-right.

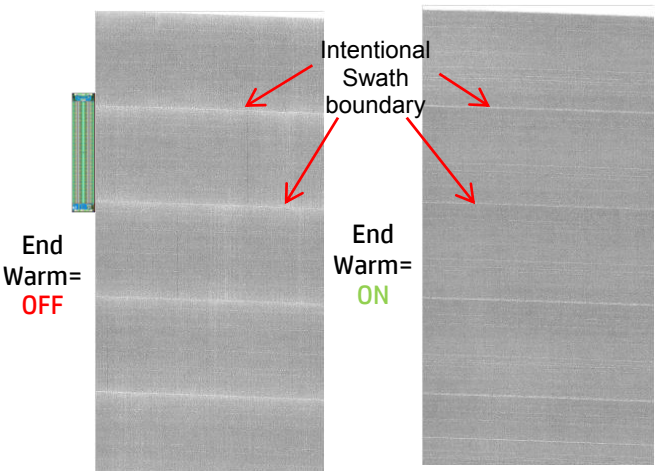

Figure 8 *– Single pass light area fill with Endwarming on and off*

The resulting improvement in print density uniformity delivers better image quality when a low number of print passes are used (for example in productivity modes in a scanning printhead system). While printing images, the nozzle temperature variation tends to vary in a chaotic manner. Because the circuit response time is much faster than the silicon thermal response time, good control of uniformity is observed under dynamic printing conditions.

Circuit Development Influence across Market Segments

The development of HDNA demonstrates synergy between HP's commercial and consumer/business print markets. Cost pressures on consumer printheads drove the development of a smaller resistor drive circuitry and reduced pad counts for electrical interconnect savings. Those developments ultimately enabled the upgrades implemented on the HDNA platform without an increase in die size or pad count. Additionally, the energy regulation solution employed on the HDNA platform was first introduced with the HP OfficeJet Pro X-series business printers. Thus, many of the innovations required for reduced interconnect benefitting the HDNA platform for graphics printing came from cost reduction efforts in the consumer and business space. In the future, features developed for Commercial/Industrial printing solutions will be optimized for more cost-sensitive markets completing the circle of leverage between HP's printing businesses.

Web Press Product Introduction

HP's Inkjet High-speed Production Solutions (IHPS) group has announced that HDNA technology with dual drop weights will provide both image quality and speed enhancements to their new generation of web presses to be introduced in 2016.[1] Existing presses can be field-upgraded to HDNA. Two print modes will be supported: *Performance mode* using high drop weight nozzles (HDW) that will fire the same size drops but at higher frequencies than the HP A51 Printheads, and *Quality mode* that utilizes both high and low drop weight nozzles (LDW) to deliver improved image grain and finer color addressability in-gamut resulting in dramatically improved image quality.

A comparison of the nozzle arrangement on the HP A51 Printhead with 1200 nozzles per slot inch and the new HP A53 (HDNA) Printhead with 2400 nozzles per slot inch are shown in ***Figure 9.*** Note the non-circular bores used for the HDW nozzles on both printheads, and that LDW nozzles are placed between HDW nozzles on the HP A53 Printhead.

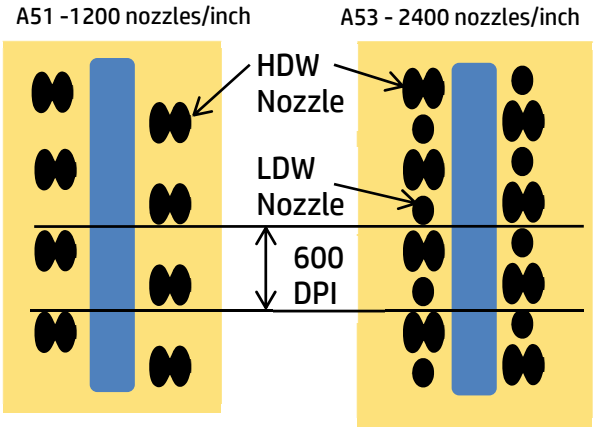

Figure 9 *– Comparison of Nozzle arrangements*

A SEM image of HDNA drop generator chambers and nozzle plate is shown in ***Figure 10***. The section is through the center of the non-circular bore of the HDW nozzle.

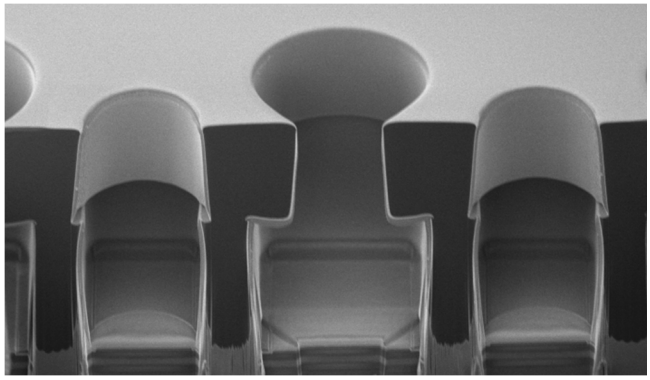

Figure 10 *– HDNA firing chambers and nozzles*

Significant MEMS processing advances have been required to enable both higher performance from HDW nozzles for faster speeds while doubling nozzle density for higher image quality.

Having 1200 nozzles per inch of both LDW and HDW nozzles permits using combinations of LDW and HDW drops from four nozzles during 600 DPI printing as illustrated in ***Figure 11.*** In this figure the box indicates a 600 DPI pixel and the LDW and HDW drops are indicated by small and large dots. Note that patterns with vertical symmetry (i.e., 1 LDW, 1 HDW, and 1 LDW + 1 HDW) produce equivalent gray levels.

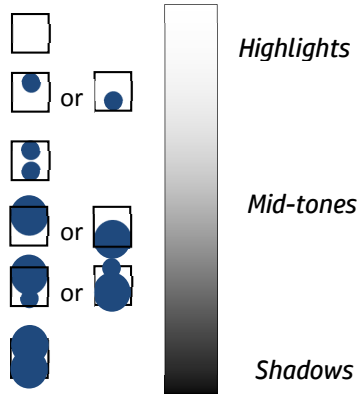

Figure 11 *– Combinations of drop weights across image densities*

Images printed with HDNA's dual drop weights have reduced grain compared to single (HDW) drops as shown in ***Figure 12.*** The same HP A50 Pigment Black Ink was used in both cases.

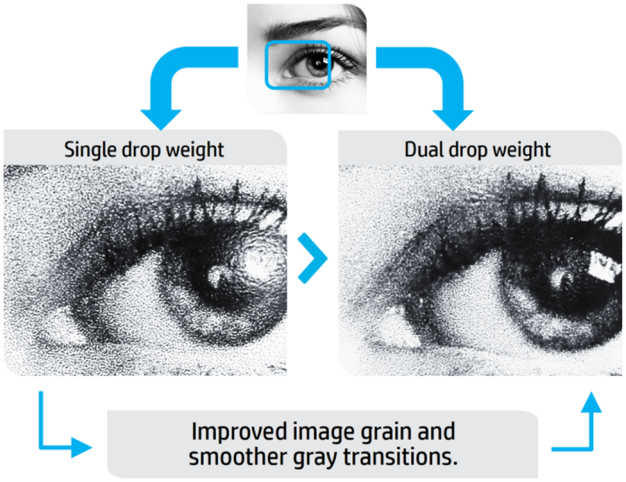

Figure 12 *– Web press image detail with HDW vs. HDW and LDW nozzle printing*

The combination of HDW and LDW also allows finer addressability within the existing color gamut— which is determined by the inks and paper— resulting in more precise color reproduction with better rendering of subtle shading in images. Tone breaks are suppressed, and smoother color and density transitions are possible with better highlight and shadow detail.

Summary

HDNA is a new technology developed by HP based on capabilities of HP Scalable Printing Technology (SPT). HDNA offers higher printing speeds, twice the nozzle density, and improved image quality with a unique dual drop weight configuration. HDNA delivers speed and quality improvements to IHPS inkjet web presses with a new set of printheads compatible in form-factor to the original (HP A51) printheads. This facilitates upgrading existing web presses to HDNA. HDNA is the latest example of IHPS's strategy to roll the latest printing technologies into its web press portfolio using upgradeable designs that preserve the investments of HP's customers. Advances such as HDNA are possible because HP's vertical integration of R&D and Manufacturing includes the entire printing ecosystem from servers, image processing, data path, printheads, ink, paper, to the paper path. This gives HP the ability to co-develop solutions (i.e. new data paths and inks that match its printheads' capabilities) that are optimized across these disciplines. In addition, HP's strong market presence in multiple application spaces gives HP the scale to rapidly and efficiently develop and optimize new solutions. In the future, office printing and Large Format solutions in packaging, design, graphics, and signage will benefit from the improved performance and feature set of the HDNA platform.

References

[1] "HP Pagewide Technology, Quality and Speed", http://www.hp.com/united-states/campaigns/pagewide/media/4AA5-7513ENW_hires.pdf

Author Biography

Jim Przybyla has 35 years of Silicon and MEMS experience in the design, device and processing realms. At Hewlett Packard he initially worked on 8 generations of internal NMOS and CMOS development as a design, process, device and integration engineer. He began supporting inkjet development in 1998 and led the HP SPT CMOS and piezo printhead development efforts. In his current role he develops printhead technology for next generation printheads. He holds 26 US patents.