Something for Nothing – Developing MEMS Silicon for a Vertically Integrated Market Leading Business – The example of HP Thermal Inkjet

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Abstract

There are two essential steps in growing and sustaining vertically-integrated market leading technologies in a field as diverse as digital printing, and these steps can be summarized as creation and refreshment of technology platforms. Growth is enabled by the creation of new platforms that bring new capabilities to open new application opportunities. Because maturing markets present price and performance challenges to each new generation, sustaining market presence over time can be achieved by refreshing existing platforms - offering "Something for Nothing" by extending the current platforms. 'Improved performance at the same cost', or 'the same performance at reduced cost' can be strong value propositions to extend existing platforms. Traditionally in integrated circuit businesses, this is done by reducing electronics cost or increasing performance according to Moore's Law. MEMS (Micro Electro-Mechanical System) processes take considerably longer to develop than conventional IC processes resulting in a more difficult challenge to keep up with the fast pace of product introductions. This is partially-compensated by the much longer lifetime a successful MEMS process can enjoy, so it becomes essential to create improved MEMS designs and process variants that add features and/or reduce cost.

HP's Scalable Printing Technology (SPT) is used in HP's vertically-integrated inkjet printer and web press product lines that span a price range from $99 to $4.5M and are produced by many HP divisions. Innovations within SPT that enable new silicon value propositions will be used to demonstrate the strategic benefits of giving internal product developers and HP customers 'Something for Nothing'. Examples include silicon circuit and process simplifications to enable cost reductions, fluidic process and design optimizations to enhance performance, and radical design and process technology improvements within the existing footprint of silicon printhead chips (called "die") to add completely new capabilities.

Introduction

The first HP Thermal Inkjet printhead—ThinkJet—was introduced in 1984. HP Thermal Inkjet has maintained high market share across HP's portfolio of printing solutions since that time defying the "innovator's dilemma": *"Should we invest to protect the least-profitable end of our business so that we can retain our least-loyal, most price-sensitive customers? Or, should we invest to strengthen our position in the most profitable tiers of our business with customers who reward us with premium prices for better products?"*[1] The latter course is commonly chosen by companies to maximize return on assets, which can yield disasterous long-term results when "good enough" solutions are developed by competitors who undercut the price structure of existing solutions. HP's Moore's Law for HP thermal Inkjet printing (see **Figure 1**) shows that HP has not been immune to this dilemma as larger and faster systems have been regularly developed at an impressive rate. This begs the question: *how has HP maintained its core markets even as it has pursued these higher productivity solutions?* The answer is multi-faceted, but one factor has been HP's willingness to reinvest in existing printhead assets to improve their competitiveness.

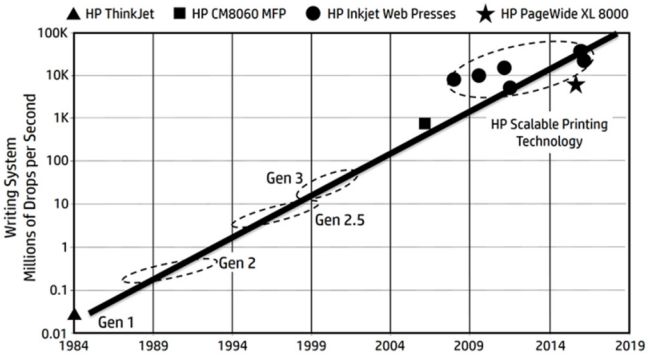

Figure 1 – HP's Moore's Law for HP Thermal Inkjet Printing

Printhead Platforms

Introduction

Developing and commercializing a new printhead platform requires an extensive technical and financial commitment from the business. Costs are significant for custom silicon circuits, MEMS design, processing, electrical testing, and debugging. The cost of custom assembly lines dedicated to a specific design can run into 10's of millions of dollars. A variety of related investments are required in electronics to test, drive, and measure the performance of the printheads. In the printer, specific electronics, pen pockets, servicing stations, and other solutions need to be developed to work with the printhead, and the debugging of these systems is time- consuming and expensive.

To justify such large expenditures, the development of a new application space (i.e. signage or packaging), or a substantial market share increase in an existing space, must be expected and significant increases in key specifications are generally required to accomplish these goals. Once this required capability and the

corresponding printhead capacity have been established, there are strong financial incentives to utilize it for extended periods of time.

Platform Attributes and General Strategy

Key printhead attributes are listed in **Table 1**.

Key Printhead Parameters
Ink Colors
Print Swath Length
Nozzle Density
Distance between print columns
Firing Frequency
Drop weight
Ink compatibility
Uniformity of drop characteristics

Table 1 – Key printhead attributes

Other enabling attributes of printheads are listed in **Table 2.** Printheads in higher-cost applications tend to be more sensitive to these attributes.

Enabling Printhead Parameters
Printhead life
Power consumption
Temperature control capability
Servicing requirements

Table 2 – Enabling printhead attributes

If improvements in some of these attributes can occur within a platform without requiring all the investments required for a new platform, then that platform can be extended and its investments leveraged across longer time scales. Because the capabilities of the active circuitry on the silicon die determine many of the printhead's key specifications, updating the integrated circuit (IC) elements of the printhead is one method to improve a platform's performance over time to keep it competitive. A complementary method is to update the MEMS fluidic elements of the die to accommodate a new ink or new performance target.

Scalable Printing Technology (SPT) is Hewlett Packard's most advanced thermal inkjet technology as seen in **Figure 1**. SPT supports a large variety of printheads supporting printers and presses with *Average Selling Prices* (ASPs) varying by over four (4) orders of magnitude. **Figure 2** shows the range of ASPs that are supported by HP's SPT platform.

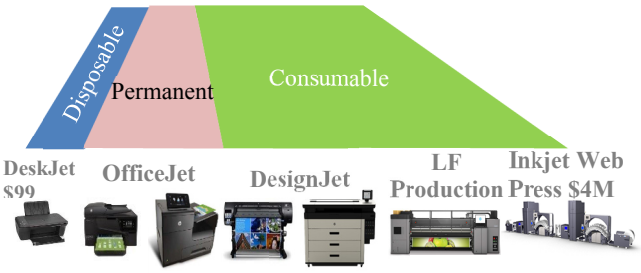

Figure 2 – Overview of HP's printer portfolio using SPT printheads

Obviously, key attributes—such as those in **Tables 1** and **2**—vary significantly for the printheads in these systems. The volume of printheads produced also varies dramatically across such a wide range of performance and price points, and therein lies an opportunity. If new features in silicon can be developed and shown to be effective for the higher performance, less cost-sensitive markets, then engineering optimization can make these features more cost-effective and feasible on higher-volume, lower-cost platforms. Once the second generation of silicon is proven, it can be substituted for the original design on the high performance platform. Often, this means silicon real estate becomes available for additional functions and new features, resulting in a virtuous cycle. Advances in silicon performance and features can lead to successive generations within a printhead platform, each with greater capabilities than the previous one, while retaining essential physical characteristics of the printhead assembly—the mechanical, electrical, and ink interconnects—and size and form-factor of the silicon die. This provides compatibility with existing assembly lines and printer platforms, which preserves manufacturing investments. For the printhead manufacturer, this strategy resides on two key tactics: reducing the silicon area required to support essential functions to free space on the die, and adding new features that the printer development partners and end-users will find valuable.

The existence of manufacturing and testing infrastructure on existing platforms reduces the innovation and investment required to develop and introduce the changes. In addition, new solutions that are form-factor compatible with existing solutions inherently confer another benefit: printer development partners can leverage existing printhead mechanical, electrical, and ink supply interfaces and hardware from existing platforms to allow faster and lower-cost product implementations.

Printhead Silicon Layout

For a new platform, the printhead layout and architecture on the silicon die is determined by technical capabilities, application requirements, and economic constraints. The productivity and quality requirements for the printhead—print swath, number of nozzles per inch, number of ink colors, and drop frequency—dictate the general configuration of ink feed slots, nozzle locations

and density, and data bus requirements. Together, these requirements define the performance of the printhead's integrated electronics on the silicon die. The specific layout is also governed by the IC space required, assembly constraints, and economic factors. An example printhead and a diagram with some critical layout features on the silicon die are shown in **Figure 3**.

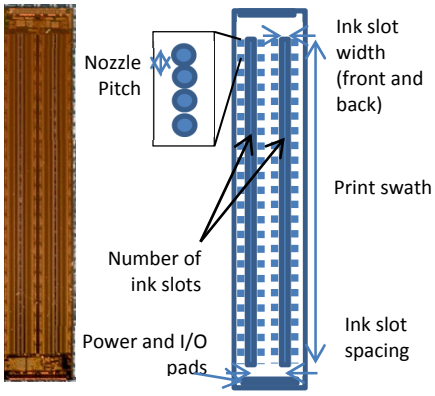

Figure 3 – Silicon printhead floor plan

Tall silicon die with long print swaths give the fastest print speeds; narrow die with small spacing between ink slots produce the most-economical printhead designs. But, there are practical limits to the aspect ratio of the printhead. In high aspect-ratio die, the silicon area between the ink slots must contain appropriate control and power devices on the front side (where the fluidic structures for drop generation will be added) and serve as an attachment point to one or more ink supplies on the backside. This attachment point must robustly segregate separate ink colors without leakage and mixing. In addition, the ink slots enhance concerns about die fragility during assembly. These concerns grow acute if the ink slots are too long or close together. These requirements create a natural tension between the economic advantages of narrow die—which allow more die per wafer and lower cost—versus lower yield due to rejects in assembly from either die breakage or failure to seal and ink mixing on the backside.

Because assembly costs often match or exceed silicon costs, higher-end platforms (whose volumes are less elastic in price) can accept a conservative design. However, when the market requires a high-volume, low-cost solution, then the resulting silicon design is typically more aggressive to lower manufacturing costs.

Technology examples: design and process improvements to reduce silicon area

As the number of electrical interconnections increase between printer electronics and the printhead circuits, strong drivers emerge for integrating CMOS and Power FET circuits into the printhead die. ICs allow serial data loading at high speed through a small number of interconnects, reducing costs on high nozzle count printheads. When developing a printhead die with ICs, obvious cost synergies result from having a common silicon substrate and common interconnect layers for CMOS and MEMS. A negative consequence of integration of MEMS and electronics is that Moore's Law will inevitably enable a lower-cost IC technology that is not realizable in the integrated printhead die due to the high development cost associated with each instance of integrating new circuits and MEMS devices. The outcome of these factors is that IC/MEMS processes typically have exceptional longevity, where multiple improvement cycles add features and cost reductions.

Some examples of features that have been added into HP's SPT process are listed below in **Figures 4 - 6**:

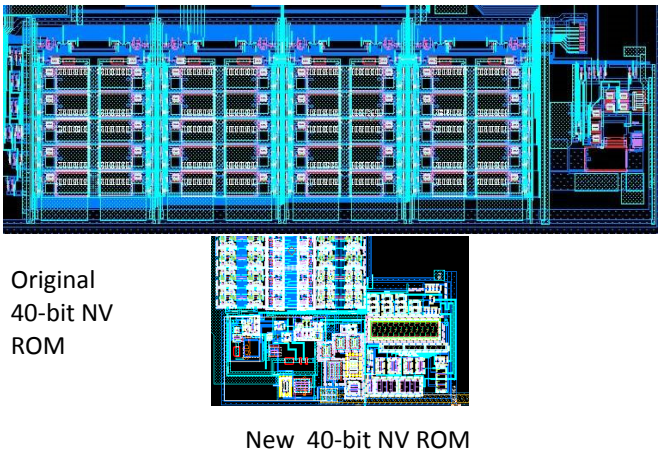

Figure 4 - Replacing Fuse-based non-volatile ROM with EPROM

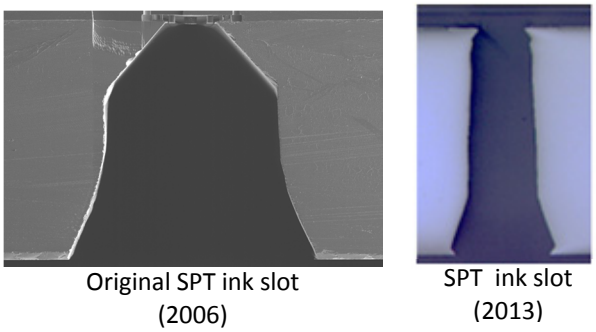

Figure 5 - Decreasing the ink slot backside width enables smaller spacing between ink slots

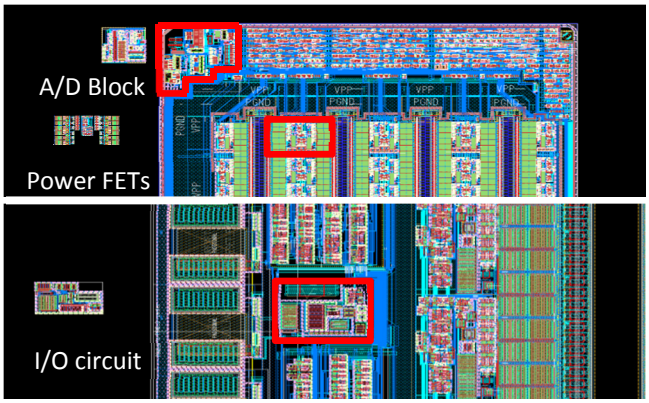

Figure 6 - Improved circuit elements (left side) vs. original (red outline)

These design and process improvements enable new smaller and cheaper silicon die or new versions of the silicon die for an existing platform with enhanced functionality placed into the reclaimed space.

Example of low-end platform improvement: circuit redesign and process changes

The original HP SPT process technology was designed to enable consumer, office, and industrial printing. A concerted effort was made to accommodate the needs of all three application spaces within a single process technology. This was necessary to focus resources and to facilitate learning across the different printheads being developed. As the consumer and office markets matured, the cost pressures on these platforms intensified. In addition, the scanning printhead technology employed reached fundamental productivity limits, and surpassing these limits required a transition to pagewide printhead technology—HP PageWide Technology— that had already been introduced and proven in commercial printing on HP's T-series Inkjet Web Presses. However, the manufacturing cost structure for the commercial printing solution was not suitable for an office product. These considerations led to the development of a simplified SPT process flow that could support the throughput and ink design requirements of consumer and office printers. The simplified process flow eliminated one layer of metal interconnect and its corresponding dielectric layer from the silicon process. This yielded a cost advantage while imposing a heavy interconnect burden on the remaining metal layers. The substantial design and process changes necessary for the new process led to substantial concerns about its suitability that could only be answered by qualifying it for use on a printer. The four ink slot 1.15" HP 950 printhead was selected for conversion to the new process. In undergoing the conversion a substantial savings on wafer manufacturing costs were possible without changing the die size, yield, or performance characteristics of the part. Conversion of the HP 950 gave HP office printing a clear "something for nothing" value proposition in that the high volume of printheads used in this application would now be cheaper to manufacture. Strategically, the qualification of the simplified process flow allowed for future lower-cost printheads to be pursued with confidence. The opportunity (due to underutilization of metal layers in the existing process) and challenge (extreme density of metal in the cost reduced process) is highlighted in **Figure 7,** which shows one of the interconnect layers for the HP950 printhead die before and after the process and design changes.

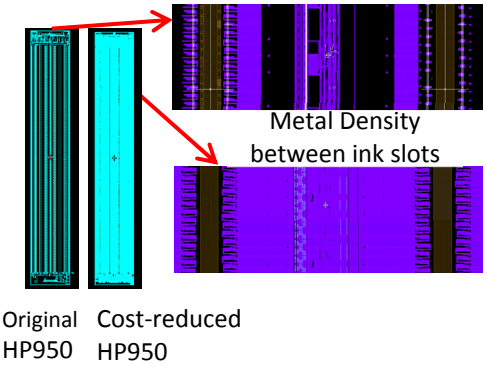

Figure 7 – Metal mask density of HP950 SPT printhead

This design change gave compelling short-term program benefits that justified the design and process development effort. It also gave the long-term strategic benefit of demonstrating the new platform, which enabled a lower cost structure for pagewide printing. Because nozzle counts go up dramatically on pagewide printheads (typically by an order of magnitude), the cost structure savings helped enable a new market opportunity for HP Thermal Inkjet: HP PageWide printing.

Example of high-end platform improvement: fluidics design and process changes

The original HP T300 Inkjet Web Press, introduced in 2009, utilized the CH57x and CH58x 4.25-inch HP SPT printheads. It was capable of printing mono (black-only) and color at 400 feet per minute (fpm). The electrical capability of this printhead exceeded the ink flows it was capable of sustaining under conditions of extremely high ink coverage. An electrically-compatible second generation solution was developed that improved the efficiency of the drop ejector, enabling higher ink fluxes and productivity. While the die size was unchanged, the process flow and fluidic design were optimized around the new performance level. As a result of changes to the thin film stacks, fluidic chambers, ink slotting technology, and printhead operating conditions, the maximum speed of the HP T300 was increased from 400 fpm mono and color to 600 fpm color and 800 fpm mono. The cost structure for the printhead remained unchanged, enabling a "something for nothing" value proposition for HP's inkjet web press division.

Example of high-end platform improvement: complete silicon redesign

In the previous examples, the essential elements of the printhead listed in **Figure 3** are unchanged, and either cost structure or performance enhancements were made to create a new value proposition. With HP High Definition Nozzle Architecture (HDNA) Technology in the new HP A53 Printhead,, the 4.25-inch

HP A51 Printhead platform is reused without changing the essential process flow or printhead dimensions, but the nozzle pitch is halved, enabling a doubling of the number of nozzles on the printhead[2,3]. **Figure 8** shows the nozzle density differences between the old (HP A51) and new (HP A53) versions of HP's 4.25-inch printhead.

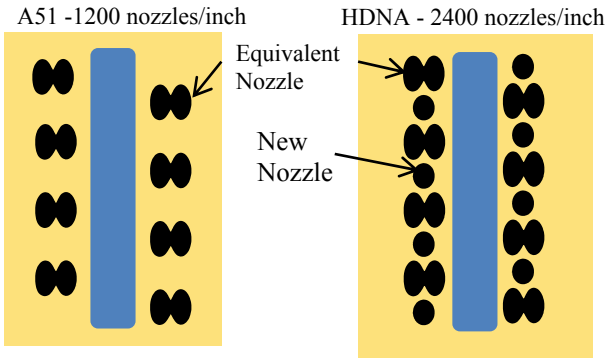

Figure 8 – HDNA nozzle density improvement

As a point of interest in **Figure 8**, the "bow-tie" shape of the larger nozzles is a non-circular bore designed to enhance drop break-off at high drop generation rates. This improves print quality. The HP A53 Printhead features dual drop weights, and the nozzles added between the larger ones produce smaller drops.

Data bandwidth and data path changes need to be made at the system level to support the extra nozzles, and this requires upgrading some of the web press electronics. But, the printhead and die form-factors are unchanged enabling existing web presses to be upgraded to HDNA Technology while reusing mechanical, electrical, and ink interface hardware in its pagewide print bars.

Summary

HP's Thermal Inkjet technology has dramatically increased the scope of its applications over time while maintaining its competitiveness in lower-end market segments in defiance of the "innovator's dilemma". Cost-sensitive markets have not been sacrificed—they are now served even better than before because HP has reinvested in new silicon designs for existing platforms with cost-reduced integrated circuit and process changes offering enhanced capabilities. These changes have also been leveraged across platforms providing a virtuous cycle of improvement that allows both cost-sensitive and high-performance SPT platforms to continually evolve.

References

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[2] "HP Pagewide Technology, Quality and Speed", http://www.hp.com/united-states/campaigns/pagewide/media/4AA5-7513ENW_hires.pdf

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Author Biography

Jim Przybyla has 35 years of Silicon and MEMS experience in the design, device and processing realms. At Hewlett Packard he initially worked on 8 generations of internal NMOS and CMOS development as a design, process, device and integration engineer. He began supporting inkjet development in 1998 and led the HP SPT CMOS and piezo printhead development efforts. In his current role he develops printhead technology for next generation printheads. He holds 26 US patents.

Jeff Hintzman has worked in silicon and MEMS processing and design for 25 years. He has worked on CMOS process development and was a member of the design team on several high performance ASICs. He has managed an EDA design tools group and currently manages integration engineers for HP's Scalable Print Technology thermal inkjet print heads. He holds 5 U.S. patents.

Robel Vina has 16 years of Silicon and MEMS process development, process integration, and product management experience. He began his career as a process engineer supporting 0.25 and 0.13um CMOS manufacturing. He has been at Hewlett Packard for the past 12 years, developing thermal inkjet print head technology. In his current role, Robel manages the Thermal InkJet Product Engineering team, charged with leading the TIJ silicon specification and design process, intro to manufacturing, and production ramps.