

Large-Scale Fabrication of All-Inkjet Printed Organic Thin Film Transistors: a Quantitative Study

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Abstract

In recent years inkjet printing technology has been increasingly applied as advanced deposition technology in the field of printed electronics.[1] The reasons for the awakening interest to use inkjet printing are the high flexibility in terms of patterns (mask-less) and materials, and the low cost approach as only a small amount of materials is required in comparison to other solution-based deposition techniques.[2].

Most of research works are based on laboratory inkjet equipment for manufacturing using single nozzle systems or small printheads and fabricating small numbers of devices. Therefore, the variability and mismatch of large quantities of printed devices are underrepresented in literature and are key factors towards commercialization of printed electronics. [3,4]

Our work focuses on the manufacturing of hundreds of all-inkjet printed Organic Thin Film Transistors (OTFTs) in A4 flexible foils using small R&D printheads. Electrical and morphological characterizations were performed in order to obtain device statistics to investigate the origins of the failures responsible for the decreasing yields. The statistical results of such characterization are studied and presented.

Introduction

The development of robust processes for manufacturing Organic Thin Film Transistors (OTFTs) circuits is a challenge due to the sensitivity of organic electronic materials, limitations in material compatibility and printing technologies restrictions. The device layout, architecture, and material selection have a strong influence on the choice of processing techniques and the fabrication procedure. In this work, we have been focusing our effort on inkjet printing of OTFTs. Several examples of all-inkjet printed OTFTs can be found in literature [5][6][7]. This work explores various aspects of OTFT fabrication, concretely the large-scale fabrication and characterization of transistors in sheet-fed configuration (S2S) by using inkjet printing technologies.

Although device materials and geometries can be identical, device performances can differ significantly according to the processing method. Because charge carriers moves through the semiconducting layer near the dielectric layer, the semiconductor–dielectric interface characteristics and the molecular ordering of the semiconductor is a key to achieve a high performance [8][9]. Dielectrics must be uniformly deposited to reduce the gate leakage current and source/drain electrodes should

be sufficiently conductive and have an appropriate work function for the effective injection of charge carriers. The satisfaction of these requirements would lead to functional transistors and facilitate the design of OTFT circuits manufactured by printing processes. The mere application of a printing method to OTFT fabrication does not necessarily imply the successful preparation of properly functioning devices and circuits.

The inkjet printing setup used in the present work is based on a Fujifilm Dimatix DMP2831 desktop printer. The device structures and geometries were defined taking into account the printing tolerances related to the employed printing systems.

First section will be devoted to introduce the device stack and geometry. Second section will introduce the characterization methodology used, and finally, last section will introduce the results of the characterization of large quantities of OTFTs.

Process description

Transistors based on organic semiconductors as the active layer to control current flow are commonly referred to as OTFTs, or sometimes Organic Field Effect Transistors (OFETs). Generally speaking, the OTFT MISFET (Metal-Insulator-Semiconductor FET) is composed of three electrodes (gate, source and drain). The source (S) and drain (D) electrodes directly contact the semiconductor, whereas the gate (G) electrode is separated from semiconductor by a dielectric layer. The gate turns the device ON and OFF with an applied voltage, and thus controls the current flow (I_{DS}) in the semiconductor between the source and drain electrodes.

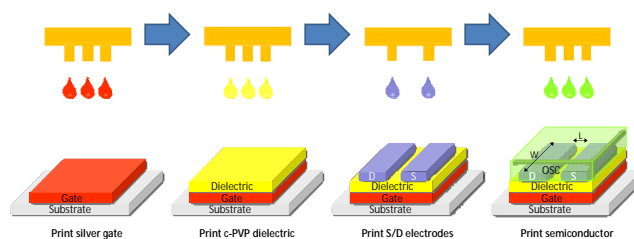


Figure 1. Manufacturing process for BG-BC OTFT by inkjet.

The OTFT structure is well adapted to low conductivity materials, and is currently used in amorphous and polycrystalline silicon transistors [10].

Various structures of OTFTs can be used in printed electronics. Each structure has its advantage and disadvantages. For inkjet printing processes, the solvent interaction between layers is critical. So, the most common structure is the bottom-gate and bottom-contact type (BGBC).

Figure 1 shows the manufacturing process for BGBC TFTs using solvent-based dielectric. At first, the gate was deposited on the substrate using silver nanoparticle ink with an average height of about 450nm and sintered on a convection oven. In the second step, the cross-linked Poly vinyl phenol (cPVP) dielectric was printed on top of the gate electrode followed by curing in convection oven in order to evaporate the solvents and polymerize the dielectric. A layer of 300 nm thickness was obtained although a pronounced coffee ring stain can be observed (**Figure 2**) in the extremes of the printed pattern. But immediately after the coffee ring wall a flat dielectric surface is obtained as can be seen. It is mandatory to increase the dielectric area to assure that coffee ring stain is outside the active area.

Next, the source-drain electrodes were printed using silver ink on top of the dielectric layer and sintered on a convection oven, as shown in Figure 2. Oxygen plasma was applied to improve the printability and finally, the OSC was deposited and cured on a heating plate.

The conductive ink used was Sunchemical's Silver ink EMD5603 (commercially known as Suntronic Jettable Silver). This ink is a 20% weight silver nanoparticle solution. An in-house developed cPVP ink was used to obtain well-defined and homogeneous dielectric layers. Finally, a p-type polymer (FS0027) organic semiconductor provided by Flexink Inc (UK) was used as active layer. The devices were constructed over a flexible PEN (125 μm) substrate (Dupont Teijin Teonex® Q65FA) pre-cleaned with ethanol.

The optimization of individual layers as well as the integration between layers is the main challenge in inkjet printing. Figure 1 shows the process steps layer by layer and **Figure 3** Left shows the final transistor fabricated.

The measurement of the dielectric cPVP was performed by optical profilometry and shows a layer thickness of approx. 740 nm using a measurement length of about 500 μm . When increasing the measurement length, the average layer thickness decreases to about 370 nm. In particular, the internal region of the printed cPVP area resulted almost flat with average thickness of around 400 nm.

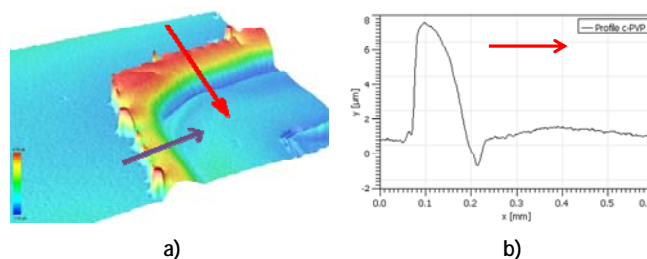


Figure 2. a) Confocal image of the c-PVP edge, b) characteristic cross section profile of c-PVP by optical profilometer. Purple arrow shows the printing direction.

The coffee ring stain is not homogeneous in all the cPVP layer sides. As it can be observed in **Figure 2**, the upper wall has an average thickness of 8.1 μm and an average width of 580 μm . But vertical walls have an average thickness of 4.9 μm with an average width of 450 μm . The ink coalescence causes a displacement of the ink to the top left part of the printed pattern.

The OTFT design uses finger-type (interdigitated) source/drain electrodes. Because of the low mobility of the organic semiconductors and the large channel length (>15-20 μm) due to inkjet printing restrictions, it is required a large channel width/length ratio to improve drain current through the channel. It is worth to mention that achieving a high resolution and low channel width without bulging effect [4], drain and source electrodes were printed in parallel to the printing direction.

Figure 3 Right shows a characteristic profile of source and drain electrodes printed on cPVP and characterized by optical profilometry. The electrodes show a clearly visible coffee-ring effect with peaks ranging from 20 to 200 nm. They have an average height of about 500 nm and a finger width of about 40 μm .

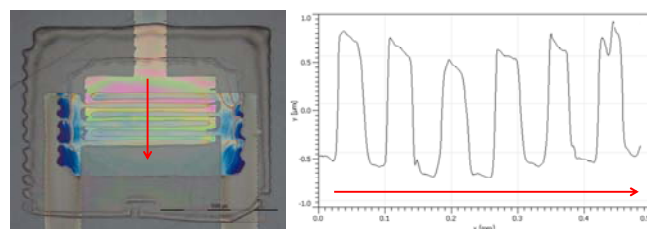


Figure 3. Left: all-inkjet OTFT; Right: cross section profile of S/D interdigitated fingers.

The previous image shows that the electrode profile is regular and with sufficient separation in order to obtain a reasonable yield.

But ink coalescence and wet/dewetting processes create different effects resulting in short and open circuits in S&D electrodes. In order to avoid these undesired effects, we have applied the compensation techniques based on extracting or adding

additional drops to electrodes and junctions, thereby improving the morphology of D&S electrodes and increasing the yield of the fabricated devices [4].

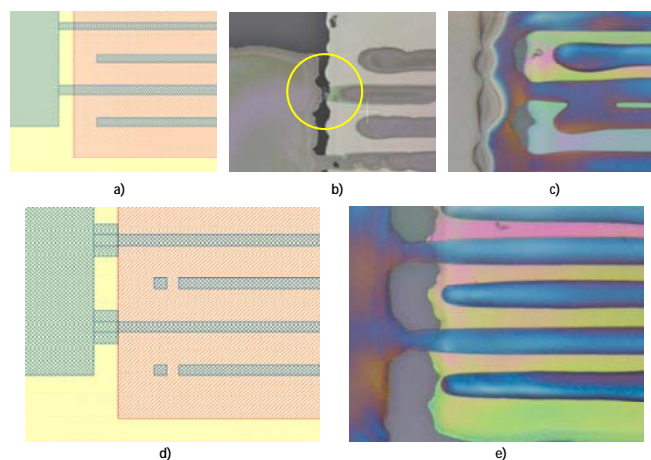


Figure 4. a) Layout of source & drain electrodes without compensations; b) and c) different effects occurred to non-compensated electrodes and junctions; d) Compensated layout; and e) Compensated electrodes.

Figure 4 shows the different printed patterns obtained with and without the application of compensation strategies. **Figure 4** b) and c) shows different effects that occurred to non-compensated electrodes and junctions such as a bulging effect at the end of the electrodes creating short circuits between D&S electrodes (**Figure 4** c) and strangled junctions producing open circuits (**Figure 4** b).

Characterization of all-inkjet printed OTFTs

Several hundreds of devices were fabricated using the device structures and geometries defined taking into account the tolerances related to the employed printing system.

The output and transfer curves exhibit the typical OTFT characteristic, as shown in **Figure 5** and **Figure 6**.

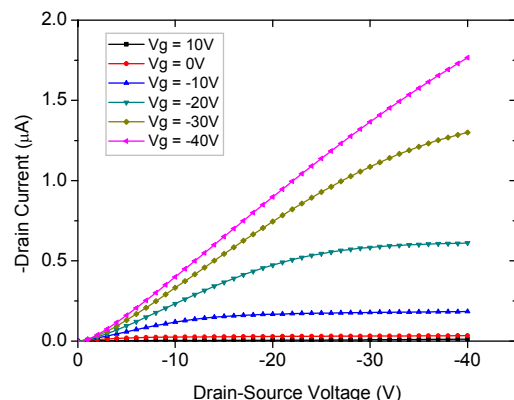


Figure 5. Output characteristics of the inkjet printed OTFTs.

Good results were obtained in the all-inkjet printed transistors. A mobility up to $3.4 \cdot 10^{-4} \text{ cm}^2/\text{V}\cdot\text{s}$, with a threshold voltage (V_T) of -1.4V, an On/Off ratio up to 200 and a maximum drain-source current of $1.76 \mu\text{A}$ were achieved for a transistor having a $L=40 \mu\text{m}$ and a $W=10 \text{ mm}$ (W/L ratio = 250) as shown in **Figure 5**. 1350 transistors with different W/L ratios were printed obtaining an average yield near 50%. The OTFT devices with reduced W/L ratios showed the best yield.

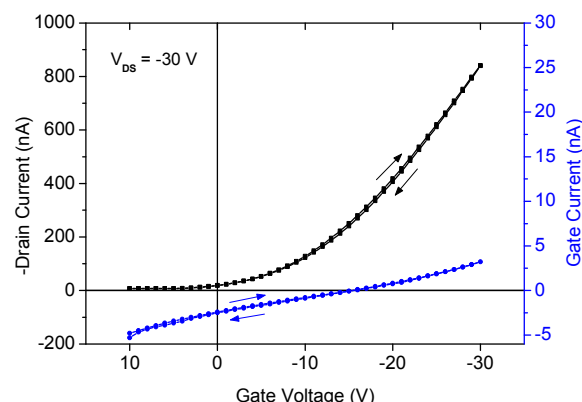


Figure 6. Drain-source current and Gate current curves for OTFTs with V_{DS} ranging from +10 to -30V.

Although these good results, OTFTs still suffer from an important Off-current (thus decreasing On-Off current ratio), some contact effects and device instability.

For a proper integration in future electronic circuits, the electrical properties of the OTFTs need to be stable over a long period of time, otherwise the lifetime of the end product would be too short to be commercially viable.

The high sensitivity of most organic semiconductors to ambient conditions or environmental influences, such as oxygen, humidity, light, and temperature, creates a huge limitation on the performance and stability of OTFTs [11]. For example, atmospheric oxygen and moisture, as well as photo-induced oxidation have a doping effect on the organic material, causing an increase in the conductivity which degrades the On-Off current ratio, hysteresis, threshold voltage shifts and off-current increases. Often these are not caused by the semiconductor but by the dielectric or the printed integrity of material stack.

As expected and based on existing literature [12], after prolonged exposure to oxygen and moisture the proper transistor behavior was lost. Oxidative doping upon air and moisture results in an uncontrolled increase in the conductivity losing the channel modulation property of the organic semiconductor as shown in the measurements made during 3 weeks. Off-current increases up to 209.15 nA reducing drastically the On/Off current ratio and declaring OTFT non-functional.

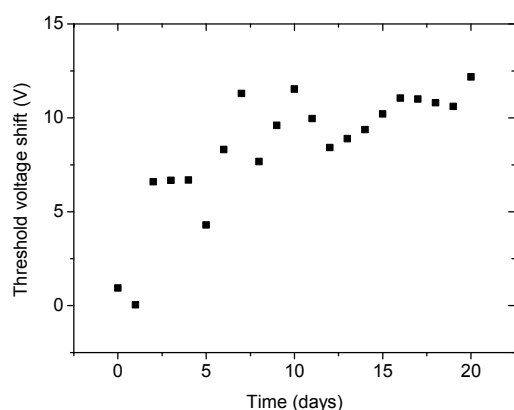


Figure 7. Threshold voltage shift vs time by static bias stress.

Nevertheless, the main change in the transistor behavior starts just 48 hours after its fabrication and exposure to air and moisture. Although it cannot be observed a big change in mobility and the drain current at On-state, the change is observed in Off-current and Threshold Voltage. Initially the V_T is close to zero increasing to -6.6V after 48h of exposure to ambient conditions. After this increase, the parameter slowly increases up to -11V after 21 days of exposure limiting its applicability in organic circuits.

Large-scale fabrication of inkjet-printed OTFTs

Process variations present during transistor fabrication lead to a certain variability on the resulting transistor parameters. The structural disorder inherent in thin-film semiconductor leads to challenges in the design and fabrication of robust OTFT circuits, because the disorder limits charge transport and reduces uniformity across devices [13].

A large-scale OTFT manufacturing was fabricated and characterized in order to study the variability, scalability and yield of all-inkjet printed OTFTs. OTFTs were fabricated at UAB and characterized at IMB-CNM facilities using a semiautomatic probe station. **Figure 8** shows a printed foil and the characterization setup. The amount of samples manufactured by the fully inkjet printing approach can be considered as outstanding achievement.

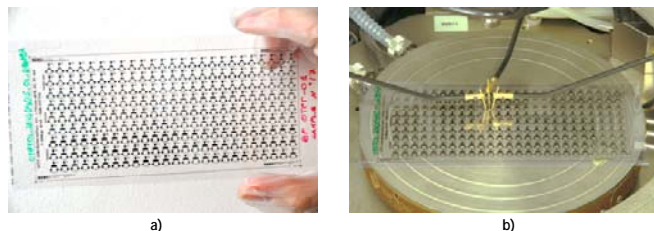


Figure 8. Left: Batch of OTFTs devices fabricated by S2S process; Right: OTFT characterization matrix under test [14].

A large number of OTFT foils were designed and fabricated with different device geometries and W/L ratios: 125, 250, 500, 750 and 1000 and with short- and large-finger topologies. The channel length (L) was designed to be 40 μm . But, as previously studied, due to ink coalescence and the dielectric surface tension, the final dimensions obtained were in the range of 14.1 to 24.6 μm with an average of $19.1 \pm 3.4 \mu\text{m}$.

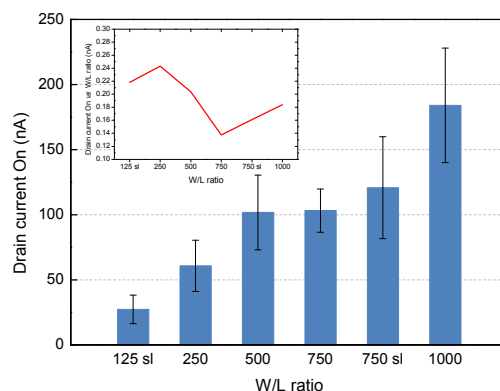


Figure 9. Drain current at On-state as a function of W/L ratio.

Figure 9 depicts the drain Ion current for different W/L ratios. Current increases linearly following the W/L ratio increase. Inset graphs show the normalized Ion current value per W/L ratio to compare different OTFT sizes and evaluate scalability. In both cases, the normalized current can be considered close to constant coefficients resulting proportional to transistor area. Differences can arise by geometric effects. One reason is due to that current density extends beyond of the region of drain and source electrode overlap (lateral conduction effects), resulting in an increase of the effective width of the device. The current density flowing outside the electrode overlap depends on the channel length (L) and on the device structure.

Figure 10 inset shows the yield of the large batch of devices fabricated as a function of the W/L ratio. Transistors with higher W/L ratios have lower yield percentages. The result is clearly showing that increasing the number of fingers (higher W/L ratios) equals to higher chances of non-working devices. The yield obtained was 78.7% for a W/L ratio of 125 and 26.7% for a W/L ratio of 1000.

However, the yield is not only related to W/L ratio or transistor geometry. Printing effects are mostly governing the final yield. **Figure 10** shows the yield per printed row grouped by W/L ratios. It can be seen that the distribution of failures is not uniform per row. Some rows shows very low yields (any or just some OTFTs working) decreasing the yield of the W/L ratio group that in another row is showing good percentages. E.g. the W/L ratio of 750 with large-fingers has two rows without a single working OTFT and a row with a 60% of yield closer to the average.

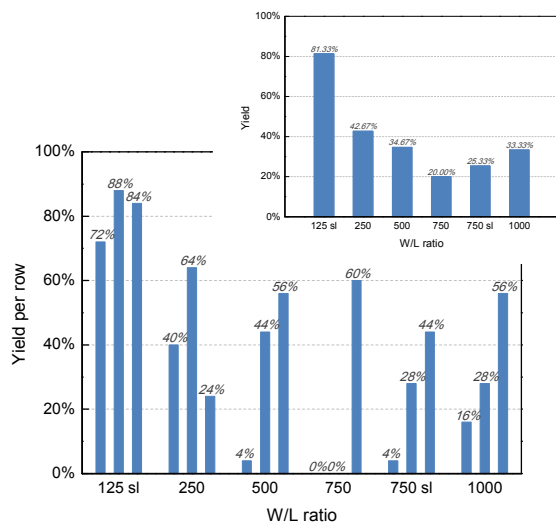


Figure 10. Yield as a function of printed row grouped by W/L ratios, Inset: yield versus W/L ratio.

It is important to remember that the direction of printing is from left to right row by row. The deposition of the different layers uses a number of nozzles ranging from 3 to 12 depending on the materials deposited, and the printhead is periodically purged and cleaned. That means that if some nozzles clogs, deviated drops or satellite drops appears at some moments of the printing process, this problem is not solved until the next cleaning process, affecting a complete row of OTFTs.

From the variability point of view, we studied the variation of transistor performance proportional to the transistor area. We focused on intra-foil variations (currently named within- or intra-die WID variations), which are categorized as deviations of the transistor parameters in the same foil.

Figure 11 depicts the ratio between standard deviation on On-current and the average of On-current versus the transistor area respectively. We can observe that the percentage of spread in On-current increases linearly with decreasing square root of transistor area, as already demonstrated by Myny et al in [15].

For a reliable technology in, e.g. display applications, the absolute value and the spread on On- and Off-current, V_T and mobility at large negative VGS values are key parameters.

Conclusions

A complete manufacturing process operation for inkjet printing and post-treatment methods has been developed based on the materials evaluated.

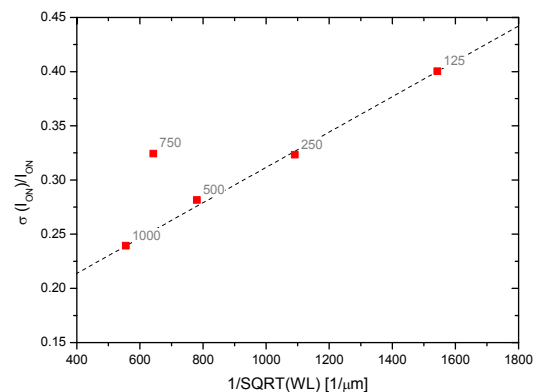


Figure 11. Intra-foil standard deviation of parameters of the p-type organic TFT plotted versus the inverse square root of the transistor area, measured on one sheet. The dots are the obtained measurements; the dashed line is the corresponding fit. The label of the red dots shows the W/L ratio for each OTFT.

Layers and their geometries were designed and assembled to multilayer stacks to build-up OTFTs successfully. For the geometries, printing tolerances were taken into account related to the employed printing system to ensure efficient manufacturing and parameter variation. The manufactured layers and devices were also characterized according to the morphological and functional properties of the individual layer as well as the performance of the complete device.

The OTFTs fabricated and characterized displays values of μ around $3.4 \cdot 10^{-4} \text{ cm}^2/\text{V} \cdot \text{s}$, $I_{ON}/I_{OFF} \sim 10^2$, and V_T ranging from 0 to -8V, but they are all-inkjet printed and fabricated at room conditions.

Several hundreds of OTFTs were manufactured using the current recipe developed and all of them fully inkjet-printed. All of the devices were characterized. Yields up to 78% for a fixed design were obtained.

The primary sources of the variability are (i) printing effects during the fabrication and (ii) the morphology and thickness variations in the deposited functional layers, which are more pronounced in inkjet printed than in photolithographic processes.

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