High-resolution Patterning Technologies using Ink-jet Printing and Laser Processing for Organic TFT Array

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Abstract

A 150 ppi organic thin film transistor (OTFT) array, which TFT have pixel circuit with two transistors and one capacitor was fabricated by printing methods and laser processing. TFT array pitch was 169 μm, a minimum width of the source electrode was 15 μm, channel length was 5 μm, and a diameter of via hole was about 20 μm. We have developed the surface energy controlled ink-jet printing with UV irradiation for fine Ag electrodes and the conventional ink-jet printing for organic semiconductor (OSC), and laser processing for Via hole.

Introduction

In recent years, printed electronics are gaining attention as a technology that enables various electric devices such as organic thin film transistors (OTFTs) [1, 2], RF-ID tags [3], printed circuits [4], sensors [5], displays [6] to be fabricated using printing process. This is because printing technologies have their potential for low cost, low environmental impact and large area fabrication. Then, several printing methods such as ink-jet printing, flexographic printing, screen printing, gravure printing, off-set printing have been developed to fabricate these devices. Ink-jet printing method has advantages of on-demand process, non-contact printing process and its scalability. However, one of the important problems is the resolution. A typical resolution using a conventional ink-jet printing method is limited around 50 μm. Therefore various methods have been proposed to improve resolution of printing using bank structures [2], self-assembled monolayer [7] and laser irradiation during ink-jet printing [8]. Another important problem is to connect two TFTs through a via for more functional devices such as RF-ID, printed circuit and sensors.

In previous work, we have developed the surface energy controlled ink-jet printing technique with UV irradiation son a novel polyimide for high-resolution electrode patterning [9] and fabricated 160 ppi all-printed TFT array on plastic substrate in 2008 [10, 11]. Then, we published 200 ppi all-printed TFT array and demonstrated a 200 ppi electronic paper display in 2009 [12]. Furthermore, we fabricated finer TFT array, a 300 ppi all-printed OTFT array on plastic substrate in 2010 [13]. Those TFT have pixel circuit with a single transistor and a storage capacitor (1T1C) for electrophoretic display, which is driven by applying a voltage across the two electrodes. TFT array pitch for 300 ppi with 1T1C is 85 μm.

In this paper, we have developed a new fabrication process of printed OTFT array using the surface energy controlled ink-jet printing and laser processing to connect two TFTs. And to integrate these methods, we fabricated current driven TFT array, which TFT have pixel circuit with two transistors and one storage capacitor (2T1C) [14]. TFT array pitch is 169 μm.

Experiment

TFT structure

Figure 1 shows a schematic cross-section of printed OTFT array with 2T1C. OTFT array pitch is 169μm. TFT is bottom-gate bottom-contact structure. The gate electrodes of both two transistors were fabricated using Ag nanoparticles ink by the surface energy controlled ink-jet printing. The gate insulator was a novel polyimide film fabricated by spin coating. Via hole was fabricated using excimer laser ablation, and diameter of via hole was about 20 μm. The source/drain (S/D) electrodes of both two transistors consist of Ag were also fabricated by surface energy controlled ink-jet printing method. During this step, the drain electrode of the switching transistor (Tsw) was electrically connected to the gate electrode of the driving transistor (Tdr) through a via. Small-molecule OSC for 150 ppi OTFTs with 2T1C was fabricated by conventional ink-jet printing under ambient conditions.

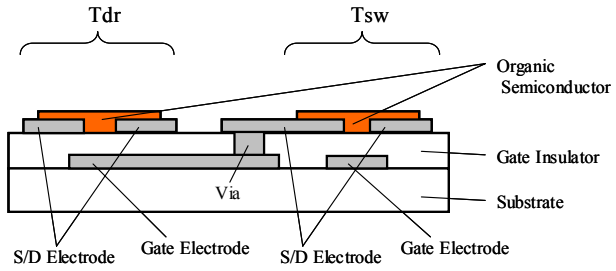

***Figure 1**. Schematic cross-section of a printed OTFT array with 2T1C.)*

Surface energy controlled ink-jet printing process and laser processing

We have developed a new hybrid process of the surface energy controlled ink-jet printing and laser processing for high-resolution and high-functional electrode patterning (see Figure 2). To contact two electrodes, additive process is only laser ablation compared with our previous surface energy controlled ink-jet printing methods.

The novel polyimide film was fabricated on electrodes by spin coating, whose surface had low surface energy after post-baking in N_2 condition at 180˚C (Figure 2(a)). Next, via hole was made by selective removal of the polyimide film using an excimer laser (KrF λ=248nm) (Figure 2(b)). After UV irradiation from super-high pressure mercury lamp through a photo mask from the front side of the substrate, the high surface energy area corresponding to electrode patterns and the low surface energy area were formed on the novel polyimide film surface (Figure

2(c)). Hydrophilic Ag nanoparticles ink was ink-jetted onto the high surface energy area and spread over the edge of the area with via hole filling (Figure 2(d)). After post-baking under ambient condition at 180˚C, the fine electrode patterns with via were fabricated. Using this novel polyimide as an insulating layer, additional fabrication process of wiring is only two photo process. One is exposure process without such wet process as development and cleaning. The other is laser processing to make electrical connection of two electrodes through a via. Thus, our hybrid process of the surface energy controlled ink-jet printing and laser processing takes advantage of practical number of process steps. Using laser processing for via hole we are connecting two more TFTs, and can fabricated higher functionality.

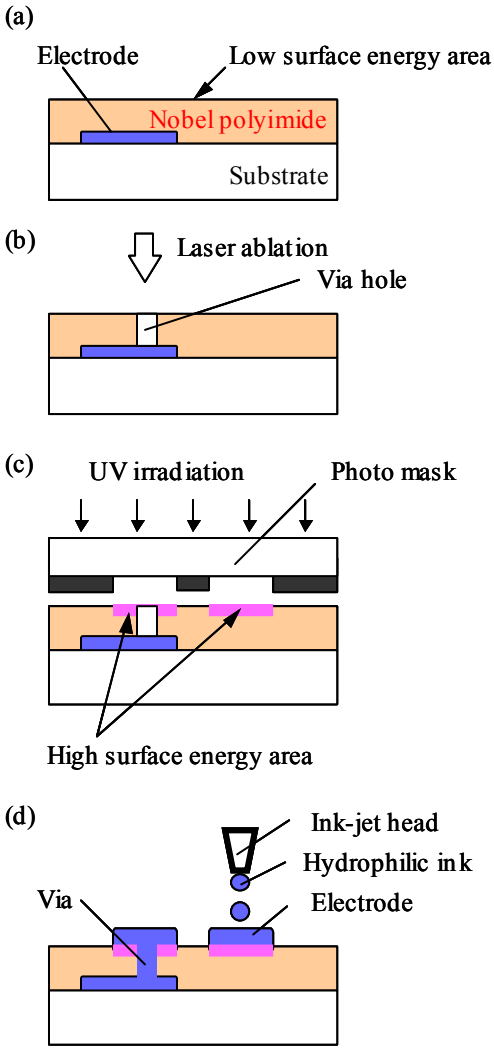

***Figure 2**. Schematic of the surface energy controlled ink-jet printing process (a) novel polyimide film coating, (b) Via hole pattering, (c) Formation of areas with different surface energy by UV irradiation, (d) Fabrication of electrodes with via by ink-jet printing*

Results and Discussion

Electrode printing

Figure 3 shows an optical micrograph of electrode patterns overlaid with the gate insulator (a) without and (b) with the surface energy controlled ink-jet printing. Electrodes without the surface energy controlled ink-jet printing (Figure 3(a)) show droplet-like shape and rough surface with interference fringes, which depends on the difference of the film thickness due to surface roughness of electrodes. On the other hand, electrodes with the surface energy controlled ink-jet printing (Figure 3(b)) show photo mask-like sharp profile and very smooth surface because of no interference fringes.

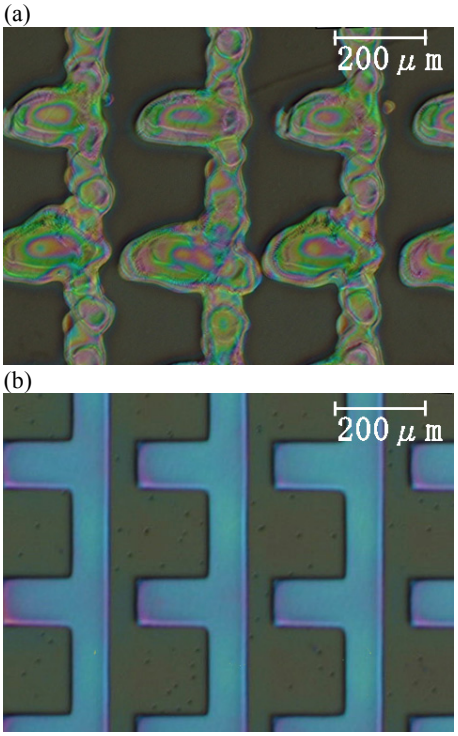

***Figure 3**. Optical micrograph of electrodes (a) without and (b) with the surface energy controlled ink-jet printing*

To investigate the minimum space between two electrodes, we prepared a photo mask with various line and space patterns. After UV irradiation on the novel polyimide film through the photo mask, hydrophilic Ag nanoparticles ink was ink-jetted. Controlling with ink-jet printing conditions such as drop size and ink volume per unit line, two kinds of electrodes with different thicknesses were fabricated. Figure 4 shows the dependence of the yield of electrodes separation on designed space against electrode thickness. Yield means the ratio of separation between the two electrodes and was determined by using an optical microscope with 100 points in one sheet. Figure 4 shows that minimum space up to 2 μm (designed) could be fabricated using the surface energy controlled ink-jet printing with UV irradiation on the polyimide film. In this case, minimum space of this photo mask was 2 μm. Then, smaller designed space of 1.0, 0.8, 0.6, 0.4 μm was investigated. Figure 5 shows the electrodes with minimum space

0.8 μm (1.4μm measurement) was successfully fabricated for our process. Then, our surface energy controlled ink-jet printing is superior in the resolution to conventional ink-jet method.

We also examined alignment margin of electrode fabrication by this ink-jet technique, increasing the distance between the center of high surface energy line pattern and that of ink droplets impinging position 10 μm. Figure 5 shows that electrodes with linewidth of 80 μm can be successfully formed same as photo mask patterns apart from the center of the ideal impinging position by a distance of 50 μm. This is because the hydrophilic ink droplets, which land onto the low surface energy area, could be drawn into the high surface energy area. It is necessary to control jetting conditions such as velocity deviation and angle deviation from ink-jet nozzles for the conventional ink-jet printing precisely. Otherwise, the alignment margin of our process was very large such as ±50 μm for linewidth of 80 μm. Then, our process was robust for jetting conditions.

Thus, the surface energy controlled ink-jet printing technique possesses such unique features as good surface roughness, high-resolution patterning and high alignment margin because of using a photo mask.

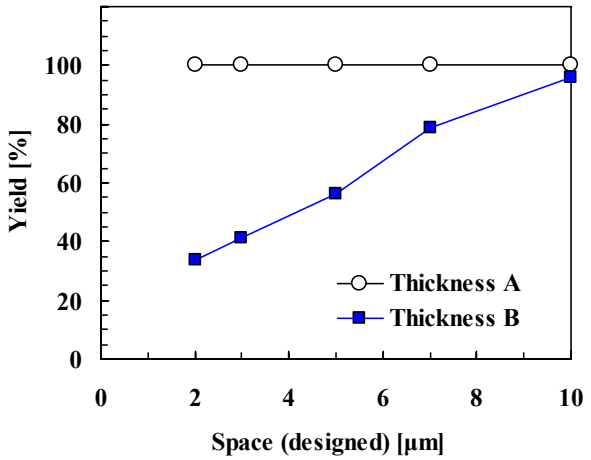

Figure 4. *Relationship between yield of electrodes separation and designed space against electrode thickness*

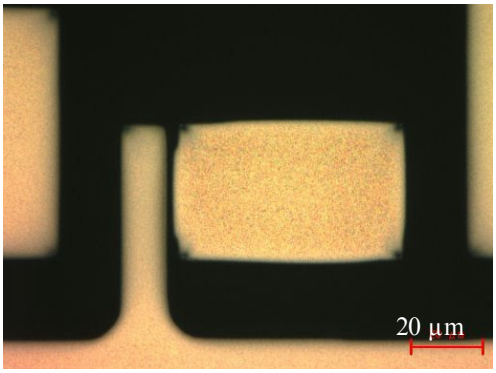

Figure 5. *Optical micrograph of electrodes with minimum space 0.8 μm (1.4 μm measurement).*

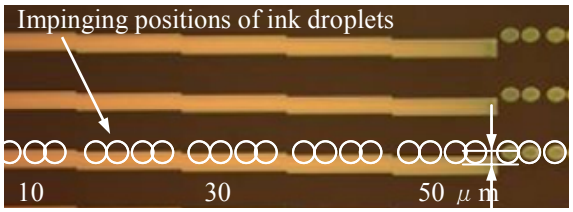

Figure 6. *Optical micrograph of electrodes with linewidth of 80 μm to show alignment margin of the surface energy controlled ink-jet printing. White circles show impinging position of ink droplets*

Via formation

To confirm via formation process experimentally, we fabricated via-hole chain test pattern. Both line width of upper electrode and lower electrode were 60 um. Diameter of via-hole was 20um and number of via-hole in series was 960. We fabricated successfully all via without any failure to optimize such as the upper and lower electrode thickness and laser ablation condition. Electrical connection between two electrode layers was also confirmed and resistance per via is below 0.1 Ohm. Figure 7 shows a SEM image with cross-section of via of test pattern. As shown in this figure, via-hole filling and upper electrode formation with fine shape can be confirmed.

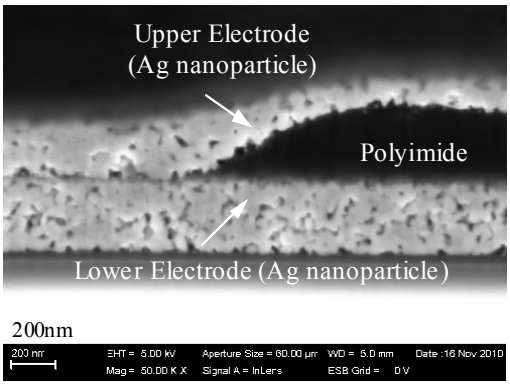

Figure 7. *A cross-section SEM image of a via.*

Process integration of TFT array

For printing process, deposition and pattering is same step. This point of view is very important for process integration of printing process. In general it is difficult to achieve fine electrode patterning and low resistivity at same time. Therefore, we optimized the electrode thickness and the curing time for low resistivity. The electrode thickness was controlled by ink-jet condition such as ink volume per unit line. For example, the electrical resistance per unit length at 30 μm linewidth was 0.5 kΩ/cm.

We have fabricated a 300 ppi (TFT pitch is 85 μm × 85 μm) all-printed OTFT array with 1T1C on plastic substrate (see Figure 8). The minimum linewidth of the gate line and the source line were 25 μm, 20 μm, respectively. And both of the minimum space

of the gate line and the source line were 10 µm. A channel length was 3 or 5 µm, a channel width is 57µm.

Next, we have optimized TFT design such as the line and space of the gate electrode and the S/D electrode. Adding to new laser ablation process for via formation, we have fabricated a 150 ppi (array pitch is 169 µm × 169 µm) printed OTFT array with 2T1C (see Figure 9). The minimum linewidth and the minimum space of the gate line were 25µm and 10 µm, respectively. And the minimum linewidth and the minimum space of the source line were 15 µm, 10 µm, respectively. A channel length was 5 µm, a channel width is 40µm. Via hole diameter is 20µm. Optimizing the surface of the gate insulator and small molecule OSC ink formulation such as the solvent and the concentration, OSC profile was separated with each others at 169 µm pitches without any bank structure. Maximum process temperature was 180˚C. All printing process, UV irradiation and laser process were done in air. Therefore, we showed a low cost, low environmental impact and high functional manufacturing process with the finest photo-assisted printed TFT array.

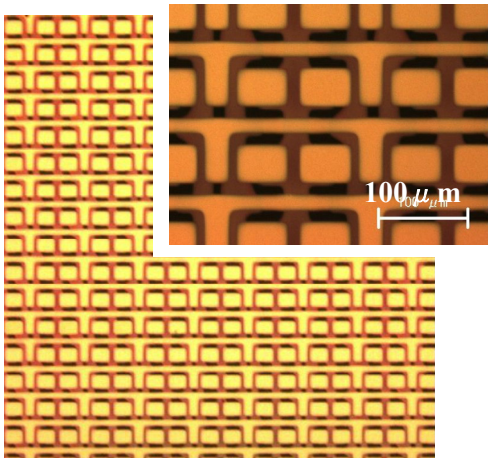

***Figure 8**. Optical micrograph of a 300 ppi printed OTFT array with 1T1C (after S/D electrode fabrication).*

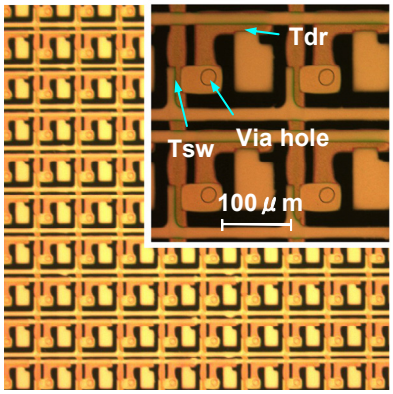

***Figure 9**. Optical micrograph of a 150 ppi printed OTFT array with 2T1C (after S/D electrode fabrication).*

Performance of OTFT

The transfer characteristics of a 150 ppi printed OTFT with 2T1C, W/L = 40 µm / 5 µm after OSC printing. Mobility of 0.19 cm^2/Vs, Vth of 5.4 V, an on/off current ratio of 10^6 at Vds = -20 V were obtained after small-molecule OSC printing (see Table 1). These value were almost same as those of 300 ppi all-printed OTFT with 1T1C. High on/off current ratio is because of the separation of small-molecule OSC patterning with high mobility of TFT to optimize small molecule OSC printing process. As shown in figure 10, transfer characteristic of driving transistor can be controlled by voltage "Vsel" applied to switching transistor. Then we showed the switching characteristics of two transistors through via.

Table1 Transfer characteristics of 150 ppi 2T1C and 300 ppi 1T1C

	1T1C	2T1C
Channel length L [µm]	5	5
Channel width W [µm]	57	40
Mobility [cm^2/Vs]	0.25	0.19
Vth [V]	1.3	5.4
on/off current ratio	> 10^6	~ 10^6

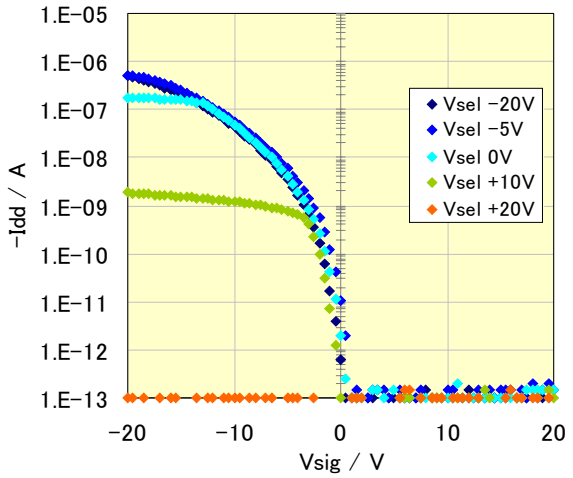

***Figure 10**. Static Characteristic of Integrated Transistor Circuit of a 150 ppi with 2T1C (Channel length L = 5 µm).*

Conclusion

We have developed the surface energy controlled ink-jet printing with UV irradiation for Ag electrodes and the conventional ink-jet printing for OSC, and laser processing for Via hole. To integrate these printing methods and laser processing we have succeeded in fabricating a 150 ppi OTFT array with 2T1C. Laser processing method, surface energy controlled ink-jet printing method and conventional ink-jet printing method have very high affinity to digital fabrication. Then, our hybrid process of the surface energy controlled ink-jet printing and laser processing is promising for high-resolution, high-functional, low-cost and low-environmental impact manufacturing process.

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Author Biography

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