Patterned by Printing—a New Approach to Printed Electronics

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Abstract

Today's printed electronic elements are formed by printing the active materials in the desired patterns, requiring that the active materials be formulated into a printable form. We explore an alternative approach to printed electronics where the patterning is achieved by printing, but the active material is deposited via atomic layer deposition (ALD). We thus separate the ink-like requirements from the active materials requirements. In this "patterned by printing" approach to printed electronics, a director material is printed that inhibits the deposition of the functional material. The active material is globally applied but only deposits in the areas where the director is not present—and as such is patterned at the time of deposition. In our work, the active materials are deposited by an atmospheric pressure, roll-compatible spatial ALD (SALD) process. Details on the director materials and printing techniques are discussed, and results from thin film transistors (TFTs) will be presented.

Introduction

Common threads in printed electronics today are high materials usage and high throughput (low cost), high substrate latitude (electronics everywhere), and the use of digital patterning (low-volume manufacturing and custom designs). Typical printed electronics efforts employ processes wherein the active layers of an electronic device are digitally printed. Using additive printing processes for fabricating printed electronics requires that semiconductors, dielectrics, and electrode materials have ink-like as well as electronic properties. This need for active materials to be "printable" greatly restricts the materials available for use in the formation of printed electronics, and has to date limited device performance.

The "patterned by printing" approach removes the ink-like constraint from the additive material, and in our case requires a single director ink formulation to build complete devices or circuits. It also relaxes the constraints on the quality of printing required. In additive printed systems, the active materials interfaces are formed in the printing steps and layer uniformity is critical. As we will demonstrate, a relatively non-uniform printed director does not influence the ability of the director to direct and the active materials interfaces are formed via spatial atomic layer deposition (SALD), leading to low defect interfaces.

There are three key elements in our "patterned by printing" approach: 1) spatial ALD (SALD), 2) director materials and mechanisms, and 3) printing methods. In this paper we will walk through the important aspects of each element, and link them into a process flow for thin film transistors (TFTs). New performance data from representative TFTs made using this methodology clearly show the potential to form high quality devices and ultimately circuits.

Spatial Atomic Layer Deposition

The majority of ALD reactors are enclosed systems used to expose a substrate to a succession of reactants, by introducing and then evacuating the precursor and inert gases. While this approach is very successful at producing high-quality films, there are limitations. First, it requires a chamber to allow control of precursor introduction and purging, and the chamber must therefore be larger than the substrate under consideration. Second, the ALD chamber rarely operates at steady state. Instead, a sophisticated valving operation is required, leading to equipment complexity and a constantly varying composition of precursors in the chamber. Third, the purging process generally takes significantly more time than the exposure, leading to relatively slow growth rates.

An alternative to the above approach is to confine each of the reactive gases to particular spatial regions of a deposition head [1], [2] and allow relative movement of a substrate to accomplish the alternate exposures of the ALD cycle. The schematic of a spatial ALD system (Figure 1) shows a substrate and the localization of precursor and inert gases in channels. As the substrate moves, each point on the substrate sees the sequence of localized gases originating from the coating head. The actual sequence is very similar to that experienced in a chamber-based ALD system. As with chamber ALD, the success of the process requires that any gas phase mixture of the precursors be avoided. In the case of the SALD system, this means that the composition of the gas experienced at any point on the substrate must change sharply as the point is moved from one gas channel to another. Our system employs linear inlet and exhaust slots, and carefully designed pressure gradients to prevent gas mixing. The arrangement of gas channels on the surface of the coating head is shown in Figure 1, along with the desired localization of gases.

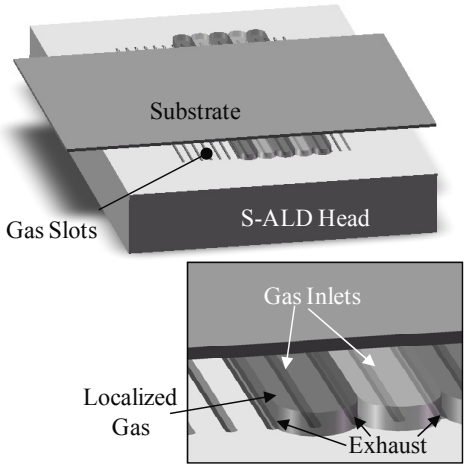

Figure 1. *Schematic of SALD head, showing localized gas flows. Substrate oscillates over the different precursor and inert inlets to build up a film.*

In operation, the substrate is allowed to approach the head until the pressure field resulting from the gas flow supports the substrate, much like a hockey puck on an air table. The closeness of the substrate to the head forces the gas emitted from an inlet slot to flow only to the adjacent exhaust slots, and additionally makes the effective chamber size very small, leading to high turnover rates for each channel and thus improved gas isolation. In typical deposition conditions, the entire channel volume is replaced in a few tenths of a millisecond.

Our models and experiments indicate very good gas isolation, regardless of the speed at which the substrate travels over the head [2]. However, reaction times need to be fast enough so that nearly complete exposure will take place in the residence time of the substrate over a channel, and this provides the limit to how fast the system can operate at a given temperature.

The high degree of gas isolation provided is essential not only for separating the ALD reactants, but also for isolating the ALD reaction system from the surrounding ambient. The result is that the SALD system is able to operate in open air without any confinement while the deposition region environment is perfectly controlled. This gives a substantial advantage in footprint and equipment complexity, as the deposition system can be smaller than the substrate and requires no chamber and no sequenced vacuum pumping.

Director materials and mechanisms

Selective deposition, while possible with CVD [3] and even physical vapor deposition by the use of masking oils [4], appears to be most useful in the ALD process. Because of the low-energy nature of the ALD process, it is possible to apply inhibiting materials to a deposition surface that prevent subsequent ALD growth. Thus, hard inorganic materials deposited by ALD can be patterned without the use of post-deposition photolithographic and etching steps. Typical printed electronics materials, such as organic semiconductors, can also be deposited with relatively simple patterning processes. However, the quality of ALD-deposited semiconductors and dielectrics cannot be matched by organic materials. Leveraging selective deposition with a "patterned by printing" use of inhibitors has the potential to distinguish ALD, and in particular, large-area ALD, from other inorganic deposition methods.

The inhibition of ALD growth can be achieved by the use of self-assembled monolayers [5] (SAMs) as well as polymers [6,7]. The inhibition by SAMs is likely due to removal of surface-reactive sites by attachment of a chemically inert monolayer, although effects of monolayer chain length suggest that prevention of precursor diffusion is an important feature. Polymer inhibition likely relies upon prevention of reactant diffusion. This is evidenced by studies of mass uptake of reactant by polymer films on quartz crystal microbalances in ALD chambers [6]. While the prior work has demonstrated and explored the mechanisms of ALD selective deposition, the refinement of the process to a point where it can be used as a primary patterning method for large-area electronics has not been developed. Practically, the SAMs method is difficult to pattern, while polymer solutions maybe easily formulated for printing.

It is known that polymers such as poly(methyl methacrylate) (PMMA) can be very effective selective deposition inhibitors.[6] In our laboratory and using the spatial ALD system, we have demonstrated that very thin layers of PMMA inhibit the growth of ZnO.[8] For a bare glass substrate, as expected, film growth occurs almost linearly with the number of ALD cycles. The presence of PMMA inhibits the growth, as evidenced by a period of no measurable ZnO growth during a number of ALD cycles. PMMA layers as thin as 9 Å (confirmed by ellipsometry and consistent with spin coating models) offer some inhibition while thicker layers, still only approximately 40 Å, inhibit enough to be useful for device patterning. [9]

Generally, it is considered that nonpolar or inert polymers are required to perform the ALD inhibition, which limits useful polymers to ones such as PMMA that require organic solvents. Large-scale printed patterning operations can experience problems with the strong solvents found in PMMA. We find that certain water-soluble polymers make excellent selective deposition inhibitors for the deposition of ZnO and related materials. In particular, many polymers that do not contain low pKa moieties, such as polyvinyl alcohol and polyvinylpyrrolidone (PVP), enable excellent selective deposition.

Like PMMA, thin layers of PVP can inhibit the SALD growth of inorganic materials useful for devices. We have seen in the lab that that 50 Å of PVP is sufficient to inhibit more than a 1000 Å of ZnO (for example). PVP is soluble in many solvents making it an excellent candidate for use as the director material in the "patterned by printing process." This versatility of PVP enables it to be formulated into inks that can be printed by a variety of methods.

Printing approaches

Using hydrophilic polymers like PVP, inhibiting inks for printing can be formulated using water or simple alcohols, and subsequently patterned by inkjet or transfer printing techniques such as flexography. Unlike additive printing for active materials, a single simple ink formula is sufficient to make complete devices because the different active layers are each inhibited by the same "ink"

In our lab we have used both flexography and inkjet printing for printing our director materials. The director is printed as the inverted pattern (negative) of the desired final active material pattern. In this methodology, steps that are difficult in standard semiconductor processing such as vias are easy to accomplish, as the insulator is simply not permitted to grow where the via is desired.

We have found in the lab that as long as the thinnest portion of the coated pattern is above the minimum director thickness required to inhibit the desired active material film thickness, the uniformity of the director thickness is not important. This loose uniformity requirement allows additional freedom in ink formulation as well as large tolerance in overall print quality.

The optical micrograph in Figure 2 illustrates the quality of a typical director pattern. The pattern is that of the source-drain contacts for a planar thin film transistor (TFT). The region between the two "T" structures defines the channel of the TFT. In this instance the director material is PVP K-30 formulated in diacetone alcohol and printed with a Dimatix 2800 piezo inkjet printer. The Dimatix 2800 piezo inkjet printer has 16 nozzles

which print in a swath. The ridges visible in Figure 2 are the overlap areas between printed swathes.

It is critical that the inhibitor completely inhibits the growth of the conductor over the semiconductor in the channel to insure that the electrodes do not short. . A close-up of the print quality in the channel area can be seen in Figure 3. Typical transistors to-date have been printed using 10 pL droplets, and a single row of drops is used to define the channel. There is clear evidence of the "coffee-ring" effect in Figure 3, evidenced by the thicker edge, but such print artifacts in the director pattern still produce quality transistors.

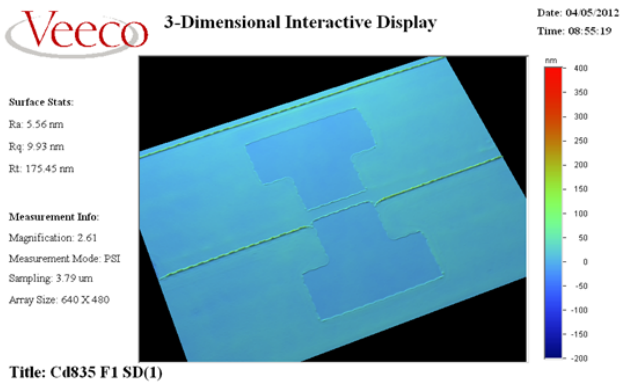

Figure 2. *Veeco Wyko optical profiler image of inkjet printed director pattern; the printed area shown is 2.4 mm x 1.8 mm.*

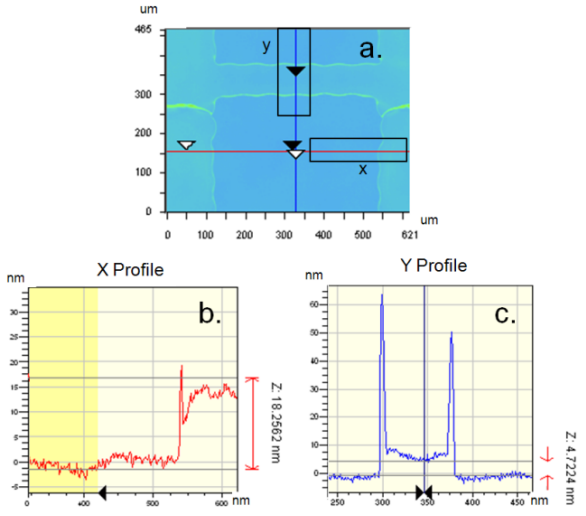

Figure 3. *A 3D representation of inkjet printed PVP director as measured by a Veeco Wyko optical profiler is shown in a. Graphs b. and c. are the cross-sectional profiles within the boxes drawn in a.*

Figure 4 shows approximately 1000 Å of aluminum-doped zinc oxide (AZO), which was patterned by a printed director as in Figure 3. There is a clear translation of the inhibitor pattern to the grown film, as seen by the scalloped edges in inset c. of Figure 4. We have found that this artifact has not limited our device performance; however in applications where a straight edge is required more care would be needed in patterning the director. In contrast to the uniformity and film quality of the printed director, the AZO film is flat, with a relatively smooth surface and vertical edges along the pattern boundary.

Although we have not discussed inhibitors printed by flexography in detail here, the same rules apply – namely that print artifacts and non-uniformities in the director material are tolerable as long as a minimum thickness is obtained. We have found that inhibitor performance is dependent on the material and the layer thickness, not on the method of deposition.

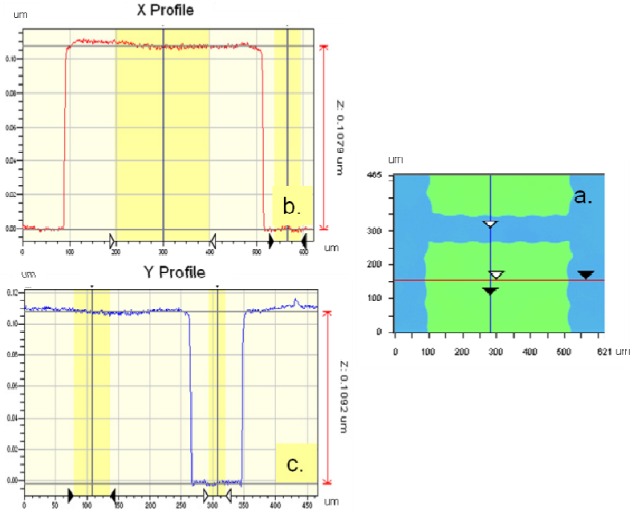

Figure 4. *A 3D representation of a directed AZO film as measured by a Veeco Wyko optical profiler is shown in a. Graphs b. and c. are the cross-sectional profiles along the lines drawn in a.*

"Patterned by printing" Devices

"Patterned by printing" devices are formed by combining the three key elements discussed above. An active material process block would be to clean the substrate, print the director pattern, deposit the active material via SALD, and then clean the substrate to remove the director pattern. The director may be removed using a number of methods including oxygen plasma or solvent wash.

Recently we have formed TFTs wherein all device layers were deposited by SALD: source / drain and gate were composed of aluminum doped zinc oxide (AZO) while the dielectric and semiconductor were Al_2O_3 and ZnO, respectively. Prior to each deposition, an inhibiting pattern of polyvinylpyrrolidone (PVP) was applied using flexographic printing or inkjet printing. Both printing methods yielded functional TFTs with mobilities of 2 cm^2/Vs or greater. Details on the flexographic devices can be found in Reference [9].

Table 1 outlines the inkjet process flow used for forming our bottom gate TFTs. Typical SALD depositions are carried out at 200°C; lower and higher temperature depositions have been used and 100°C is roughly the lower limit for device quality film growth. Residence times and gas flows are optimized for each material based on the precursors. The total time for each SALD step, including loading and unloading the sample is less than 15 minutes. Printing and substrate cleaning are relatively fast operations, in our experimental runs using 2.5" substrates, cleaning and printing are each on the order of 5 minutes. Thus complete devices can be fabricated in a couple of hours using only three

processing tools. There is potential to design each of these processing tools for roll-2-roll operation, implying that not only is the "patterned by printing" approach simple but it should be scalable to large scale high-throughput manufacturing.

Table 1: Typical process flow for a "patterned by printing" bottom gate TFT.

	Process	Equipment	Material
1	Clean	O_2 Plasma	-
2	Print gate pattern	Inkjet Printer	PVP k-30
3	Deposit conductor	SALD system	1000 Å AZO
4	Clean	O_2 Plasma	-
5	Print dielectric pattern	Inkjet Printer	PVP k-30
6	Deposit dielectric	SALD system	500 Å Al_2O_3
7	Clean	O_2 Plasma	-
8	Print semiconductor pattern	Inkjet Printer	PVP k-30
9	Deposit semiconductor	SALD system	200 Å ZnO
10	Clean	O_2 Plasma	-
11	Print source-drain pattern	Inkjet Printer	PVP k-30
12	Deposit conductor	SALD system	1000 Å AZO

Figure 5 an optical image of a completed a bottom gate TFT made according to the process flow in Table 1 and its performance. Curves are shown for the transistor in the linear regime (Vd = 0.2 V) and the associated gate leakage. The device shown had a mobility of 5.6 cm^2/V-s. This experiment had 84 devices; greater than 90% of the devices were functional with an average mobility of 7 cm^2/V-s. As can be seen from Figure 5, print artifacts can be tolerated in the "printed by patterning" approach. These devices were formed on a silicon substrate and devices made on glass substrates have been found to have equivalent performance. There is ongoing work in our lab to translate this process to various types of substrates including Kapton® and Teslin®.

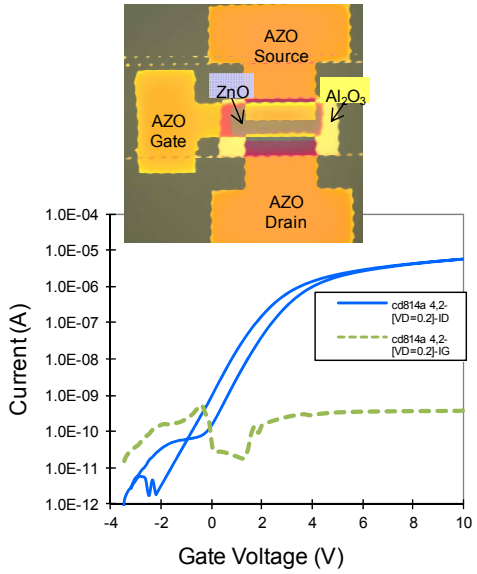

Figure 5. *An optical microscopy image of a "patterned by printing" TFT and the corresponding performance curves for drain current (solid) and gate leakage (dashed).*

Conclusions

In summary, we have discussed the important aspects of our "patterned by printing" approach to printed electronics. This approach to printed electronics has a simple process flow with only three necessary pieces of equipment, implying a manufacturing process that would only require process control and understanding of three fundamental processes. We have shown fully "patterned by printing" devices with performance rivaling that of devices made with standard semiconductor industry process. This combination of quality devices, additive patterning, and simple processing steps leave us excited about the future of devices and circuits formed using "patterned by printing."

Acknowledgments

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