Metal Oxide Transistors with Good Substrate Latitude

Shelby F. Nelson, Lee Tutt, David Levy, and Mitchell Burberry; Kodak Research Laboratories, Eastman Kodak Company; Rochester, NY USA

Abstract

When considering "printed electronics," the substrates of interest can vary from smooth glass to flexible polymeric supports, and even to rough paper. Relatively few standard semiconductor processes adapt readily to a wide variety of substrates. We will discuss an approach to thin-film electronics that uses the conformality of atomic layer deposition to produce good-quality metal oxide thin-film transistors on a wide variety of substrates.

Deposition of the active materials is by an atmospheric pressure, roll-compatible process called spatial atomic layer deposition (SALD), and the materials deposited are metal oxides. Electrical properties of SALD-grown planar thin-film transistors include mobility above 20 cm^2/V-s, high on/off ratios, and good uniformity of the deposited layers.

In addition to depositing good-quality thin-film transistor layers at temperatures of 200 °C, this process allows for decent transistors at temperatures down to 100 °C, thus opening up the range of usable substrates.

A novel vertical transistor geometry that exploits the conformal nature of the SALD deposition system will also be introduced. This device architecture shows good electrical properties and could provide a promising approach for both rigid and flexible substrates.

Introduction

The field of zinc oxide (ZnO)-based electronics has shown significant growth in past years because of features that include high mobility [1], the ability to form ternary and quaternary systems that exist as amorphous films [2], and excellent electrical and chemical stability for materials that are grown at relatively low processing temperatures [3],[4]. Typical oxide deposition methods require vacuum processing, which can limit the ability to handle continuous substrates and can add processing complexity.

In this work, we describe oxide-based devices produced by a rapid atmospheric pressure atomic layer deposition (ALD) system termed Spatial Atomic Layer Deposition (SALD). This process can operate in open atmosphere and is extendable to large or continuous substrates.

Spatial Atomic Layer Deposition

The majority of ALD reactors are enclosed systems used to expose a substrate to a succession of reactants, by introducing and then pumping the precursor and inert gases. While this approach is very successful at producing high-quality ALD films, there are limitations. First, it requires a chamber to allow control of precursor introduction and purging, and the chamber must therefore be larger than the substrate under consideration. Second, the ALD chamber rarely operates at steady state. Instead, a sophisticated valving operation is required, leading to equipment complexity and a constantly varying composition of precursors in the chamber.

An alternative to the above approach is to confine each of the reactive gases to particular spatial regions of a deposition head [5], [6] and allow relative movement of a substrate to accomplish the alternate exposures of the ALD cycle. The schematic of a spatial ALD system (Fig. 1) shows a substrate and the localization of precursor and inert gases in channels. As the substrate moves, each point on the substrate sees the sequence of localized gases originating from the coating head. The actual sequence is very similar to that experienced in a chamber-based ALD system. As with chamber ALD, the success of the process requires that any gas phase mixture of the precursors be avoided. In the case of the SALD system, this means that the composition of the gas experienced at any point on the substrate must change sharply as the point is moved from one gas channel to another. Our system employs linear inlet and exhaust slots, and carefully designed pressure gradients to prevent gas mixing. The arrangement of gas channels on the surface of the coating head is shown in Fig. 2, along with the desired localization of gases. The substrate is allowed to approach the head until the pressure field resulting from

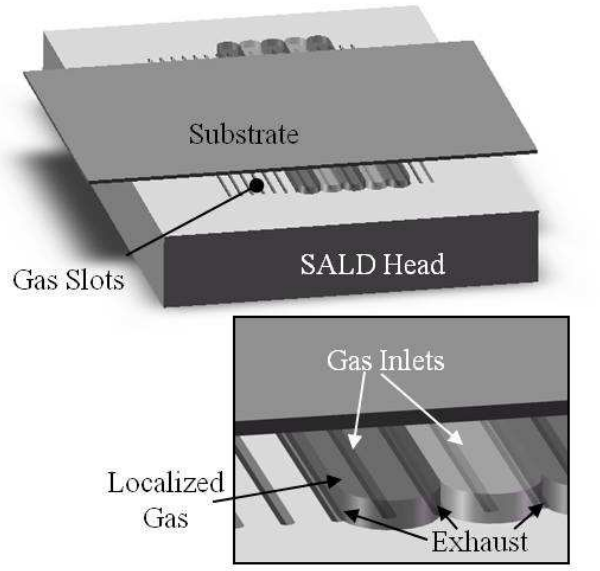

Figure 1. *Schematic of SALD head, showing localized gas flows. Substrate oscillates over the different precursor and inert inlets to build up a film.*

the gas flow supports the substrate, much like a hockey puck on an air table. The closeness of the substrate to the head forces the gas emitted from an inlet slot to flow only to the adjacent exhaust slots, and additionally makes the effective chamber size very small, leading to high turnover rates for each channel and thus improved

gas isolation. In a typical operation, the entire channel volume is replaced in a few tenths of a millisecond.

Our models and experiments indicate very good gas isolation, regardless of the speed at which the substrate travels over the head [6]. However, reaction times need to be fast enough so that nearly complete exposure will take place in the residence time of the substrate over a channel, and this provides the limit to how fast the system can operate at a given temperature.

The high degree of gas isolation we provide is essential not only for separating the ALD reactants, but also for isolating the ALD reaction system from the surrounding ambient. The result is that the ALD system is able to operate in open air without any confinement while the deposition region environment is perfectly controlled. This gives a substantial advantage in footprint and equipment complexity, as the deposition system can be smaller than the substrate and requires no chamber and no sequenced vacuum pumping.

ZnO Thin-Film Transistors

Typical thin-film transistors are planar and often have the form of the staggered-inverted structure shown schematically in Fig. 2. For our routine measurements, a substrate coated with chromium serves as the gate contact. The SALD system is then used to deposit an Al_2O_3 film of approximately 500 Å at 200 °C. During this deposition, the partial pressure of TMA in the metal channels is 220 mtorr, while the partial pressure of water in the

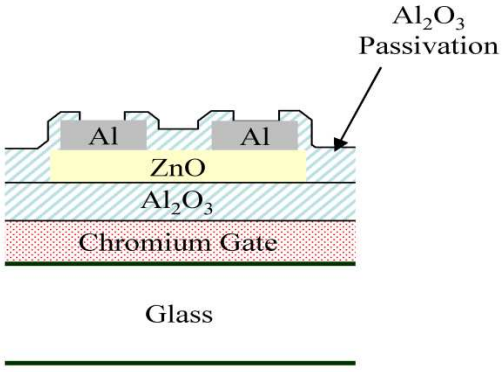

Figure 2. *Schematic (not to scale) of staggered inverted thin-film transistor with passivation.*

oxygen source channels is 230 mtorr. The substrate speed yields a channel residence time of 100 ms (the same for all precursor and inert streams), and a growth rate of 0.92 Å/cycle is obtained.

The ZnO semiconductor layer, with thickness varying from 120 Å to about 300 Å, is deposited on top of the Al_2O_3 dielectric, using the same equipment but with the metal channels now containing a partial pressure of DEZ of 310 mtorr. The total time for loading the sample and depositing the insulator and semiconductor, and unloading the sample is less than 10 min.

Aluminum top source and drain contacts are patterned from a lithographic lift-off process. The TFTs are isolated by etching the ZnO, using PMMA to protect the channels, using a very dilute nitric acid solution. After the PMMA is stripped, a final passivation layer of 300 Å thick Al_2O_3 is deposited under the same conditions as for the gate dielectric.

Devices made this way on glass show typical peak mobility of over 20 cm^2/V-s in both the saturation and linear regimes, for devices with channel lengths of 5 µm and longer. The SALD deposition system shows remarkable thickness uniformity (less than 0.2% across the width of the deposition), and the electrical uniformity follows suit. In current designs, for example, as measured over 240 TFTs distributed across the deposition area, the typical threshold voltage variation measured is less than 50 mV.

Devices can also be fabricated at lower deposition temperatures. A series of samples was prepared on glass substrates with deposition temperatures of 200 °C, 150 °C, and 100 °C, for direct comparison, as shown in Fig. 3. The difference

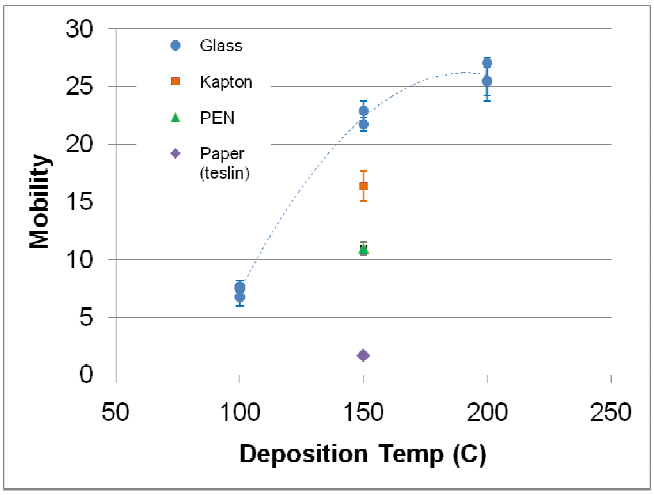

Figure 3. *Thin-film mobility as a function of deposition temperature on glass substrates. Similar depositions at 150 °C on Kapton, PEN, and artificial paper (Teslin) are included.*

between 200 °C and 150 °C is relatively small, while below 150 °C the properties appear to degrade more quickly. However, the mobility even at 100 °C is over 6 cm^2/V-s, remarkably enough. The threshold voltage variation, shown in Fig. 4, is not large. Importantly, the gate leakage was comparable on the glass substrates over the whole temperature range. While the stability of ZnO devices grown at 200 °C is excellent [6], that of the lower temperature devices has not been measured.

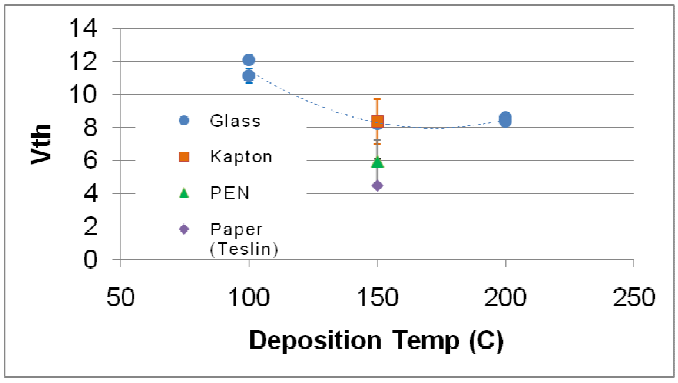

Figure 4*. Threshold voltage (Vth) variation as a function of deposition temperature on glass substrates, with comparison to Kapton, PEN, and artificial paper samples grown at 150 °C.*

For comparison, similar depositions were performed on a polyimide (Kapton) substrate and on a PEN substrate. The Kapton shows a mobility of 16 cm^2/V-s, slightly higher than the 11 cm^2/V-s achieved by the PEN sample. Although not part of the same series, a similar experiment on synthetic paper (Teslin), deposited at the same temperature, showed that the extremely rough paper had working transistors, but with a mobility of only about 1 cm^2/V-s, and noticeably worse gate leakage characteristics. More experiments are underway to understand the substrate dependence of these properties.

Vertical ZnO Thin-Film Transistors

Patterning and alignment of planar transistors on flexible supports continue to be a challenge for short channel lengths. A solution to this can be found in a novel vertical transistor architecture enabled by the conformality of atomic layer deposition processes. The vertical transistor (VTFT) architecture has both high alignment tolerance as well as submicron channel lengths and is further compatible with flexible supports.

By using a reentrant profile at the edge of the gate, we coat with SALD to give uniform films of gate insulator and ZnO semiconductor that maintain the reentrant profile. Deposition of the drain-source electrodes by a beam deposition process automatically yields a transistor. A cross-sectional SEM of one transistor architecture that employs this approach is shown in Fig. 5. In this figure, a dielectric of aluminum oxide overhangs the gate metal electrode to give the reentrant profile. The sample was conformally coated with the insulator and semiconductor. Evaporative deposition of aluminum provided the drain and source, divided from each other by the reentrant gap at gate edge.

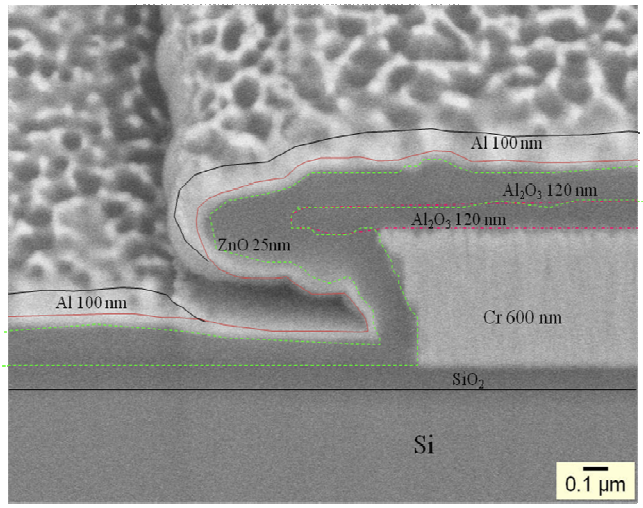

Figure 5: *Cross sectional view of a vertical transistor: The SEM picture shows the reentrant profile as well as the excellent conformal coating properties of the SALD process. Pitting of the aluminum electrodes was incurred during the focused ion beam (FIB) cross-sectioning.*

In the best design, the transistor's drain current ranges from about 10^{-11} A at a gate of -2 V to almost 1 mA at a gate of 10 V, for a drain voltage of 1.2 V, showing promise of good performance at low voltage. These vertical transistors can also be constructed on flexible substrates.

In summary, the combination of conformal coatings and good electrical performance give SALD-grown devices good potential for emerging applications where traditional thin film materials and processes face significant challenges.

References

[1] B. Bayraktaroglu, K. Leedy, and R. Neidhard, "Microwave ZnO thin-film transistors," *IEEE Electron Device Lett.*, vol. 29, no. 9, p. 1024, 2008.

[2] K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, and H. Hosono, "Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors," *Nature*, vol. 432, p. 488, 2004.

[3] P. Görrn, P. Hölzer, T. Riedl, W. Kowalsky, J. Wang, T. Weimann, P. Hinze, and S. Kipp, "Stability of transparent zinc tin oxide transistors under bias stress," *Appl. Phys. Lett.*, vol. 90, p. 063502, 2007.

[4] D. H. Levy, D. Freeman, S. F. Nelson, P. J. Cowdery-Corvan, and L. M. Irving, "Stable ZnO thin film transistors by fast open air atomic layer deposition," *Appl. Phys. Lett.*, vol. 92, p. 192101, 2008.

[5] T. S. Suntola, A. J. Pakkala, and S. G. Lindfors, "Method for performing growth of compound thin films," U.S. Patent 4 413 022, Nov. 1, 1983.

[6] D. H. Levy, S. F. Nelson, and D. Freeman, "Oxide electronics by spatial atomic layer deposition," *J. Display Tech.*, vol. 5, no. 12, 2009.

Author Biography

Shelby Nelson is a Senior Research Scientist at Eastman Kodak Company. She received her Ph.D. in Applied Physics from Cornell University, and has worked on device physics in a variety of organic and inorganic electronic materials at the IBM T. J. Watson Research Center, as a professor at Colby College, and at Xerox Corporation. She joined Kodak Research Laboratories in 2001.