Optimization of Inkjet-Based Process Modules for Printed Transistor Circuits

Huai-Yuan Tseng, Shong Yin, Vivek Subramanian
Department of Electrical Engineering and Computer Sciences, University of California, Berkeley
144MA Cory Hall, Berkeley, CA 94720-1770, Phone:510-643-4232, Fax:510-642-2739 Email: hytseng@eecs.berkeley.edu

Abstract

We report on the development of inkjet-based process modules for printed transistor-based circuits. The requirement for realization of printed transistor-based circuits is the capability to print consistent fine lines for transistor electrodes and uniform/conformal layers of insulators and semiconductor islands on top of the printed electrodes by optimizing the printing parameters and surface energy of the underlying layers. The baseline processes accomplished the above-mention requirement were developed. In addition, we demonstrate novel process modules such as self-alignment of transistor electrodes, printed self-aligned interconnect and printed local interconnect by simultaneous dissolving and connecting the underlying metal layers. Lastly, a printed inverter circuit utilizing the complete printing modules was demonstrated to illustrate the simplicity and the feasibility of the inkjet-based process modules towards the realization of low-cost printed electronics

Introduction

Printed electronics, an emerging field of electronics, has gain increasingly research activities in recent year due to its capability of realizing low-cost and disposable printed RFID tag and flexible display. The low-cost origins from the solution processable materials such as metal nanoparticle, polymeric insulator and soluble organic/inorganic semiconductor that allows the usage of printing technique such as screen printing, gravure printing and inkjet printing to avoid the capital costly vacuum based equipment [1]. Moreover, the additive printing process further reduces the waste abatement cost. As a result, low-cost fully printed electronic active and passive devices have been demonstrated in our previous works [2]. However, inkjet-based process modules specifically for transistor based integrated circuits have not been studied. Therefore in this work, the printing process of electrodes, layers and the manipulation of the surface energy for printed circuit consideration have been examined. In addition, novel printing results such as self-aligned transistor, self-aligned interconnect, local interconnect by dissolving and contacting were demonstrated. Finally, the case study of printing an inverter was discussed.

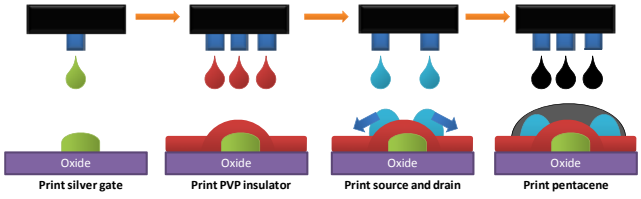

Figure 1*. The process flow of an inkjet printed transistor*

Baseline Printing Processes

The process for printing a bottom-gate and bottom-contact transistor is shown in Fig. 1. All inkjetting was performed using a Dimatix DMP-2800 printer and oxidized wafer were used as substrate. As illustrated by the transistor structure, the gate surface roughness would determine the leakage current and breakdown field of the insulator. In addition, comformality and surface roughness of the insulator have a strong impact on the transistor mobility. Therefore, the significant printing parameters associates with device performance were discussed.

A. Print electrodes

Printed electrodes are essential for realizing gate, source and drain (S/D) and interconnections in the printed circuit applications. Silver nanoparticle ink (Suntronic U5603) was used throughout this work. Significant parameters of a printed electrode are line width, roughness. Lines height and width can be controlled by printing multiple layers; however, the possibility of miss-alignment arises between layer-to-layer registrations. Instead, single layer of printing with various drop spacing is extensively used to control the width and height. Printed line width and height as a function of drop spacing are shown in Fig. 2.

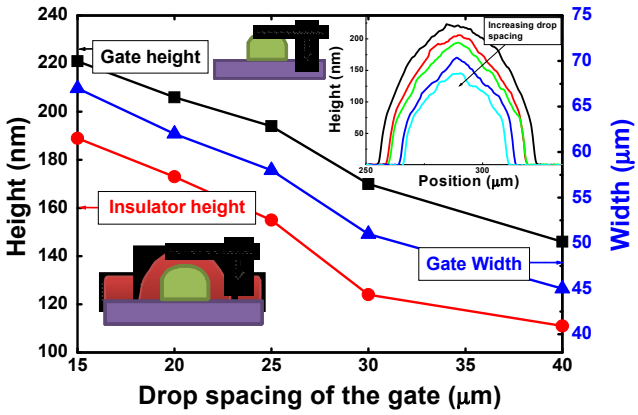

Figure 2*. The width of the silver gate line and the step height of the gate and insulator as a function of printing drop spacing. Inset shows the profilometry of the silver gate lines with varying drop spacing.*

Line surface roughness and profile can be determined by the sintering temperature as shown in Fig. 3. The ink solvent consist of water, ethanol and ethylene glycol (EG), therefore the sintering done at 150°C drives out the low boiling point solvent first and then slowly evaporates EG resulting in better surface roughness and smoother line profile. However, 200°C anneal is favorable in order to reduce the resistivity. Therefore the optimized sintering should consist of a low temperature followed by a high

temperature annealing to achieve the best conductivity and low surface roughness. The lowest surface roughness ~14nm obtained from AFM measurement as shown in the Fig. 3 is limited by the distribution of the nanoparticle size.

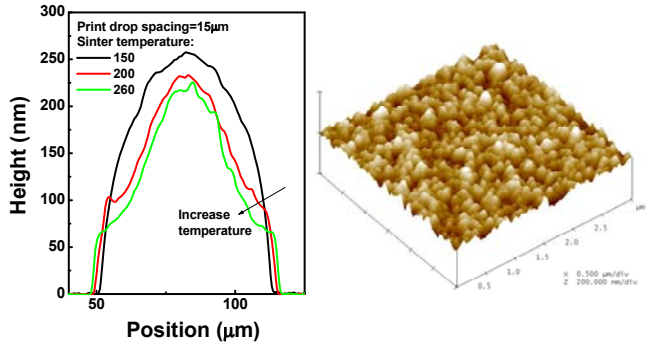

***Figure 3**. The profilometry of the printed silver line with various sintering temperature. Also shown is the AFM result of the line surface.*

B. Print layers

The printed insulator need to be conformal on the gate step height. 7.6 wt% of Poly(4-vinylphenol) (PVP) dissolved in hexanol with 0.6% by volume of cross linker poly(melamine-co-formaldehyde) was used as our insulator ink. The ink has a good wetting behavior on variety of substrate including oxide, metal and plastic. Due to the momentum of the inkjet drop landing, the ink tend to flow outward while drying and hence resulting in a big coffee ring as shown in the inset of Fig. 4. Fortunately, after the solvent dry out, the PVP are smooth and has a good conformal coverage as shown in the profilometry of Fig. 4. The average dielectric breakdown ~ 2MV/cm was consistently obtained comparable to the same material system [3]. The thickness of PVP can be scale down by increasing the drop spacing, decreasing both the printed layers and mass loading of the ink as reported in our previous work [4-5]. Here we also conclude that using more nozzles in printing improved the uniformity of the PVP layer; because the ink can dry more uniformly instead of drying from single side resulting in thicker at one side than the other as shown in Fig. 4.

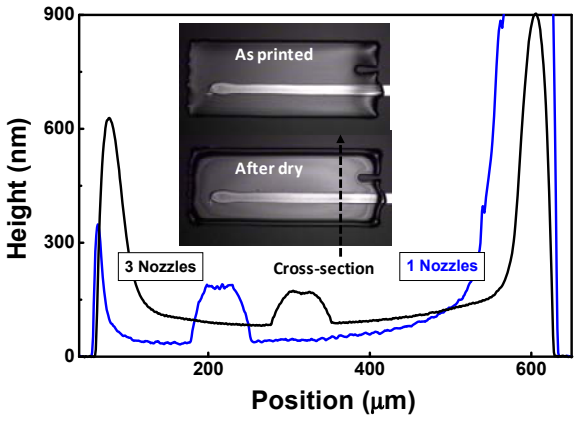

***Figure 4**. The profilemotry of the printed PVP with one and three nozzles printing simultaneously.The inset shows the optical micrograph of a printed PVP layer with three nozzles printed at the same time.*

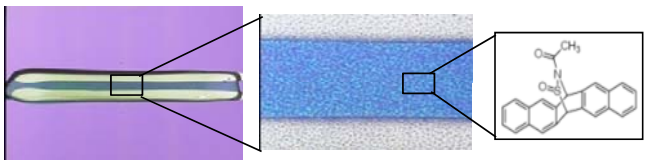

***Figure 5**. Optical microscope of the printed pentacene layer on top of printed silver source and drain.*

The printing of semiconductor layer requires a uniform coverage on the channel surface. 1.5wt% of pentacene precursor (Sigma Aldrich) dissolved in anisole was used as our semiconductor ink. Anisole was selected as the solvent due to the high boiling point of 150°C that can prevent the ink from clogging during the jetting process. Fig. 5 shows the optical micrograph of printed pentacene on the top of printed silver S/D. Low surface energy of the substrate is favorable for achieving a better molecule stacking and also cause the ink to dewet and accumulates surrounding the S/D electrodes as shown in Fig. 5 for better coverage of the channel region.

C. Surface energy manipulation

Control of substrate surface properties, especially surface energy, is critical to form precise features. Surface energy and uniformity affects the wetting of inks on substrates, and correlates to line width and line edge roughness. UV ozone and subsequent heat treatment has been demonstrated to raise and lower surface energy of a PVP dielectric film. With spun-cast PVP smoothing layer as the substrate, this module facilitates printing of narrow gate lines first followed by a series of wide and thin PVP insulator, then printing narrow feature interconnection lines again by reversing the surface energy of PVP substrate. Fig. 6 illustrates this effect by performing 10 minutes of UV ozone treatment to significantly increase hydrophobicity of the PVP, which is partially reversed following heating at 150°C for 1.5 hours. This demonstrates the feasibility of this technique as a process module to control surface energy and printed linewidth. The use of monolayer treatments to modify PVP surface energy has also been explored. Exposing PVP films to HMDS (Hexamethyldisilazane) and FOTS (Fluorinated-octyl-trichloro-silane) vapor lower the surface energy making them more hydrophobic.

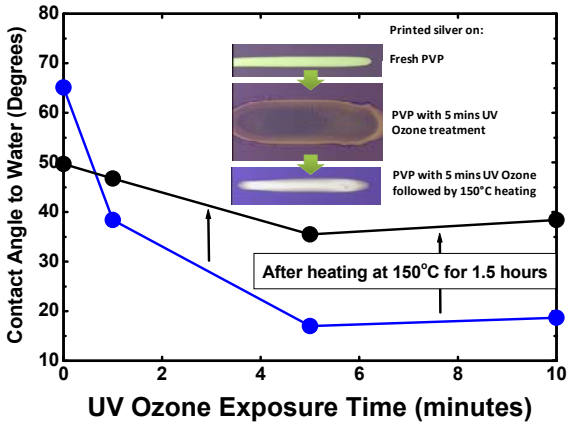

***Figure 6**. Water contact angle on PVP with various UV ozone exposure time and heating treatment. Inset shows the optical micrograph of printed silver line on PVP substrate with several treatments.*

Novel Process Modules

In this section, we demonstrate three process modules that have a significant impact on the printing circuit breakthrough.

A. Self-aligned source/drain to gate

In order to overcome the poor layer-to-layer registration capability of the printer, we recently developed a self-aligned printing to minimize the S/D to gate overlap capacitance, resulting in the enhancement of the transistor speed [6]. The self-alignment is achieved by facilitate S/D to dewet and roll-off the PVP surface. The procedure ares (1) Treat PVP with HMDS vapor to decrease its surface energy (2) 15% by volume of water was added into the silver S/D ink to increase the surface tension of the ink (3) Control the step height of PVP by controlling the printing drop spacing of the gate lines. Fig. 2 shows the same dependent of step heights on varying drop spacing for both gate and insulator due to the conformal PVP layer. Although smaller drop spacing gives a larger step height to facilitate S/D ink dewetting, the resulting larger line width and hence larger channel length is unfavorable. At too large drop spacing, the gate line edge roughness become severe and the self-alignment yield drops because of insufficient step height.

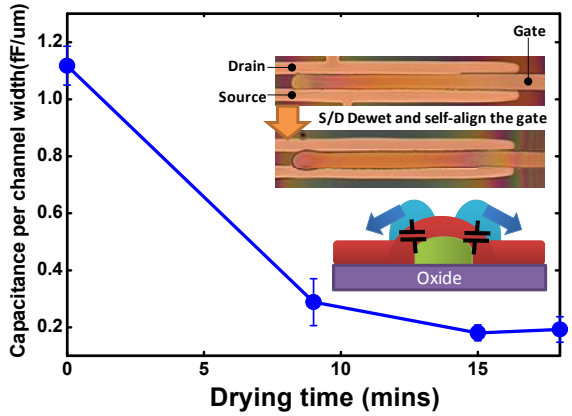

***Figure 7**. Parasitic capacitance per channel width as a function of source and drain drying time. Inset shows the optical micrograph of printed self-aligned transistors with S/D drying immediately (top) and after 15 minutes (bottom) respectively.*

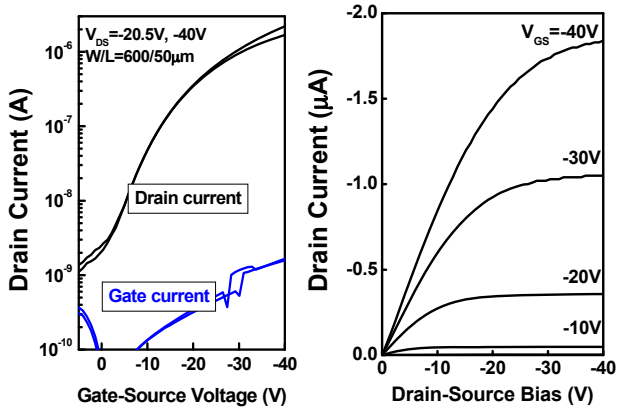

***Figure 8**. Tranfer (left) and output (right) characteristics of a printed self-aligned transistor.*

Fig. 7 shows the S/D to gate overlap capacitance per channel width as a function of drying time before sintering of silver. The overlap capacitance has been significantly reduced by an order of magnitude. The inset of Fig. 7 also shows the optical micrograph of the all printed self-aligned transistor without semiconductor layer for better clarity of the self-alignment. Fig. 8 shows the transfer and output characteristics of the all printed self-aligned transistors. The channel width and length is 600um and 50um respectively. The saturation mobility is 0.011cm^2/V-s and the on/off ratio is 1600.

B. Self-aligned interconnect

The principle of dewetting source and drain was further carried out on the printing of integrated circuits. A novel technique of self-aligned interconnect was demonstrated in this work. Fig. 9 shows the micrograph capturing the process of the self-aligned interconnection. A perpendicular silver line (black line) was printed across the three pre-printed self-aligned transistors. Driven by rheology, the silver ink not only tend to dewet the channel surface, but also preferably wets and flows toward the pre-printed S/D electrodes in the vertical direction and thus creating an extra force of line splitting. Therefore, the S/D electrode completely split while three transistors are still connected in a cascade scheme after 10 minutes. The technique demonstrates the simplicity of inkjet printing interconnects. Moreover, the yield of printed circuit can be significantly improved since the probabilities of shorting S/D by mis-alignment are entirely eliminated.

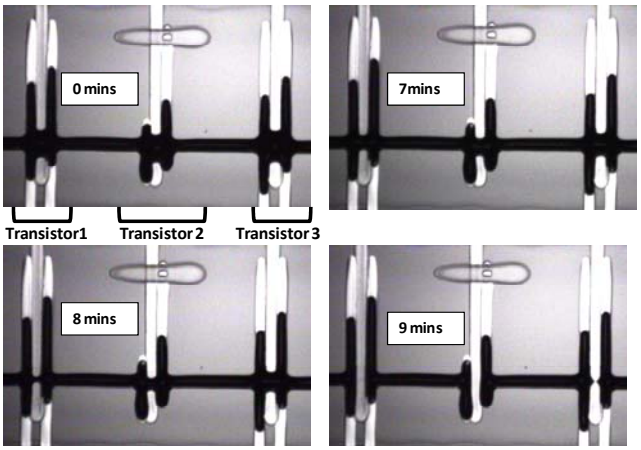

***Figure 9**. Image captured from the inkjet printer camera while the printed interconnect line was splitting.*

C. Local interconnect

In order to print an inverter, a novel local interconnect printing technique was introduced. The alcohol-based solvent of the silver ink can be used to dissolve the pre-crosslinked PVP. Therefore, the local interconnect can be accomplished by printing a second silver line to dissolve the pre-crosslinked PVP and form a contact to the first layer of silver simultaneously. Fig. 10 shows a good physical contact between the two layers of silver given a sufficient dissolve time of several minutes. Fig. 10 also shows the measured resistance of the contact chain connected between the 1st vertical silver segment and 2nd horizontal silver with the PVP layer in between. Second layer of silver was printed with three different drop spacing. With the 5um drop spacing, good contact and low resistance local interconnect can be achieved.

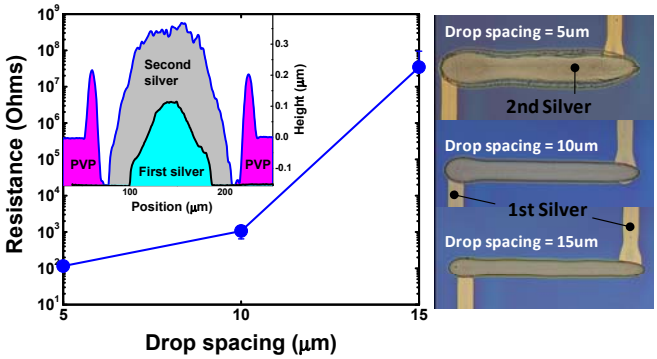

Figure 10. *The resistance of the contact chains as a function of printing drop spacing of the second silver. Inset shows the profilometry of a second printed metal dissolving the insulator and contact the first layer of silver. The optical micrograph shows the segment of the contact chains connect by two layers of silver line with PVP in between.*

Case Study – Printed Inverter Circuit

With the complete process modules, the circuit building block –inverter can be printed by a simple procedure. Fig. 11 shows the printing sequences for a inverter printing: (1) horizontal gate lines are printed first (2) vertical PVP are printed next (3) local interconnect was printed and dissolving the pre-crosslinked PVP to form contact to gate lines (4) horizontal lines for self-aligned S/D printing are performed (5) vertical line for interconnect the two transistor are printed and self-align the S/D of each transistors. Finally, semiconductor material can be printed on demand such as p-type on one transistor and n-type on the other. In this case, diode-connected transistor is used as the load transistor, therefore only p-type pentacene is required be printed or spin-cast to complete the inverter printing. The inverter shown in Fig. 11, using a ratio of W_{DRIVE}/W_{LOAD}=3 optimized from circuit simulation, is capable of producing a maximum voltage gain of 1.46 as shown in Fig. 12. The voltage gain of the inverter passed the criteria (V_{GAIN}>1) to construct a ring oscillator which is required for an asynchronous low-cost printed RFID applications.

Conclusion

Robust baseline process of printed transistors along with novel process modules were developed and demonstrated. The simple and complete process modules developed in this work have ensured the feasibility of realizing the low-cost printable integrated circuits for the RFID or sensor circuits in the future.

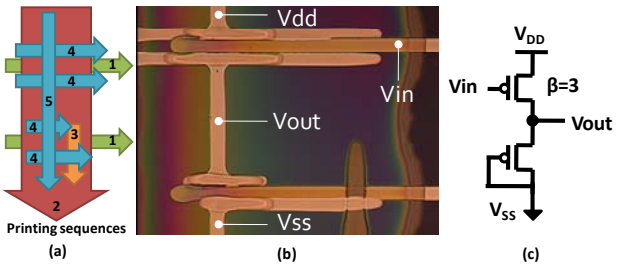

Figure 11. *(a) Printing sequences of the inverter using a self-aligned diode connected load transistor (b) Optical micrograph of the printed inverter (c) Circuit schematic of the inverter.*

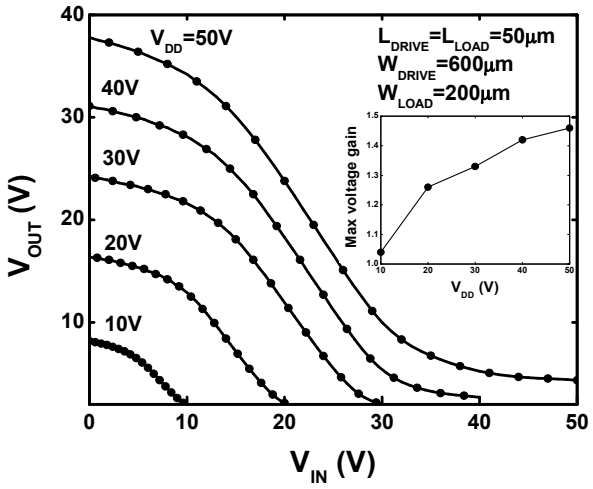

Figure 12. *Voltage transfer characteristic of the printed inverter with various V_{DD}. Inset shows the maximum voltage gain as a function of V_{DD}*

Acknowledgements

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Author Biography

Huai-Yuan Tseng received B.S. degrees in Physics from the National Ching-Hua University, Taiwan in 2000 and M.S. degree in Electronics Engineering from the National Chiao-Tung University, Taiwan in 2002 respectively. He was then recruited by Industrial Technology Research Institute as a research and develop engineer from 2002 to 2007. He is currently pursuing a Ph.D. degree in Department of Electrical Engineering and Computer Science at the University of California at Berkeley. His research interests include inkjet-printing organic transistors and modeling/simulations associated with printed integrated circuits.