Dynamic Correction of Interconnections in Printed Electronics Manufacturing

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Abstract

This paper studies the problem of automatically aligning the interconnections of integrated components in printed electronics modules. During the process, molding material is deformed and the components get displaced. Unless this is compensated on a per-module basis, the ink jetted connectors do not reach their targets. In this paper we propose a new connection redrawing method that applies a smooth displacement function to each pixel of the bitmap. Experiments show that using the new method, deformations are smoother, and the original shapes and intended electrical behavior are better preserved.

Introduction

The current trend in electronics manufacturing is increasing awareness of environmental implications of production and logistics. At the same time consumers are more demanding and looking for products to serve their needs. Further, electronics industry is investing significantly on technologies that would allow miniaturization of electronics assemblies. The key point in satisfying these needs is to have a manufacturing technology that is environmentally friendly, and allows miniaturization of electronics assemblies with high level of flexibility in demand-supply-networks. One of the most prominent new technologies satisfying these needs is *printed electronics*.

Printed electronics is an additive process and a relatively new area of research, which uses traditional printing devices for interconnecting or manufacturing components. One of the fundamental technologies is *inkjet* printing, which relies on the principles of traditional inkjets, but with special fluid materials targeted for electronics. An example of an application of this technology uses conductive nano particle and dielectric inks to create interconnection circuits between connector pads of integrated circuits (IC's) and discrete components that have been molded onto the background surface [6]. In this paper we call this concept a printed module. One such module is shown in Figure 1, where there are four IC's molded into the background. The next step in the processing would be to print the wiring shown on the right on top of the module.

One of the most significant challenges in printed modules is the accuracy of the manufacturing process. The errors in component locations are mostly due to inaccuracy in the component placement process, molding process related movement, and molding material shrinkage and bending. The latter category is typically the most significant one, and also the most unpredictable [4].

The unpredictability of the deformation of the module is the main reason why the traditional approaches [7] for printed circuit board (PCB) manufacturing are unsuitable for this problem. In PCB manufacturing the background materials are rigid, which allows only translation and rotation. In our case, the substrate may shrink or expand causing the components to move with respect to each other. In addition to the complexity of the transformation, most existing approaches concentrate on quality control instead of dynamic modification of manufacturing data of individual structures, termed as *dynamic correction* in this paper. In our case, the interconnection structure resides as an image in computer memory, which makes it easy to correct prior to printing.

In order to simplify the manufacturing, we do not assume any alignment marks at the correction stage. Instead, we align the wiring to the connectors of one IC (so-called *calibration IC*). Because the IC is rigid, this gives us the correct scale irrespectively of the image resolution. The wiring targets are always exact for this particular IC, but more and more incorrect the further we go from the calibration IC due to the compression of the back-

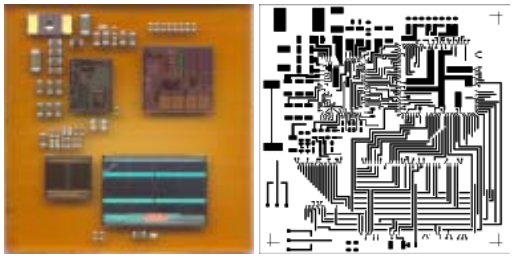


Figure 1. *A sample multi-IC module (left) ready for printing the connections (right).*

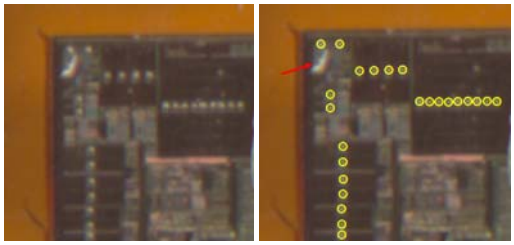


Figure 2. *Closer look at the module. The wiring targets are the golden pads near the edges of the IC. They are detected automatically by the front end, as seen on the right. Note, that the pad pointed by the red arrow is covered by dust, and can not be found by the front end.*

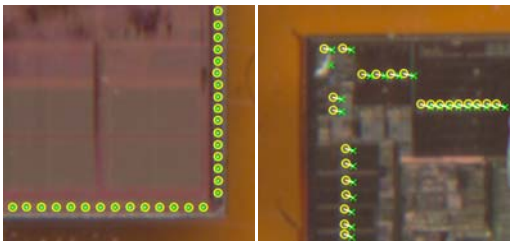


Figure 3. *Pairing the design data with the detection result. The figures show the match with the true locations of the pads. The figure on the left shows a part of the calibration IC, and the one on the right is a part of another IC.*

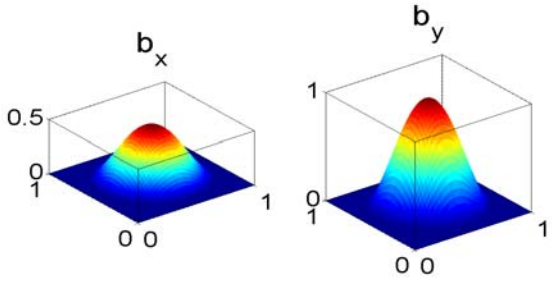


Figure 4. *An example of smooth bump created with piecewise biquadratic polynomial with* $(x,y) = (0.5,0.5)$, $\boldsymbol{\delta} = [0.5\ 1]^T$ *and* $s = 0.4$ *(and* $R = 0.45$*).*

ground material. An example of this is shown in Figure 3. It is evident that using the designed locations, the printed connection paths may end up in a wrong place. Detecting the true locations and transforming the wiring accordingly will give an accurate fit to the true situation.

In our earlier papers [2, 3], we have described a correction system that uses neural network based image analysis for locating the connectors of the IC's on the module. The correction adapts the design data in the computer memory to each individual module using a digital photograph taken from the module prior to printing. The detection result of the front end is illustrated in Figure 2. The back-end then couples the detected true locations with the intended positions as described by the design data. After coupling, the following layer is transformed to match the true locations. Earlier, we proposed to correct the difference between design data and true situation using an erase-and-redraw based method for the wire endpoints [2]. However, this tends to produce sharp edges, and is applicable only in limited cases. In this paper we propose a redrawing method that applies a smooth displacement function to each pixel of the bitmap. The function is constructed such that it translates the ends of the wires onto the true connection points, and the amount of displacement decreases radially. Experiments show that using the new method, deformations are smoother, and the original shapes and intended electrical behavior are better preserved in the studied cases.

Smooth Correction Method

The proposed method processes the data on the bitmap level and does not employ any information about the structure of the design data; for example, the wiring and the dielectric layers are treated equally. The method is based on a displacement function $\mathbf{d} : \mathbb{R}^2 \to \mathbb{R}^2$, which determines the amount of correction needed in horizontal and vertical directions for each wire point in the original image. The definition of the displacement function is based on the required displacement vectors $\boldsymbol{\delta}_1, \boldsymbol{\delta}_2, \ldots, \boldsymbol{\delta}_N$ for each connection point $(x_1,y_1),(x_2,y_2),\ldots,(x_N,y_N)$. This displacement data is obtained from the image analysis module, and a set of such data is illustrated in Figure 3.

The most obvious requirement for the displacement function is that it should translate the ends of the wires onto the true connection points. A secondary criterion is *smoothness*, which ensures that the wiring does not have sharp discontinuities that might harm the functionality of the module. The third criterion is that the correction *should have a finite support*, i.e., the correction for each connection point should take place inside a limited area. Thus, the displacement function should be defined so that it is continuous everywhere and decreases smoothly to zero when moving radially away from each connection point.

The derivation of the displacement function follows the idea of blobs [1]. Each wire end should create a smooth bump onto the displacement function. We also require that all the bumps weld together smoothly. It's also important that the heights and locations of the bump peaks don't interfere with each other, because we want the wire ends to be translated exactly to their right positions to ensure a flawless connection.

First we need to decide the model of the bump, i.e., how should the correction propagate and attenuate while moving away from a wire end. An example of a function satisfying the above requirements is the biquadratic polynomial defined as

$$\mathbf{b}_i(r) = \begin{cases} \left(\frac{r^4}{R_i^4} - \frac{2r^2}{R_i^2} + 1\right)\boldsymbol{\delta}_i, & \text{when } r < R_i, \\ \mathbf{0}, & \text{otherwise,} \end{cases}$$

where $r = \sqrt{(x-x_i)^2 + (y-y_i)^2}$ is the distance from the i^{th} wire end (x_i, y_i). Moreover, $\boldsymbol{\delta}_i = [\delta_i^{(x)}\ \delta_i^{(y)}]^T$ defines the displacement between the i^{th} wire end and its intended location and the parameter R_i is the correction radius allowed for the i^{th} connection point.

The correction radius R_i defines the area which is affected by the correction. On one hand, it should be reasonably small not to spread the deformation further than necessary. On the other hand, the radius cannot be too small or the correction may become impossible. Since the amount of required correction varies in different areas of the module, it's reasonable to make the radius adaptive and dependent on the correction distance. This can be achieved, for example, simply by setting the distance proportional to the required correction radius: $R_i = s\|\boldsymbol{\delta}_i\|$, where the constant s is so called smoothness parameter. The larger the parameter s, the larger the correction area and the smoother the correction. An example bump is shown in Figure 4.

The second step is to create the actual displacement function $\mathbf{d}$ by adding all the individual displacements together. This should be done in such a way that the bumps of closely spaced connections points do not interfere with each other. This can be achieved by introducing a weighting function w_i for each bump $\mathbf{b}_i$:

$$w_i(r) = \begin{cases} \frac{1}{2r^2R_i^2 - r^4} - \frac{1}{R_i^4}, & \text{when } r < R_i, \\ 0, & \text{otherwise.} \end{cases}$$

The weight is zero outside the correction radius R_i and goes smoothly towards infinity when approaching the bump center.

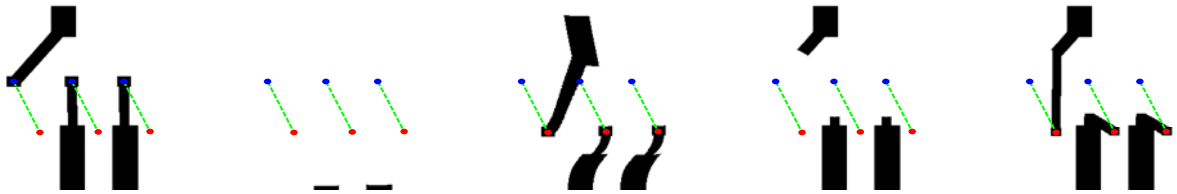


Figure 5. *Illustration of the correction process. The figure (a) shows the connection points and connectors before correction. In (b), the wire ends have been erased and in (c) redrawn using the proposed method. For comparison, Figures (d) and (e) show the erasing and redrawing phases using the old method.*

The actual displacement function is now defined as

$$\mathbf{d}(x,y) = \frac{\sum_i w_i(x,y)\mathbf{b}_i(x,y)}{\sum_i w_i(x,y)}.$$

The definition[1] is simply a weighted sum of all the bumps $\mathbf{b}_i$. The weights are needed to ensure that the effect of the neighboring bumps becomes negligible near a connection point (and that $\mathbf{d}$ is smooth on the borders of correction areas). Otherwise, the superposition of nearby bumps would make the translation too large, and the wire ends would not reach their targets. An example of a combined displacement function is shown in Figure 6.

After a displacement function has been established, the actual correction can be done. Figure 5 shows the stages of the correction. In Figure 5(a) there is the original wiring bitmap. The blue dots indicate the wire endpoints without correction, and the red dots indicate the true target locations.

The first stage of the correction — illustrated in Figure 5(b) — is to erase the falsely oriented wire ends. The erasing is limited to only those pixels that, according to the displacement function, have displacement big enough to make some difference, i.e., those that have nonzero displacement.

After all the wire ends have been erased, each erased wire pixel needs to be remapped according to the displacement function. Figure 5(c) shows the corrected wiring in the example case.

In Figure 5(d) and 5(e), the correction method is compared to our earlier method [2], which simply replaces part of the wires with straight lines so that the wire ends meet their correct location. The new method clearly creates fewer short circuits and avoids sharp corners, which may have an impact on the electric properties of the result.

Experimental Results

An example result using the new and the old method is shown in Figure 7. Figure 7(a) shows a part of the module ready for printing. However, due to component drifting, the connectors have translated, and printing the design bitmap directly will result in failed connections, see Figure 7(b). Note that this displacement cannot be corrected by translation, because that would increase the errors on other components of the module (this is the fit that minimizes the square error of the connection point locations without manipulating the bitmap).

[1]For simplicity, we have omitted two special cases when $\mathbf{d}$ is undefined: when (x,y) is one of the connection points (x_i,y_i), we should define $\mathbf{d}(x,y) = \boldsymbol{\delta}_i$, and when (x,y) is outside the radius R_i of any correction point (x_i,y_i), we should define $\mathbf{d}(x,y) = 0$.

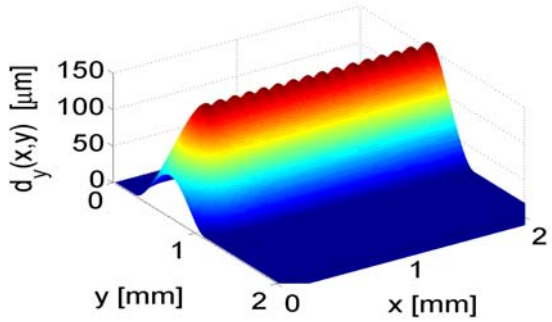
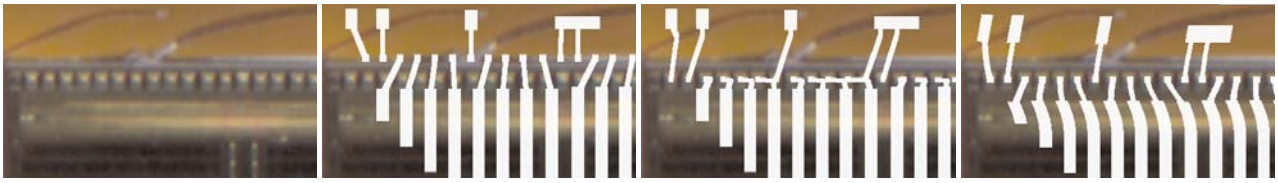


Figure 6. *A part of the displacement map used in Figure 7 (only vertical displacement shown; the horizontal direction map is similar but with negative peaks as the displacement is directed from right to left).*

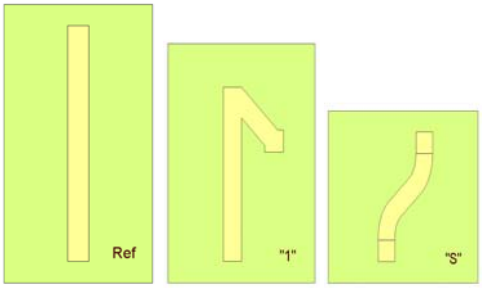
The correction results are shown on Figure 7(c) and Figure 7(d). The first one shows the result of the old erase-and-redraw method, and the second one shows the result with the smooth correction. By using the new method, there are no short circuits, the deformations are smoother, and the detailed shapes are preserved, such as the square-shaped end of each wire. Figure 6 illustrates the displacement map that was calculated in the above example. As expected, the connector pattern is clearly visible.

The electrical performance of the interconnections was verified by simulations. Three line geometries were considered (see Figure 8), a straight 550 μm line (reference), a 475 μm line including a sharp corner resulting from the erase-and-redraw algorithm ("1"), and a smooth 350 μm connection obtained with the smooth correction algorithm ("S"). The simulations were carried using CST Microwave Studio [5]. The conductivity and relative permittivity of the substrate were set to typical values for printable materials [8], $\sigma = 10^7\,S/m$ and $\varepsilon_r = 3.0$. The conductor and substrate thickness was $t = 2\,\mu m$ and $h = 5\,\mu m$, respectively. The conductor width was $W = 50\,\mu m$ resulting in 17.25 Ω line impedance. The lines were terminated to 17.25 Ω discrete ports and the attenuation between the ports was simulated. Figure 9 shows the results, which indicate that for short interconnections, the effect of line length is far more significant than the line geometry. In most practical cases the proposed smooth correction method minimizes the resulting connection length, which is therefore a key property in terms of performance. Thus, it produces the best performance in terms of conductivity for the structures analyzed. More studies are needed to analyze implications of shape to the performance and



(a) (b) (c) (d)

Figure 7. *Original module ready for printing (a), and the simulated printing result without correction (b). The simulated result with erase-and-redraw correction (c) and the result with the smooth correction (d).*



(a) (b) (c)

Figure 8. *Line geometries used in the electrical performance simulations. Original line with no component displacement (a), misalignment corrected using erase-and-redraw algorithm (b), and misalignment corrected using smooth correction algorithm (c).*

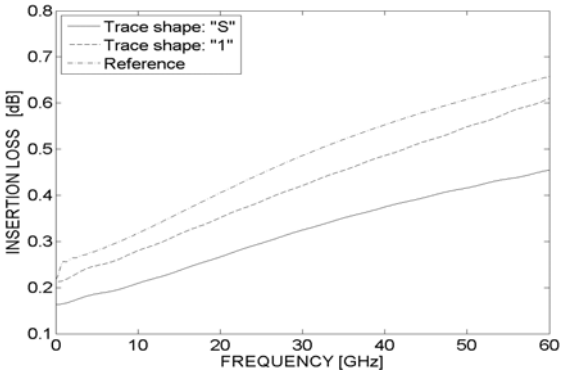


Figure 9. *Simulated insertion loss for the three different line geometries considered.*

the implications of the selected correction distance to the overall line lengths.

Conclusions

A smooth correction method for adapting printed diagrams individually for each module was proposed. The new method is based only on moving existing pixels to new locations, and therefore does not require any knowledge of the structures behind the pixels. The earlier correction method [2] assumes that the objects to be corrected are all thin wires with well defined endpoints. In practice this is not always the case, and there are various structures that the earlier method fails to correct because of this. Moreover, as the earlier method erases and redraws the wire ends, it is necessary to define the pencil used to redraw the connections.

One advantage in using a continuous displacement map defined all over the design bitmap is that the same mapping can be used to correct all printing layers in a similar manner. For example, after the wiring has been printed, the following insulator layer with vias onto the next layer can be transformed using the same displacement function as the wiring layer.

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Author Biography

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