Studies Towards the Inkjet Printed Electronics Prototype Series

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Abstract

Inkjet printed electronics enables deposition of functional materials accurately in both placement and volume. Decreased line widths and usage of conductive nanoparticle metal inks opens possibilities for electronics integration. For example, printed multilayer microstructures can be used to integrate chip scale electronic applications. At Tampere University of Technology evaluation of inkjet printed microstructures and their ability in electronics integration has been studied. The technology evaluation towards prototype and pilot series has followed a technology maturity study from subparts to whole system. The subsystem blocks of the system are first examined individually using dummy structures. Gathered data is utilized in manufacturing process to create functional integrated system. This technology evaluation study comprises of material and process research. The material study includes the initial material jetting study and material compatibility issues. Material evaluation enables the process study, which includes the study of the process to meet the structure requirement, e.g. size and performance. In addition, process parameters for application specific materials and features are defined with initial optimization in speed and quality issues.

Introduction

Inkjet printing as electronics integration method has been researched at the Tampere University of Technology, gaining attention from successfully integrating conventional components with inkjet printed functionality. Inkjet printing in principle is accurate in both placement and drop volume, being especially strong in layer-to-layer registration compared to other printing methods. The manufacturing possibilities for large scale production have been mapped through economical analyzing and process development. Architectures under research work include combinations of novel inkjet printed interconnections and conventional components, such as silicon chips and passive components. Created applications have included individual prototypes of inkjet printed System-in-Package modules. To study the series production possibilities for module concept, a set of prototypes followed by precursor production batch are manufactured utilizing the information achieved through subprocesses. The subprocess study divides the whole process flow into pieces for more detailed research work. Local phenomena can be measured and analyzed, and as a combination of these, the main processes can be formed.

The module manufacturing process utilizes additive inkjet printed electronics. Each layer is deposited on top of previous one, without need for masking or etching. Material is applied only where needed, which saves material and reduces waste during manufacturing phase. Module interconnections formed with inkjet printing utilizes typically nanoparticle metal inks and inkjettable dielectrics. [1]

Using commercial inkjet printheads that deposit nominally 12 pl drops, it is possible to achieve trace widths of 35-37 microns on a module surface. This enables fine-pitch (<100 μm) IC connections.

As said, the prototyping series of inkjet printed modules are enabled via subsystem research. In the field of electronics in general, the complexity of products is increasing and in the same time, product life cycles have shortened. This combination requires dynamic innovation and prototyping. The digital nature of inkjet printing enables quick creation of small series of prototypes.

This study emphasizes integration possibilities of inkjet printed electronics, but also comparison approach to conventional technology, wire bonding. Multilayer structure of inkjet printed traces to replace wire bonded IC interconnections has been presented [3], and process phases for novel and conventional methods are initially compared.

Inkjet printing integration possibilities

Various methods for electronics integration with inkjet printing have been presented during the last few years around the world. Inkjet deposition in electronics integration has been reported to be used typically in accurate deposition applications such as system-in-board modules.[5]

The RFID and display technologies require low voltage transistors that have been created by combining inkjet printed conductive nanoparticles, polymer dielectric and semiconductors.[6]

Laser processing enables low-temperature sintering and material ablation of nanoparticles. This combined with inkjet printing makes possible to produce multilayer passive and active electronic components on various substrates.[7]

Currently the super-fine inkjet represents the state-of-the-art inkjet printing with a drop volume of sub fl that results in <1 μm dot size on a substrate. One advantage of femtoliter drop size is that it is possible to precisely pattern designed CAD data. [8]

At Tampere University of Technology electronics integration has been demonstrated via module concept [9]. Flowchart for module manufacturing is presented in Figure 1.

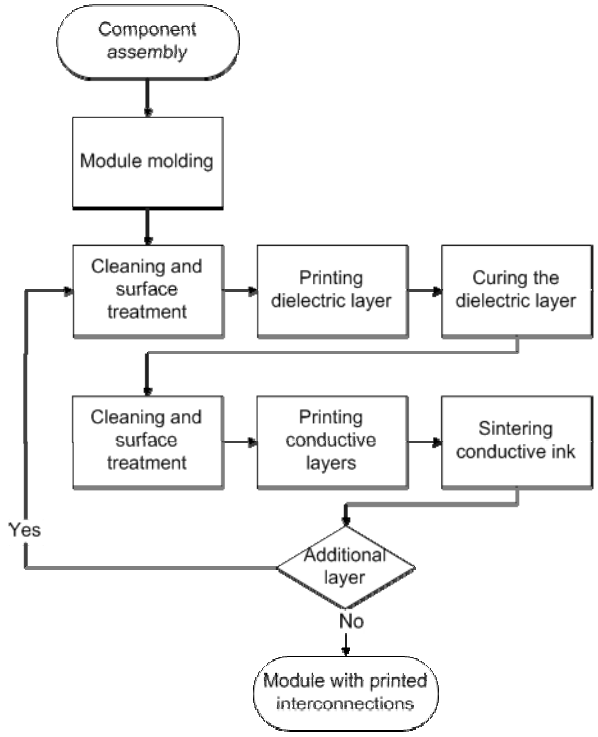

Figure 1. *Module concept manufacturing flowchart*

The module manufacturing process can be divided into subprocesses for closer research. Each subsystem uses previous process result as input and offers output for next process, respectively.

Subsystem research

The module concept can be divided into subsystems that are molding, surface cleaning and treatment, printing, and ink post-processing phases. Each process phase is individually examined and demonstrated and finally combined in the first prototype module series. The following paragraphs explain some details of the module molding to create a printable substrate, printing conductive and dielectric inks using inkjet printing, and the interaction between the printed ink and printing surface.

Module molding

In the molding phase the components are encapsulated inside an epoxy mold, leaving active sides open. This is done by assembling the components on an adhesive carrier substrate and pouring the molding material over the components. Finally, the carrier tape is removed revealing the components' electrical contacts. Figure 2 illustrates the procedure.

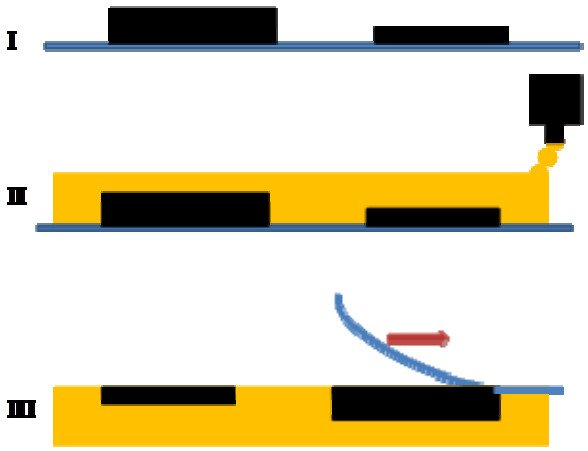

Figure 2. Molding process. I: component assembly. II: encapsulation. III: adhesive tape removal

There are both material and process related issues in the molding phase which affect the outcome of molding subprocess outcome. Material and process compatibility issues are critical to outcome quality. There are several failure mechanisms during the process. Possible defects in each process phase are presented in the Table 1.

Table 1. Possible molding process defects

Process phase	Possible defect
Component assembly	Alignment error
Encapsulation	Air traps, bubbles
Curing	Delamination, warpage

The component assembly accuracy determines the level of severity of the alignment error. The level is critical in contacting small-pitch integrated circuits and may require redesign of the inkjetted patterns to match the pad locations.

Successful encapsulation requires knowledge of material rheology in order to enable material flow between the components. Insufficient flow may result into air traps, which requires additional fill material to be inkjetted in order to level the surface or it results in rejection of the module. Bubbles or voids may result from degassing during the epoxy curing phase. This may be prevented with vacuum degassing during the curing.

Warpage issues of a molded SiP for inkjet printed interconnections have been researched and different module structures have been modeled.. Warping of the module is caused by coefficient of thermal expansion (CTE) mismatch between the molding material and the components, and may result in drop offsetting, module level interconnection error, or delamination of a component or a printed layer. Suggested actions for warpage reduction include an additional backside polymer film or a glass sheet, adjustment of the mold thickness, and controlling the post-cure cooling time.[2]

Printing

The inkjet printing process for creating interconnections for a complex SiP includes accurate deposition of two types of materials: conductive and insulating. Inkjet printable epoxy-based UV curable dielectric material is first deposited to level the molded

surface. The leveling is done due to the topography caused by IC coined bumps and passive metallization. Over the smooth dielectric layer the first conductive layer of nanoparticle silver ink is printed. However, multilayer structure is required for complex wiring, and it is formed by printing multiple cycles of dielectric and conductive materials.[9]

In the Figure 3 is presented the simplified structure of the inkjet interconnected module.

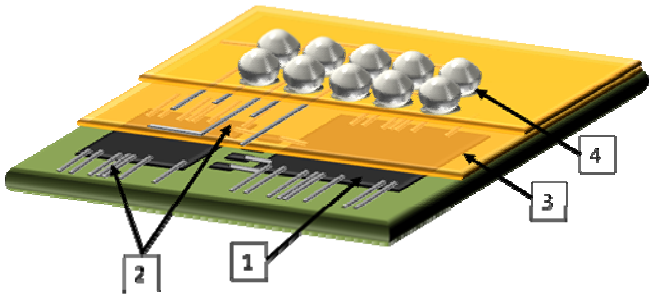

Figure 3. *Principle of the module with inkjet printed interconnections*

In the first phase, the topography caused by the molded components (1) is leveled with a printed dielectric layer. This is followed by the electrical connection of the components with a multilayer wiring circuit (2, 3). Second level interconnections (4) are formed using a method compatible with printed traces.

Material study for jettability and printability has to be done prior to final circuit design or pattern printing. The jettability research for the printed fluid is done by measuring each individual firing nozzle. The jetted fluid drop formation depends on the printhead control parameters that are presented in Table 2.

Table 2. Fluid jetting parameters

Parameter	Effect
Firing amplitude	Drop velocity
Pulse waveform	Drop velocity and size
Printhead temperature	Fluid viscosity
Meniscus vacuum	Drop velocity and shape
Substrate distance	Drop formation requirements

The parameters affect the fluid ejection from the printhead nozzle. Correct drop formation time and distance are important factors to avoid any satellite drops or incorrect drop shape on substrate. Figure 4 describes the drop formation sequence and issues that are important to the print quality.

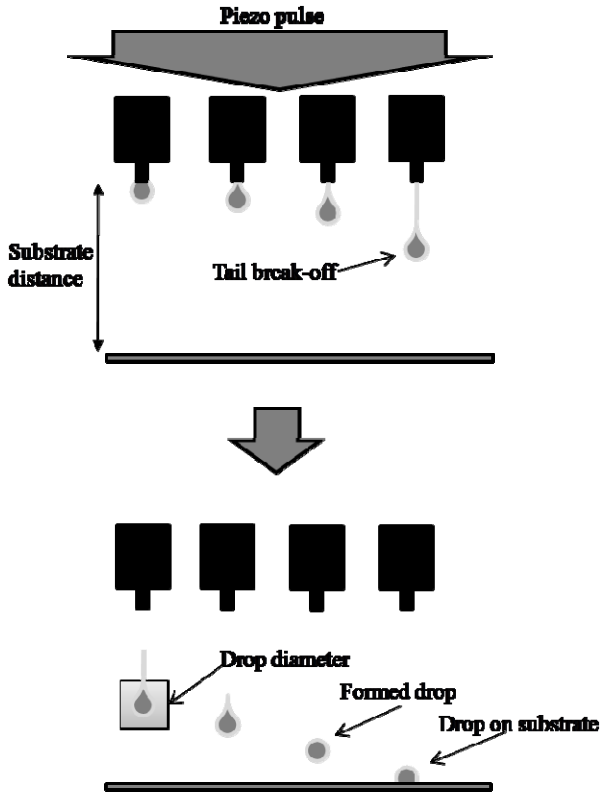

Figure 4*. Fluid ejection sequence*

Measuring drop characteristics during the flight provide information of correct settings for the process. Optimizing the droplet formation before hitting the substrate gives an advantage of wider process window and more robust process. That is, changes in printing environment do not cause defects in the printing result. The ejected drop size is nominally 12 pl, which creates drops of 58-60 µm in diameter on the module's surface that is cleaned with water-based solvent. The printing parameter effect on the drop formation are typically detected from measurements of drop diameter, formation time and distance, flight time, drop velocity, drop angle in XZ-plane and tail merge time and distance. The fluid ejection (jetting) process optimization enables further information of droplet behavior on the module's surface.

Substrate-ink interaction

Printing on a molded module substrate requires multidisciplinary approach on research work. The substrate's surface free energy and the surface tension of the liquid must be controlled in order to achieve aimed printing result. For fine conductive traces the surface energy for nanoparticle silver ink must be controlled exactly for designed drop size. Again, dielectric layer requires highly energetic surface which enables good spreading and smooth layer.

For the conductive ink, jetted droplet size on the substrate determines the used resolution and algorithm for patterning. According to the results of measured droplet behavior on a substrate, the required resolution can be calculated. Initial conductivity study of inkjet printed traces on the substrate enables

design of the electrical circuitry and trace dimensions. Since the level of conductivity of the printed conductors is not on the same level as with bulk metal, it is important to realize the maximum resistance levels for individual traces to prevent any signal distortion. That is, greater conductivity enables thinner and narrower traces, which increases the possibilities for miniaturization and integration.

The droplet behavior on the substrate can be controlled by controlling the substrate's surface energy. The surface energy is a combination of cleaning and surface treatment procedures. Depending on contamination level, the cleaning and surface treatment can be done using either physical or chemical treatment, or both. Physical cleaning includes methods such as plasma reactive ion etching (RIE) or UV-ozone treatment. Chemical treatments include usage of solvents and surface wetting agents or primers. In addition, surface energy can be modified using, for example, corona treatment or plasma. Decreasing the surface energy enables printing smaller droplets in diameter, and in that way usage of higher resolution. However, the droplet volume remains the same, and applying material at increased resolution means more material on a certain area. Without controlled deposition of adjacent drops, the fluid agglomerates on the substrate and electrical functionality is lost due to shorts and disconnections. Figure 5 shows agglomerated material caused by dispensing material without control with a high resolution and the result with a controlled process.

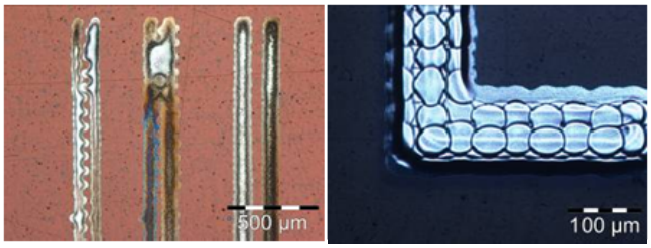

Figure 5. *Left: agglomerated silver traces printed with unsuitable process. Right: Trace printed with controlled deposition.*

The agglomeration may be prevented by using divided printfiles and printing those with a suitable algorithm. Using elevated temperatures on the stage and printing adjacent drops after drying time enables solvent to evaporate from the drops and results in fine print quality.

In order to achieve wanted characteristics for the conductive and dielectric layers, post processing is needed. Process bottlenecks are typically long ink sintering times, and process optimization is needed, as well as material development. Nanoparticle inks have enabled significantly decreased sintering temperatures, but still 200°C – 240°C is needed for 30 – 60 minutes to achieve sufficient conductivity values. Sintering profile and temperature optimization is one issue, but alternative methods for energy absorption in printed traces, such as laser sintering have been studied [4].

Results

The local blocks to enhance the quality of printed module interconnections are investigated as subsystems for the whole SiP device presented in the Figure 6.

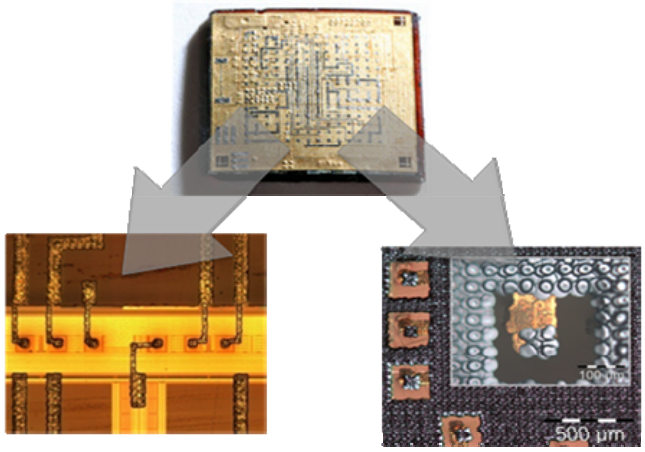

Figure 6. *System-in-Package device. Bottom left: IC-connections. Bottom right: Vias between conductive layers.*

The subsystem results can be combined and applied to the manufacturing flow. Combining the process development with statistical quality tools, the work is standardized and efficiently examined. Finally the prototype series is manufactured with optimized parameters achieved.

Interpretation

Today wire bonding is still the most commonly used technology in microelectronics mainly due to its extensive infrastructure and flexibility. In addition to a first level package connections, wire bonding can also be used to connect a chip directly to the second level package, printed circuit board. Sophisticated automated wire bonding equipments have enabled continuous process improvement with wire bonding, which has resulted in the popularity of it [10]. Inkjet printing challenging wire bonding as interconnection method has its greatest challenges in replacing the infrastructure. The general process flow of wire bonding is presented in figure 7.

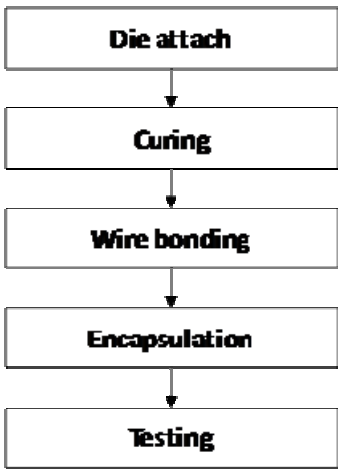

Figure 7. *Wire bonding high-level process map*

In principle, the bare die is first attached reverse-sided on the substrate using solder or adhesive. During the bonding phase, the wire is welded using either thermocompression, ultrasonic, or thermosonic bonding. Wire bonded structure is then encapsulated and tested for possible errors. However, testing can be done initially after the bonding, since once encapsulated, rework is not possible [11]. In comparison to inkjet printed interconnections, the die encapsulation is done in the beginning, leaving the active side open. Since the wiring structure is planar, need for protective structures after connecting is smaller, but can be done with thicker passivating dielectric layer. After attaching the module for the 2nd level interconnections, it can be encapsulated for an additional protection.

In the wire bonding, each bond is separately formed, that is, the operation can be characterized as single-point-unit operation [12]. Obvious disadvantage of this is that increasing the chip's I/O count increases also the throughput time of the process [10]. Inkjet printing process throughput time is dependent on the process phase durations and system complexity. The less area for interconnections and the more I/O's in the chips, the more printed layers are needed. Each layer has sintering and curing process phases, thus increasing the throughput time. Still, the yield of printed interconnections is under research work. Wire bonding is a mature and a high yield interconnection technology and it has an extensive infrastructure, therefore a replacing technology must have strong arguments. Still, inkjet printing is a promising technology, enabling alternative interconnection technology even now, being still in development phase.

Conclusion

Knowing the inkjet printing process to the core is essential in order to understand the phenomena behind the results. Module concept manufacturing process can be divided into individual subprocesses to find out the local effects of each process phase. Once found and understood the optimization of the parameters can be started, however careful experimental design and statistical analysis of the results are needed to complete the work. The knowledge gathered in the study can be used broadly in printed electronic applications in addition to the demonstrated module concept. Information on specific materials is gained, but above all, knowhow of inkjet printing process development is increased by methods, measuring systems, and analysis.

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Reference

[1] Mäntysalo, M., Mansikkamäki, P. "Inkjet-Deposited Interconnections for Electronic Packaging" Proc. of the Digital Fabrication 2007, Anchorage, Alaska, USA, 2007.

[2] Kaija, K., Pekkanen, V., Mäntysalo, M., Mansikkamäki, P. 2007 "Controlling Warpage of Molded Package for Inkjet Manufacturing" Microelectronic Engineering, volume 85, issue 5, March 2008, pp. 518-526. Elsevier Science Ltd., Oxford, UK.

[3] Pekkanen, V., Mäntysalo, M., Miettinen, J., Mansikkamäki, P. "Novel Packaging Technology for Combo Memory Package" Proc. of the 16th European Microelectronics and Packaging Conference, Oulu, Finland, 2007.

[4] Pekkanen, J., Heino, M., Mansikkamäki, P., Mäntysalo, M., Rönkkä, R. "Laser Sintering of Ag Nano Paste for Printed Electronics" Nanotech Northern Europe, Helsinki, Finland, 2007

[5] Imai, H., Mizuno, S., Makabe, A., Sakurada, K., Wada, K. "Application of Inkjet Printing Technology to Electro Packaging" Proc. of the 39th International Symposium on Microelectronics (IMAPS), pp. 484-490, 2006

[6] Molesa, S.E., de la Fuente, A., Chang, P.C., Subramanian, V. "Low-voltage inkjetted organic transistors for printed RFID and display applications" 2005 International Electron Device Meeting Technical Digest, pp. 109-112, 2005

[7] Ko, S.H., Chung, J., Pan, H., Grigoropoulos, C.P., Poulikakos, D. "Fabrication of multilayer passive and active components on polymer using inkjet and low temperature laser processing" Sensors and Actuators A: Phys. 134, pp. 161–168, 2007, Elsevier.

[8] Murata, K. "Direct Fabrication of Super-Fine Wiring and Bumping by Using Inkjet Process" Polytronic 2007 - 6th International Conference on Polymers and Adhesives in Microelectronics and Photonics, 2007

[9] Miettinen, J., Pekkanen, V., Kaija, K., Mansikkamäki, P., Mäntysalo, J., Mäntysalo, M., Niittynen, J., Pekkanen, J., Saviauk, T., Rönkkä, R. "Issues in Inkjet Printed System-in-Package Design and Manufacturing" Microelectronics Journal, In Press, Corrected Proof, Available online 2 April 2008

[10] Totta, P. A., Khadpe, S., Koopman, N. G., Reiley, T. C. and Sheaffer, M. J. "Chip-to-Package Interconnections", In Tummala, R. R., Rymaszewski, E. J. and Klopfenstein, A. G. (edit.) Microelectronics Packaging Handbook Semiconductor Packaging Part II, USA, Chapman & Hall, pp. 129-283, 1997

[11] Lau, J. H. (1994), "A Brief Introduction to Wire Bonding, Tape Automated Bonding, and Flip Chip on Board for Multichip Module Applications", In Lau, J. H. (edit.) Chip on Board Tehcnologies for

Multichip Modules, New York, USA, Van Nostrand Reinhold, pp. 1-100

[12] Elenius, P. and Levine, L. (2000), "Comparing Flip-Chip and Wire Bond Interconnection Technologies", Chip Scale Review, July/August 2000, pp. 81-87

Author Biography

Mr. Ville Pekkanen earned his M.Sc. degree in electronic engineering from Tampere University of Technology, Finland. He joined the printable electronics research group at the Department of Electronics in March 2006 and since then he has been working as researcher and candidate for Ph.D. degree. His background is on hardware design and electronics miniaturization combined with system integration. Lately his focus area has been inkjet technology in electronics integration, system integration, and production.