Inkjet Method for Forming Openings to Buried Semiconductor Layers of Silicon Solar Cells

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Abstract

An inkjet printing method for forming openings to buried semiconductor layers of silicon solar cells is described. The method uses an overlying resist as a sacrificial layer onto which a plasticiser for the resist polymer is deposited in a programmed pattern using inkjet printing. At the locations where the plasticiser is printed, the resist becomes permeable to aqueous etching solutions making it possible to form openings in underlying dielectric or silicon layer(s). The formed openings can be used to create metal contacts to the buried silicon layers of the solar cell. The increased permeability can be reversed thus enabling a single resist layer to be used to form more than one set of openings. Existing masking methods, used in solar cell fabrication, form openings in the resist layer and therefore are not well-suited to cell designs requiring more than one set of metal contacting patterns for different silicon layers.

Introduction

In order to make solar power a viable alternative to established energy sources such as fossil fuel and nuclear power, it is necessary to reduce the manufacturing cost of solar cells. This has been achieved to some extent in thin film devices by use of large area devices which require small quantities of silicon. However, the efficiencies obtained for such devices are significantly lower than those obtained for silicon-wafer-based solar cell devices.

Consequently, most solar cell devices currently commercially produced are based on silicon wafer technology which has been refined to achieve commercial efficiencies in the order of 16-18% (e.g., [1]). In general, this technology involves appropriately doping silicon wafers to form p-n junctions for carrier collection; passivating the wafer surfaces with a silicon dioxide or silicon nitride dielectric layer; and then forming metal contacts to each of the p-type and n-type surfaces. Higher efficiencies, for example 24.7% [2] have been achieved for silicon wafer solar cells where photolithography has been used to create patterned metal contacts through a dielectric on silicon surface. Lasers can also be used to scribe through dielectrics to create buried metal contacts. However, semiconductor device fabrication methods, such as photolithography and laser grooving, require costly equipment, expensive clean room environments, and generally many time-consuming steps. While high efficiencies can be achieved for solar cells that use photolithographic processes, a disadvantage of this patterning method is that if a number of different metal contact patterns are required, then the entire photolithographic process must be repeated for each pattern.

There is potential for high efficiency solar cell structures to be realised in commercial production by replacing expensive photolithographic masking steps with inkjet printing. The method of forming openings to buried semiconductor layers, which is presented in this paper, can be used to form patterns of buried metal contacts to both the p-type and n-type silicon of a solar cell. It uses inkjet deposition of a resin plasticiser to form regions in a resist layer which are permeable to aqueous etching solutions. Plasticisers are small, non-volatile molecules that can push their way between the polymer chains, setting the chains apart from one another and thus allowing the polymer to become more mobile and elastic. Unlike existing inkjet methods of patterning a resist layer where an opening is formed in the resist layer [3,4], the regions of permeability in the resist can be reversed, thus enabling a single resist layer to be used to etch more than one set of patterns in the underlying layer(s). This low-cost method may also be applied more generally to the formation of patterns of openings in buried layers of semiconductor or micro-electro-mechanical devices.

The method of forming openings has been developed to enable the formation of metal contacts to a new generation of rear-surface buried-contact silicon solar cells [5,6]. Unlike the current commercial buried-contact cells [7] where the buried contacts are located on the front (sun) side of the cell, the new design has the front surface free of metal contacts with the rear surface containing buried contacts to both the p- and n-type silicon as shown in **Figure 1**. Advantages of having both polarities contact on the rear side of the device include: (i) zero shading on the front illuminated surface which increases device current; (ii) thinner device design which cuts material cost; and (iii) potential for simpler cell interconnection lowering overall cost in module production.

In order to realise the design depicted in **Figure 1**, openings must be formed in the rear dielectric layer to expose the silicon surface for n-type metal contacts. Further etching of these openings is required to expose the deeper p-type silicon for metal contacts. The n-type silicon is contacted by an array of hole openings, whereas the p-type silicon is contacted by a series of groove openings arranged as depicted in **Figure 2**. After the openings have been formed and appropriately etched, metal (e.g., aluminum) can be deposited over the entire rear side of the cell, thus simultaneously forming electrical contacts of both polarities to the cell. The p-type groove contacts are isolated from the n-type contacts because the metal deposits only at the base of the grooves as shown in **Figure 1**.

Although **Figure 1** depicts a planar silicon surface, most commercial silicon cells have textured silicon surfaces to increase trapping of incoming light to the device. This texturing is typically achieved by chemically etching the silicon surface using an anisotropic etch resulting in a surface comprising random distributed upright pyramids. The developed method of forming openings to buried layers can be used with both planar and textured silicon surfaces.

In this paper we present the results of experiments, using polished planar wafers, which demonstrate the ability to create patterned openings for n- and p-type silicon contacts using a single resist layer. By controlling the permeability of the resist layer, n-type holes were formed in the dielectric layer and then protected from the subsequent silicon etching required to form the p-type grooves.

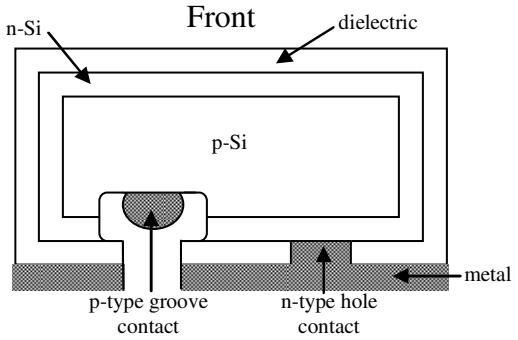

***Figure 1**. Rear-side buried contact solar cell design for which the method of forming openings has been developed.*

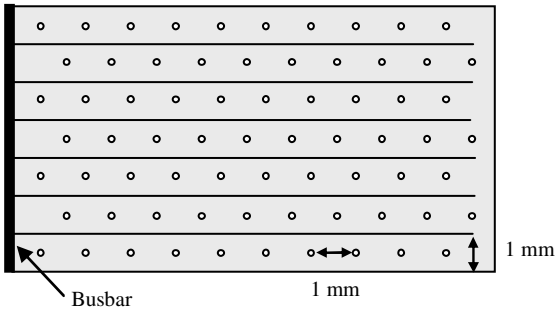

***Figure 2**. Rear contact arrangement of holes and grooves (adapted from [6]).*

Experimental

Wafer Preparation

A silicon dioxide layer of thickness ~ 300 nm was thermally grown on both surfaces of polished p-type wafers. The oxide layer serves both to passivate the silicon and form a rudimentary antireflection coating for the final cell (when thinned down to ~ 110 nm). Alternatively, silicon nitride can also be used deposited by plasma enhanced chemical vapor deposition (PECVD). A layer of Microposit FSC-M surface coating (Rohm & Haas), comprising 34% (w/v) novolac resin in propylene glycol monomethyl ether acetate (PGMEA), was spin-coated onto the rear-side surface, and then baked at 140 ºC for 10 minutes, to form a resist layer approximately 1.9 µm thick.

N-type Openings

We used diethylene glycol (DEG) as a plasticiser for the Microposit resin, though other polyethylene glycols can also be used. Drops of DEG (Sigma-Aldrich) were deposited onto the resist-coated wafers according to a "hole" pattern (substantially as shown in **Figure 2**) using a Dimatix Materials Printer [DMP] using a 1 pL cartridge. The solution in the cartridge was heated to 45 ºC in order to achieve the viscosity (~10 cP) and surface tension (~35 mN/m) required for optimal printing. The platen was heated to 60 ºC to facilitate diffusion of the DEG into the resist on contact.

A deposited droplet results in a swollen plasticised region in the resist. An AFM profile and cross-section when 8 pL of DEG was deposited on a resist layer 3.2 µm thick, is shown in **Figure 3** and **Figure 4**, respectively. Similar swollen regions were also formed with thinner resist layers.

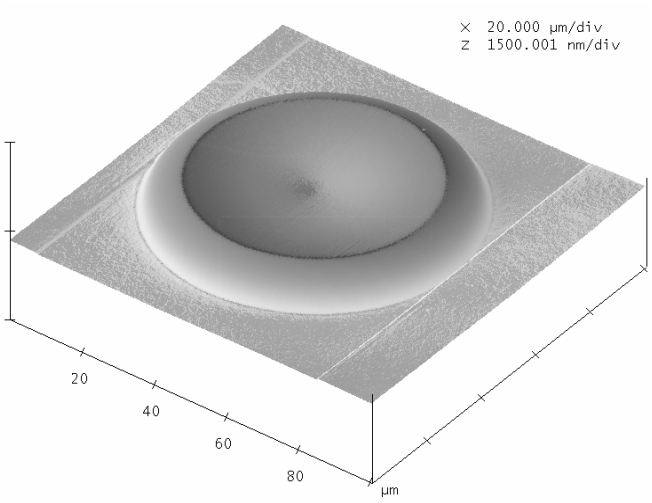

***Figure 3**. An AFM image of the surface of a plasticised resist region formed as a result of depositing an 8 pL droplet of DEG plasticiser solution on a resist-coated polished wafer. Such plasticised regions result in holes ~70 µm in diameter after etching.*

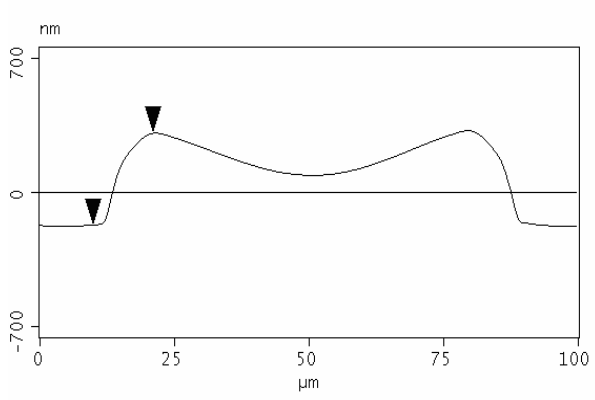

***Figure 4**. A cross-section of the AFM surface shown in **Figure 3**.*

The volume of DEG required to be deposited depends on the resist thickness, with less DEG being required for thinner resist layers. However if the resist is too thin then it cannot withstand the corrosive chemicals used for the subsequent etching processes. The final etched hole size depends on a number of factors including (i) contact angle of the deposited drop; (ii) the droplet volume; and (iii) the resist thickness. We found that etched holes ~ 40 µm in diameter formed reliably when 3 pL of DEG was deposited (as 3 layers of 1 pL drops) onto a resist layer of ~ 1.9 µm thickness.

When printing on polished or planar wafers, we found that the volume of DEG required to sufficiently plasticise a region of resist could be reduced by immersing the printed wafer in de-

ionised water for at least 5 minutes before commencing the etching process. Textured wafers require a smaller volume of DEG to be deposited, presumably because the DEG can become concentrated in the regions at the base of the pyramids.

After depositing the DEG, holes in the underlying layer were then etched through the permeable regions in the resist by immersing the wafers in 7:1 buffered oxide etch (BOE; [8]) for 10 minutes. This etch is used in preference to hydrofluoric acid because it does not damage the resist layer. The wafers were then rinsed and dried for the next patterning step. After etching, cracks appear in the permeable resist regions as shown in **Figure 5**.

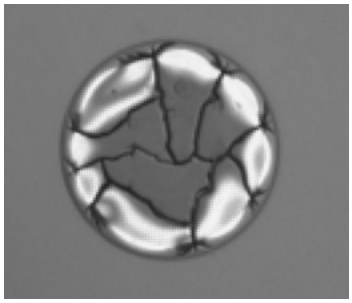

***Figure 5**. A plasticised region of resist after the wafer had been subjected to a 7:1 buffered oxide etch for 10 minutes.*

Reversing Resist Permeability

The resist's permeability to aqueous etching solutions at the locations above the etched holes can be reversed in a number of different ways. The method used depends on the subsequent processing required. If it is not necessary to form any more openings using the resist layer, the permeability of the permeable regions can be reversed by "hard baking" the wafer substrate at a temperature of at least 200 ºC for 10 minutes. After hard baking, formation of further openings by DEG deposition is unreliable (i.e., some openings do not form).

If the resist is required for further patterning of the underlying layers then it is necessary to locally reverse the permeability with out affecting the resist properties on the rest of the surface. This was achieved by depositing a solution, comprising the resist resin diluted in PGMEA [17% (w/v) solids], over the locations of the formed holes on the wafer surface. The resist solution was deposited using the DMP printer using a 10 pL cartridge on a platen which was heated to 60 ºC. It is important to note the alignment required for this printing can be relaxed as larger and more droplets can be deposited over the current permeable hole regions. Some of the holes were deliberately left un-covered to act as a control. The wafer was then heated at 100 °C for 10 minutes after printing to ensure (i) good flow of the resist into the cracked regions of the permeable regions; and (ii) evaporation of the additional solvent.

Although other baking regimes can also reverse the permeability, the above resist-cover method was employed in order to provide extra protection to the previously formed holes for the subsequent silicon etching step required to form the p-type grooves. Silicon etching solutions (as will be described later) contain very corrosive chemicals that will, with long etch times, also damage the resist layer.

P-type Openings

The p-type "groove" openings were then patterned by depositing 2 layers of 1 pL droplets of DEG spaced 25 µm apart, using printing conditions as described for the holes. The deposited droplets coalesced to form permeable linear regions ~ 60 µm in width.

The grooves were formed by first etching the silicon dioxide layer using a BOE as described above for holes, and then immersing the wafer substrate in a Trilogy isotropic silicon etch [8] for 25 min. It is necessary to etch sufficient silicon to expose the p-type silicon (which can be as deep as 4 µm into the silicon if the overlying n-Si layer, from **Figure 1**, is heavily diffused) at the base of the groove. An isotropic etch etches the silicon under the oxide dielectric layer resulting in a structure with overhanging edges. This overhang can be exploited during the metallisation process, because the metal deposited in the groove will not contact the n-type silicon thus isolating the p-type contacts from the n-type contacts.

Resist Removal & Metallisation

After both sets of openings had been formed, the resist was removed using a 'piranha etch' (a 3:1 solution by volume of 98% sulphuric acid and 30% hydrogen peroxide). The profiles of both sets of openings were checked using a Dektak. Next a thin layer of aluminum (~ 0.5 µm) was deposited by thermal evaporation on both surfaces of the processed wafer and the cross-sections of the openings were examined using focused-ion-beam (FIB) microscopy.

Results and Discussion

The depths of the n-type holes, which had been protected by reversing the permeability of the resist, were measured by Dektak, to be ~ 300 nm (see **Figure 6**). This depth, being the approximate thickness of the grown oxide layer, indicated that the holes had indeed been protected from the action of the silicon etch.

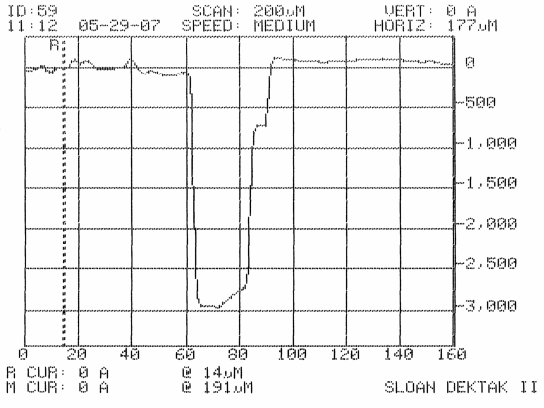

***Figure 6**. Dektak profile of a hole which had been etched under a permeable region of resist and then protected by printing resist over the permeable regions and then heating the wafer at 100 ºC for 10 minutes.*

The FIB image in **Figure 7** confirms that very little, if any, etching of silicon has occurred in these protected holes. The deposited aluminum is reasonably continuous over the hole,

however, in practice, a thicker metal layer would typically be used to ensure reliable electrical contact between the n-type silicon exposed at the base of the openings and the surface metal. The thickness of the silicon dioxide layer was estimated from the FIB image to be ~ 300 nm.

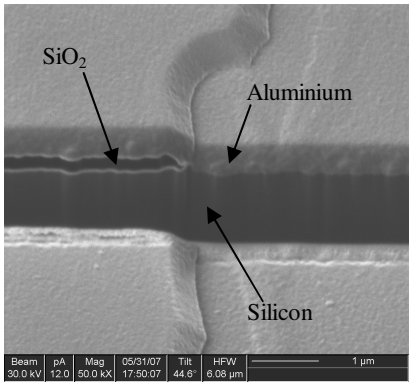

***Figure 7**. FIB image of the edge of a protected hole.*

Holes that had not been protected (explained before as control) were found to be approximately 2.5 µm deep (not shown in diagrams). The findings imply that significant etching of the exposed silicon had occurred. The grooves were etched to a depth of ~ 4.4 µm, which is deep enough to contact the p-type silicon through even a very heavily diffused layer. **Figure 8** is an FIB image showing the cross-section of one of these etched grooves. It demonstrates how the overhang, created by the isotropic silicon etch, has been effective in electrically isolating the aluminum deposited at the bottom of the groove from that on the surface (which will contact the holes).

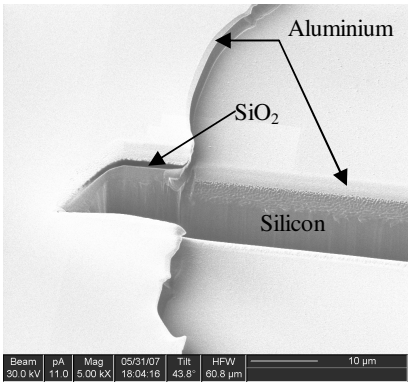

***Figure 8**. FIB image showing the overhang created by the isotropic etching of the silicon under the silicon dioxide layer.*

Conclusions

Currently commercial silicon solar cell efficiencies are significantly lower than efficiency values obtained in laboratories. This is largely because of the high cost of implementing photolithographic and laser patterning methods for metal contacts. Inkjet printing may enable higher efficiencies to be achieved in practical commercial environments.

The method of forming openings in buried semiconductor layers, described in this paper, uses low-cost inkjet printing techniques to pattern silicon solar cell layers for the purpose of buried metal contacts. It also allows a single resist layer to be used for multiple patterning steps thus providing real cost savings for a production environment. Future work will include (i) developing alternative methods of reversing the permeability of resist layers; (ii) further characterising openings formed on textured wafers; and (iii) developing silicon solar cell structures using the described patterning method.

Acknowledgements

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