Maskless Patterning of Low-Temperature High-Mobility ZnO

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Abstract

ZnO is a material that has gained a great deal of interest in the low-temperature fabrication of high-mobility transistors. For rapid prototyping of device structures, as well as cycle time reduction for investigations of processing/geometry interactions, a maskless process with high spatial accuracy is desired. High-mobility ZnO transistors were fabricated on glass using a laser-thermal-based maskless patterning process to generate working circuits. All deposition temperatures were below 200 °C, allowing this process to be compatible with polymeric supports. A variety of circuits using 5 μm design rules and various channel width and length dimensions (w/l) were fabricated and analyzed. The circuits demonstrated included ring oscillators and logic circuits, such as an exclusive OR made from NANDs and NORs. The ring oscillator frequency was demonstrated to be about 20 kHz at 20 V. An active-matrix backplane was fabricated and used to drive an OLED device. The operating characteristics of the transistors, circuits, and processes were found to be interrelated and need to be co-optimized for the best performance.

Introduction

Silicon has been the mainstay of the electronics industry for more than 40 years. Single-crystal silicon possesses properties that are difficult to compete with; its high mobility allows fast circuits as well as electronic stability. Also, given that few etches attack silicon, it is relatively simple to selectively process it. The largest drawback is that it requires high temperatures and a seeded growth.

For many devices a lower mobility is acceptable. The use of amorphous silicon has increased phenomenally with the rise of Liquid Crystal Displays (LCD). LCDs require only modest currents and therefore lower mobility is acceptable. Amorphous silicon has a mobility of only about 1 $cm^2\ V^{-1}\ S^{-1}$, which makes it marginal for driving organic light-emitting diodes (OLED), which need more current than LCDs [1]. Amorphous silicon suffers from device instability under drive conditions, which can lead to image sticking problems [2]. Amorphous silicon also requires moderate deposition temperatures, making it barely compatible with flexible organic supports.

Polycrystalline silicon enjoys relatively high mobility, but high temperatures are required and nonuniformities can result if heated locally by a process such as laser conversion from amorphous silicon. It has the advantage of making CMOS possible. It is usually converted from amorphous silicon and hence the deposition temperature is high for many organic supports.

There is a drive to make displays that are flexible and emissive. OLEDs are the natural emissive element as they are coatable and relatively efficient. The problems with silicon are that drive electronics engender a desire for a different semiconductor. Numerous semiconductors and processes are being investigated. Zinc oxide is a very promising semiconductor that is nontoxic, transparent in the visible, and can have high mobility. Numerous investigators are studying its properties [3−5].

As the problems with the semiconductor are overcome, the patterning processes become an issue. Conventional photolithography works well on a rigid support but flexible supports tend to stretch nonuniformly. This provides a challenge for optical exposure through a mask. As the size of the substrate increases the relative effect is magnified and becomes very difficult for standard processes.

One approach is to use a patterning process that can incorporate local image feedback to allow precise positioning based on the pattern already in place on the substrate. Laser patterning is a process that has both a fine resolution as well as the ability to respond to local changes in the substrate pattern [6]. Laser patterning is also extremely useful for research prototyping. All masks are digital, allowing rapid modifications of a design and saving the mask costs.

Here we present data incorporating both a zinc oxide semiconductor and laser patterning processes to achieve working devices. The laser patterning process used in this paper is a thermal process using low-cost infrared lasers. Thermal infrared processes have an extra benefit that the materials are typically not sensitive to ambient visible light.

Experimental

The key technology for laser patterning resides in the exposure print head. The print head used in Kodak's system incorporates a spatial light modulator to vary the intensity of up to 256 channels or beams [7]. The laser is a 40-watt IR diode laser with a wavelength in the 800−850 nm range. The optics after the spatial light modulator generates a linear spatial beam with a channel spacing of about 5 μm. The channels generated are square in the linear beam direction and have a Gaussian profile perpendicular to the channel array direction.

The 2.5-inch-square substrate is transported in a fast scan direction perpendicular to the channel array direction to generate an image swath. The sample is then translated in a slow scan direction one swath width and then the process is repeated. Swath registration can be on the order of a couple of micrometers, and therefore images typically have all critical dimensions, such as transistor channels lengths, within a single swath.

The materials used to pattern are two-fold. The first is an ablation resist consisting of a solution of polycyanoacrylate in a solution of 1:1 acetonitrile:cyclopentanone and an organic IR dye for absorption. The solution is spin coated to form a film. This film absorbs the energy by the IR dye absorption, causing thermal heating that dissociates the polycyanoacrylate to monomer. The monomer vaporizes and leaves a hole. There is typically a slight amount of nonvaporized polymer left in the holes. A brief O_2 plasma is used to remove this residue.

Figure 1 shows an image of a patterned molybdenum surface using this technique.

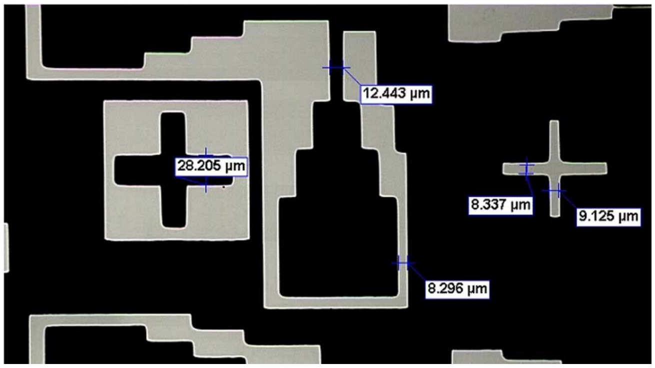

Figure 1. *Image of a laser-patterned resist surface*

The second method utilizes a thermal Novolak-based polymer resist developed by Kodak. This material acts similarly to a photochemical resist in that when exposed to thermal energy by absorption of IR light, a latent image is generated. This latent image is developable with a basic developer. It is a positive resist, being removed where exposed.

Liftoff was accomplished by coating with Shipley Microposit 1805 photoresist, sputter coating with molybdenum, and then spin coating with polycyanoacrylate with IR dye. Exposure with the IR laser removed only the polycyanoacrylate, which was then used as a mask for SF_6 plasma etching to remove the molybdenum. Finally, an oxygen plasma removed the photoresist using the molybdenum as a mask. The plasma undercuts the molybdenum generating the necessary overhangs for liftoff. The desired material was then evaporated or sputtered and the photoresist removed with acetone.

A simpler process involving the thermal Novolak-based resin was also used for liftoff but yields similar results.

The semiconductor and insulator layers of ZnO and Al_2O_3, respectively, were deposited by an atmospheric process developed at Eastman Kodak Company [8]. The aluminum oxide was deposited at atmospheric pressure from trimethyl aluminum and water vapor using a substrate temperature of 200 °C. Similarly the ZnO was deposited using diethyl zinc and water at 200 °C. The general process steps used to generate circuits are presented in Figure 2.

Transistor Characteristics

Patterned transistors are of the bottom gate variety. Molybdenum was used as the gate metal. A 110 nm layer of aluminum oxide is the insulator followed by 20 nm of zinc oxide intrinsic semiconductor. The drain-source contact metal is aluminum. A cross-sectional view of the transistor is shown in Figure 3.

A typical channel length is about 10 µm. A picture of a typical transistor is shown in Figure 4.

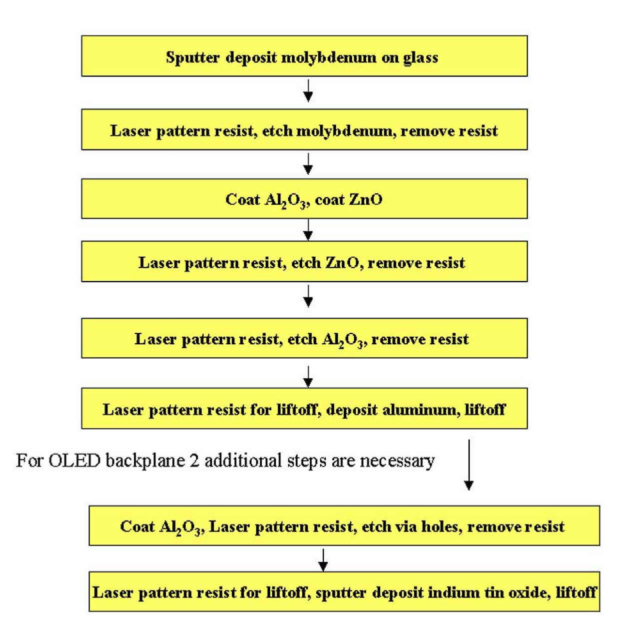

Figure 2. *Process step used to generate working devices*

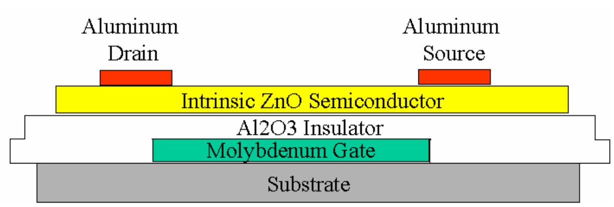

Figure 3. ***Cross-sectional view of a top contact zinc oxide transistor***

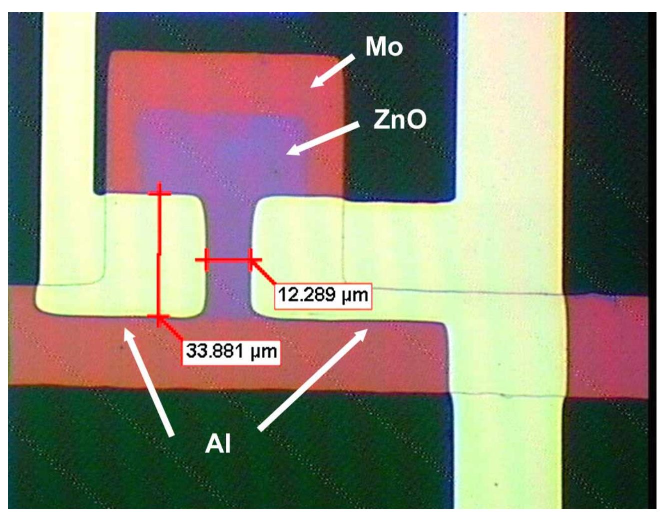

Figure 4. *Image of a laser-patterned zinc oxide transistor. Al_2O_3 is everywhere between the Mo gate and the ZnO.*

The transistor characteristics of a typical device are shown in Figure 5. The threshold voltages are typically 4 V and the mobility is ~16 cm^2/V-s at 20 V. There is a slight shift under bias stress as noted by changes in later scans. The on-off voltage ratio is greater than 10^8. The gate leakage current is exceptionally good at a low 10^{-12} A. These transistor characteristics make them a great candidate for driving OLEDs.

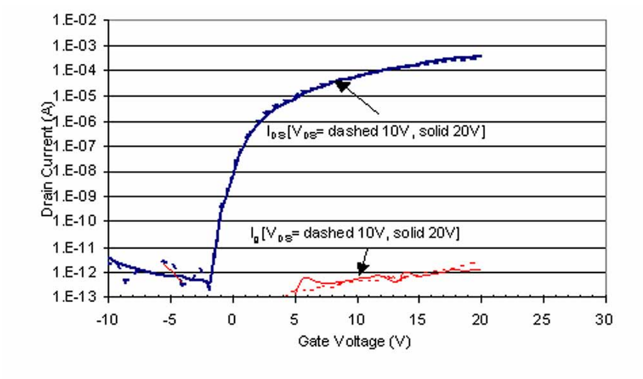

Figure 5. *Drain current versus gate voltage for a ZnO laser-patterned TFT with drain voltages of 10 and 20 V.*

7-Stage Ring Oscillator

The first circuit implement using these processes was a 7-stage ring oscillator. The purpose of this was both to test the patterning process and to analyze the responses of the 14 transistor oscillator structure.

The inverter stages consisted of two types of transistors. The pull-up transistors had a channel width to length ratio (w/l) of 2 and an absolute channel length of 20 µm. The pull-down transistor had a channel width to length ratio (w/l) of 20 and an absolute channel length of 20 µm. This gives the inverters a beta (ratio of w/l of the pull-down to pull-up transistors) of about 10. Because these are enhancement mode transistors, the pull-up transistor gate was tied to the positive voltage supply.

An important characteristic of circuit design is the transfer function. This is the voltage that is fed through the circuit to the next logic element. By looking at a single inverter we can see the transfer function characteristics. In Figure 6 the output of one stage of the inverter at a 20 V supply is shown. An input swing of 2−10 V results in an output swing of 11−1 V swing. This is sufficient to drive cascaded logic circuits without degradation. The inset shows the input voltage and output voltage from a single inverter versus time.

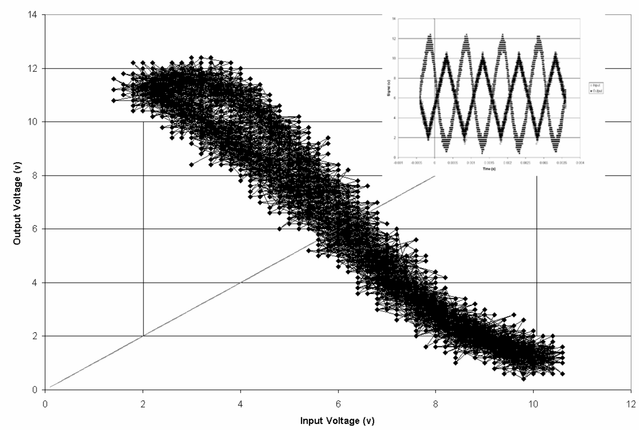

Figure 6. *Output voltage versus input voltage of a single inverter stage. The inset shows a 1 kHz triangle voltage drive of the inverter and the output voltage versus time*

In Figure 7 we show a patterned oscillator structure. The height of the device is 1.7 mm and width is 8.1 mm. Note the test pads, which are on 1 mm centers, and the large gate overlaps, which add capacitance and thereby slow the oscillation.

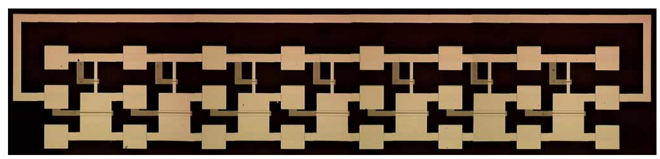

Figure 7. *Image of a work 7-stage laser-patterned zinc oxide ring oscillator*

Upon application of power the circuit oscillated spontaneously at a frequency of about 1 kHz with a voltage of 7 V. In Figure 8 the oscillation is presented in the voltage versus time graph. It should be noted that the asymmetry in the oscillation is as expected, using only enhancement mode transistors. The pull-down transistors pull strongly to ground but the pull-up transistors turn off as the voltage increases, giving a roll-off to the voltage.

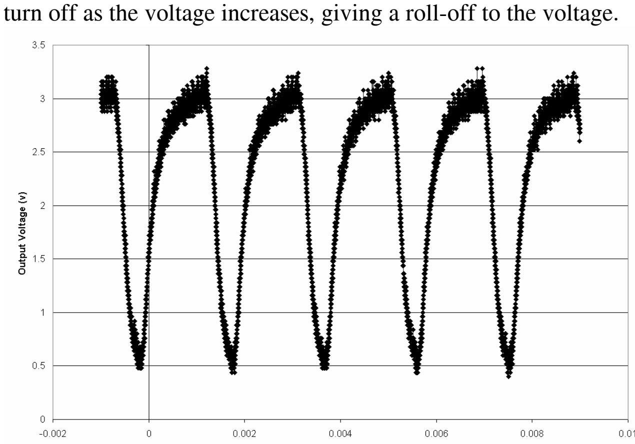

Figure 8. *Voltage versus time of ring oscillator with 7 V applied*

The oscillation frequency is highly dependent on the power supply voltage. In Figure 9 we show that at 20 V supply the oscillation is about 15 kHz. There is some variation based on the mobility, threshold voltage, channel width, and capacitance from device to device. In replicants, frequencies as high as 20 kHz at 20 V were obtained. A faster transistor can be obtained by reducing the channel lengths and gate overlaps [9].

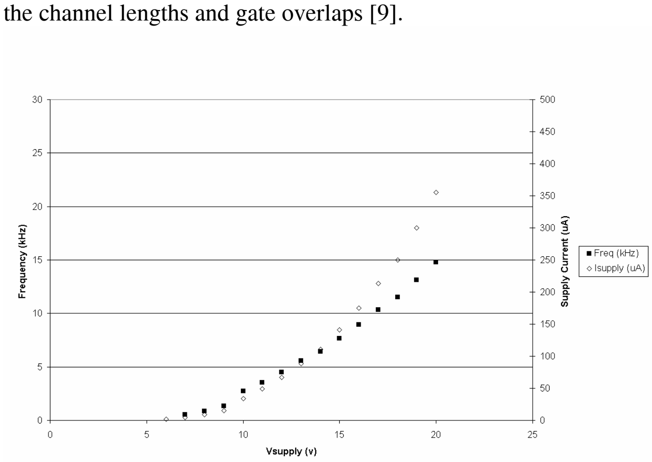

Figure 9. *Frequency and current versus supply voltage of the 7-stage ring oscillator*

Beating Oscillators

To demonstrate both logic circuits and cascaded signals a circuit was designed that used two high-frequency oscillators and beat them against each other. The schematic for this device is shown in Figure 10. The output was then used to directly drive an OLED device. Because the frequency mismatch can be voltage controlled and tuned very small, the beat frequency can be visually observed.

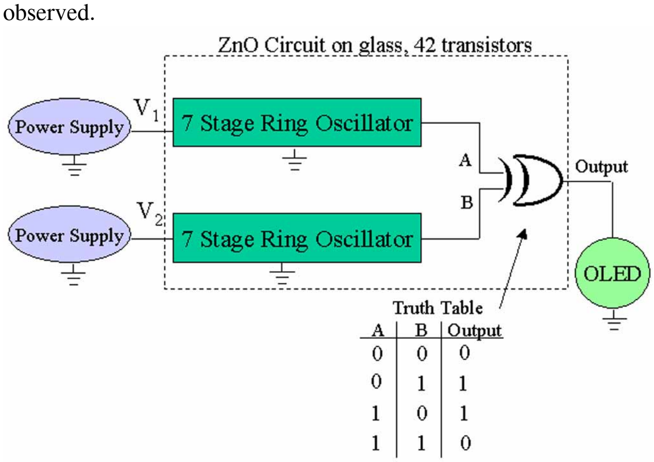

Figure 10. *Schematic of the circuit to generate a beat frequency*

To obtain the beat signal an exclusive OR (XOR) made from 2 NAND, 1 NOR gates, and 2 inverters was used as shown in Figure 11. Including the oscillators the circuit uses only 42 transistors.

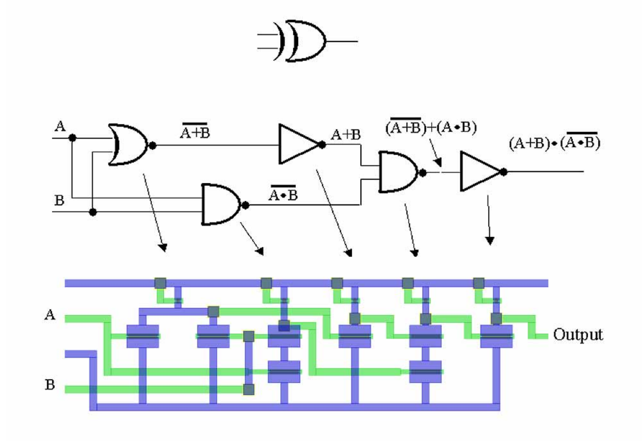

Figure 11. *Circuit and layout for an exclusive OR*

The use of separate supply voltages for each of the oscillators allowed the separate tuning of the frequencies to give a close match and hence a very slow beat frequency (~1 Hz). As the beat frequency is very sensitive to relative changes in frequencies, the stability of the transistors could easily be seen as a change on the beat frequency with time.

A simulation of the expected response using silicon transistors is shown in Figure 12. There is a rapid oscillation followed by a shutoff as the two oscillators beat against each other. The threshold voltages influence the shape of an oscillation and will have a large impact on the exact nature of the beat signal.

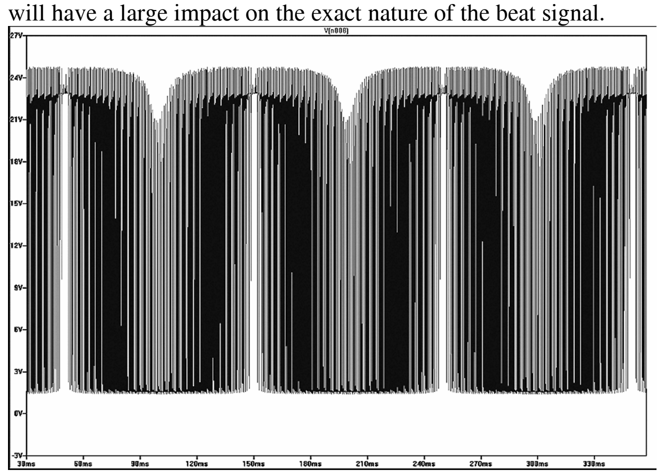

Figure 12. *Theoretical simulation of the beating oscillator circuit using silicon transistors showing duty cycle variation at the beat frequency*

In Figure 13 the experimentally measured data shows the expected beating frequency. With supply voltages of about 18 V the beat frequency was 10 Hz. The large number of oscillations per beat yield a smeared out region, which will look like lower average voltage and current and a regime of high voltage.

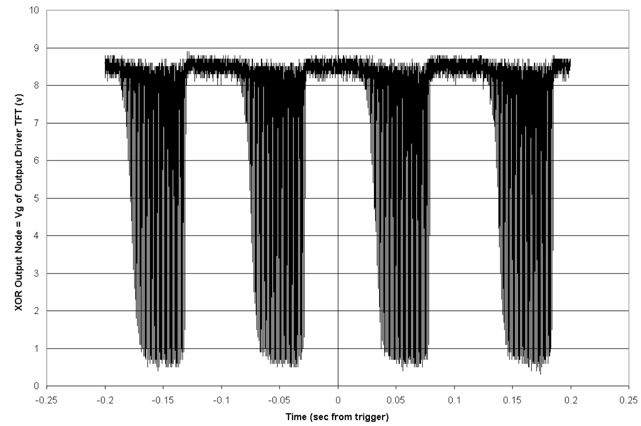

Figure 13. *Voltage versus time at the output of the XOR circuit with supply voltages set to cause the oscillators to beat at about 10 Hz*

At slightly higher mismatch of frequencies there are fewer oscillations per beat. These oscillations can clearly be seen in Figure 14. Here the supply voltages are about 19 V and the beat frequency is about 625 Hz.

The output was connected directly to a green OLED device anode and the cathode connected to ground. Changing the voltage on one of the supplies allowed a flashing rate of about 1 Hz to be obtained. As the oscillators were operating around 10 kHz a change of less than 1 part in 10,000 is easily detected in the rate. A 5 mV change every minute to one of the supplies was necessary to keep the oscillations from significantly changing and therefore prevent the OLED from flashing so fast that the beat became visually undetectable.

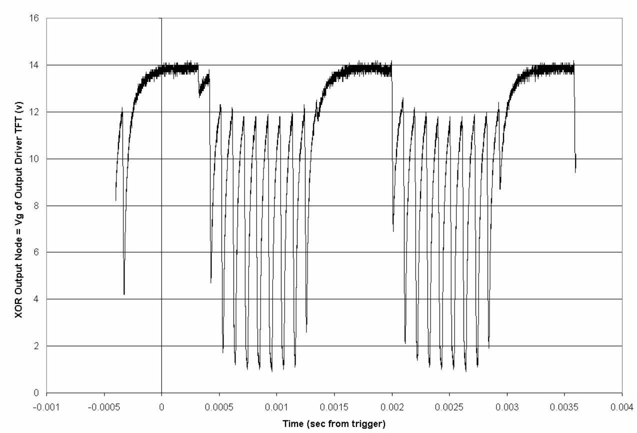

Figure 14. *Voltage versus time at the output of the XOR circuit with supply voltages set to cause the oscillators to beat about 625 Hz*

OLED Active-Matrix Backplane

The high mobility of ZnO transistors makes them ideal for driving OLED displays. An uncompensated circuit utilizing a drive transistor, a capacitor, and a select transistor can be quite small. This allows the active-matrix electronics to have a small fill factor for a bottom emitter, leading to longer life and lower drive voltages for the OLED device.

A common cathode bottom-emitting OLED active matrix requires two extra process steps as shown in Figure 2: (1) a passivation layer to prevent emission from the voltage lines, and (2) a patterned transparent anode connected to the drive transistor. An atmospheric deposition of 110 nm of aluminum oxide was again deposited and used as the passivation layer. The anode layer consisted of a patterned ITO layer.

Using these processes, we constructed an 8×8 active-matrix bottom-emitter OLED display. An image of a unit cell is shown in Figure 15. The OLED was a simple green emitter with a common cathode of 10:1 Mg:Ag.

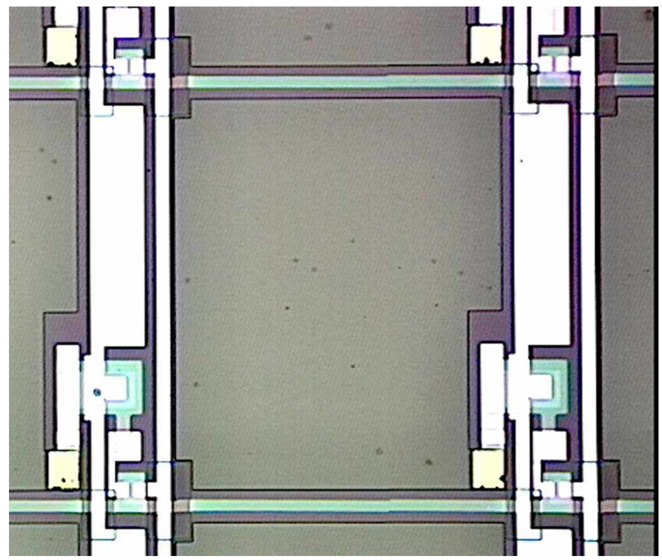

Figure 15. *Image of a unit cell of a laser-patterned ZnO 8 x 8 active-matrix backplane. The cell repeat is 1 mm*

The active matrix including the OLED was encapsulated and edge bonded. The device was driven with an image of the letter K in Figure 16. There were some pixels permanently on, which appear as very bright pixels. This is not surprising, as a short in the large drive transistor between the gate and source will hold the transistor on. The likelihood of defects is high given that no clean room was used in processing the backplanes.

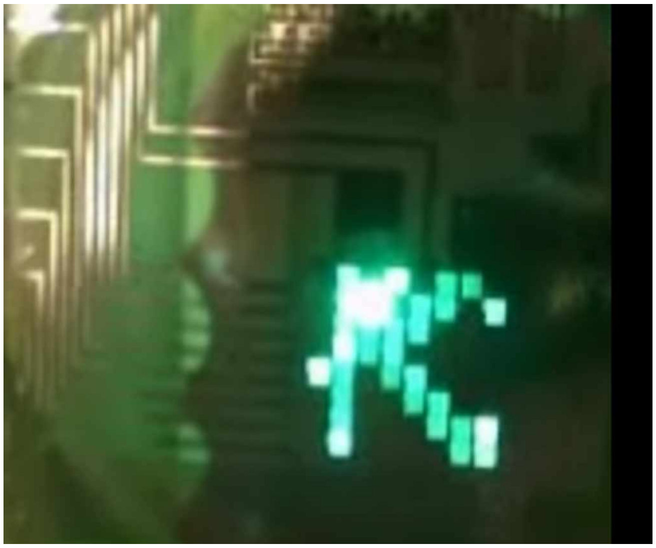

Figure 16. *8 x 8 active-matrix OLED driven with an image of the letter K*

Conclusions

There are many difficult challenges for generating a flexible next-generation display. Some of the most difficult are the low-temperature deposition of high-mobility transistors and alignment of the layers to previously patterned layers, especially when those layers may not have dimensional stability.

Here we have demonstrated high-quality transistors with high mobility capable of driving OLED pixels. Transistors having excellent on-off ratio were deposited at temperatures compatible with flexible organic substrates. This allowed the construction of logic circuits that could be cascaded without signal loss.

We have demonstrated patterning with an IR laser with feature size increments of 5 μm and comparable registrations. The patterning process is compatible with the necessary etchants and other materials while maintaining good transistor characteristics. The laser patterning process should allow an active feedback system to compensate for dimensional changes in the substrate, thereby mitigating alignment errors for large-scale patterns.

Acknowledgments

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Author Biography

Lee W. Tutt has worked in the area of light interactions with matter for over 23 years. He obtained his B.S. in chemistry from the California Institute of Technology (1979) and his Ph.D. in Inorganic Chemistry from UCLA (1984) He worked at Hughes Research laboratories for 8 years on laser material processes. In 1992 he joined Eastman Kodak Company where he has investigated laser dye transfer, ablation, and OLED technologies.