# Green Ink-Jet Technology for Fabrication of Multilayer Flexible Circuit Part II:

# Reliability Testing

***Ming-Huan Yang*, Chung-Wei Wang, Yuh-Zheng Lee, Kevin Cheng; Industrial Technology Research Institute , Hsinchu, Taiwan, R. O. C , E-Mail : miltenyang@itri.org.tw***

***Cheng Po Yu, Cheng Hung Yu, Chi-Ming Chang; Unimicron Company Taoyuan, Taiwan, R. O. C***

## Abstract

*The requirement of green technology is urgent for printed circuit boards (PCB). Not later to 2006, all the electronic products need meet green environment policy in Europe. In this paper, a novel and simple process to manufacture multilayer PCB was proposed. Follow our prior researches, base on the process of combining the self-assembly polyelectrolyte (SAP), ink-jet printing of catalyst, and electroless plating to form metal circuit pattern on the flexible substrate. This paper extended its application to fabricating of multi-layer flexible substrate. A double-sided flexible substrate with insulating material and connection holes was accomplished by this new improvement. By testing of IPC 6013 standard, the aspect ratio of thickness for metal foil and metal forming in hole was ideally near to one. In the impedance examination, the actual data was considerably closed to ideal data, within a variation of 0.4%. This improvement is helpful to fabricate high performance metal circuit on multilayer flexible substrate with holes.*

## Introduction

The green consciousness had been around for many years and the trend for environmentally-friendly deeply spread over a wider range of industries Classical PCB included several steps such as spinning photo resistor, mask patterning, etching photo resist and metal plating those are high pollution processes and face the urgent revolution. .

In recent year, non-photolithographic approaches to manufacturing printed circuits boards (PCBs) were proposed. Such as micro contact printing (μCP)[1], ink jet printing (IJP)[2] are corroborated to appropriate for this process replace. Especially, the ink-jet printing enabled to offer the additional advantages of low capitalization, low pollution, very high materials efficiency, elimination of photolithography, and non-contact processing [3]. In our prior researches, a specific approach that combined self-assembled polyelectrolytes, ink-jet printing catalyst, and electroless metal plating technologies for the fabrication of electrical circuits was successfully established. The products specifications had been accepted for industrial requirements.

Prior research [4,5,7] has completed about the ink formulation, polyelectrolyte recipe, and the process of electroless plating. In this paper, a fully process flow guided to manufacture multilayer PCB is proposed. We verified the sample in industrial standard, included the impedance test, flexure-angular test, storage problem, electrical performance, the line uniformity and sample reliability .

## Experimental Section

### *Ink-jet platform and deposition system:*

The ink-jet platform can be classified into three main groups: a four-axis X-Y-Z-θ platform, an optical system used for alignment, and a maintenance system to help jetting health control. All of components are set upon the granite base (AA Grade) with four vibration isolators to absorb the vibration. Moreover, two area CCDs read the alignment mark positions to align the position offset when loading substrate, and these marks are formed on the substrate in advance and can easy change by operator. A real time PC-based controller managed overall operation of the manufacturing process. The dimension of platform is about 2300mm (W)* 3000mm (L) * 1600mm (H). As for the printing speed, the maximum stage motion velocity is 25 in /s, and with the special divided frequency technology (DTF), the printing speed can reach up to 20 in/s, make the tack time of 20 sec at 400dpi*400dpi and 45 sec at 800dpi*800dpi resolution, respectively.

### *Measurement tools:*

An optical-interferometry 3-D surface profiler was used to measure the thin film profile (SNU Precision Co., Korea). It had a vertical resolution of 0.1 nm, and lateral resolution of 0.5 μm. Scanning range can be adjusted from micro to nanometer, depending on the interferometric optics (2x-5x, Michelson interferometry, 10x-50x, Mirau interferometry). The contact angle of water on the self-assembled films was measured using an KRUSS drop shape analysis system (DSA 10 MK2). The surface morphology and surface roughness of dip and spin self-assembled multilayer films were investigated using the tapping mode of atomic force measurement (AFM Nanoscope). An optical microscopy Leica MZ12 was used to observe the surface morphology of circuits.

### *Chemicals Preparation:*

Followed our prior researches by Cheng et al.[4], Poly(acrylic acid) (*M*w 90000) (PAA) was obtained from Polysciences. Poly(allylamine hydrochloride) (*M*w70000) (PAH)

and the Poly(sodium styrenesulfonate)(Mw 70000) were obtained from Aldrich. All polyelectrolytes were used as received without further purification. Polyelectrolyte dipping solutions of 0.01M (based on the repeat unit molecular weight) were made from 18MΩMillipore water and pH adjusted with either HCl or NaOH. Muitilayer thin film heterostructures comprised of alternating layers of polycation and polyanion were fabricated using an auto-dipping self-assembly equipment. These films were contained PAH ( Poly (allylamine hydrochloride) )/PAA ( Poly(acrylic acid) ) or PAH ( Poly (allylamine hydrochloride) )/PSS (sodium styrenesulfonate) or hybrid polyelectrolytes(PAH/PSS/ PAA).[4,5,6]

Pd-complex catalyst ink was adjusted to correspond with Spectra printed head (viscosity was 10cps, and surface tension was 40 dyne/cm). For following experiment, the electroless chemicals are commercially available.In addition, it is worthy of mentioning, the printed substrate must immerse into Autotech Accelerator solution for 3~10 sec. This step will improve the catalytic ratio.[7]

## Results & Discussion

### *Fabrication Procedure*

In this paper, commercial polyimide (PI) film was used as substrate for following–up experiment. In the first instance, the PI film (1) was cleaned with di-water and toluene, dried under constant temperature, and then stored at 40% relative humidity. PAH was used as the polyelectrolyte for the first layer adsorption to PI film, and PAA or PSS is the second layer and the covalently attached on PAH layer to form the polyelectrolyte multilayer (2). After that, the waterproof tape (3) was attached on each side of the substrate (step1) to protect polyelectrolyte multilayer from the damage of following drill procedure.

In the next procedure, the micro holes were formed on the substrate by mechanical and laser drilling (step 2), depend on the via-hole diameter. As all the holes completed, then followed the same prepare method to form polyelectrolyte multilayer around the inner wall of via-holes (step3). Next is a step to immerse the substrate into a catalyst solution to absorb the Pd nano-particles (5) on the inner wall of via-holes (step4).

After peeling the waterproof tape (7) at step 5, an ink-jet printing of catalyst patterned on the substrate surface is operated. It is notable that the waterproof tape was left on one side as a protection while the ink-jet printing of catalyst operates on the other side. At step 8, both sides of surface and via-holes were patterned with catalyst, and finally, the metal circuits (9) on both sides were formed by electroless plating while the copper ion exchanged with Pd from catalyst (step 9). The details can refer to the Fig.1.

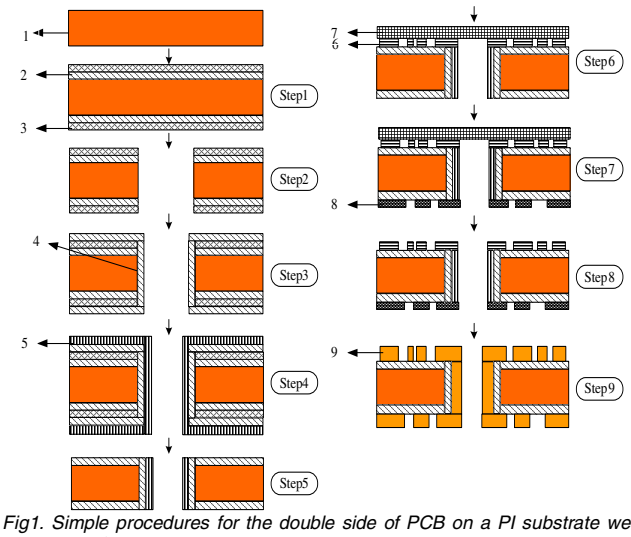



*Fig1. Simple procedures for the double side of PCB on a PI substrate were proposed.（1: PI substrate; 2: SAP; 3: waterproof; 4: SAP on inner wall of hole; 5: catalyst; 6: catalyst pattern; 7: waterproof; 8: catalyst pattern on the other side; 9: metal film）*

### *Electronic Performance*

The metal circuit electrical performance on the substrate manufactured follow above processes had been verified in Fig.2. A computer mouse pattern in four pieces on PI substrate was presented. The growth rate of metal film thickness is about 6μm / hr. Optimal electrical resistivity is about 2.1 μΩ.cm It's nearly ideal to bulk resistivity of copper ($\rho_{bulk,\ cu}$ = 1.67 μΩ.cm).

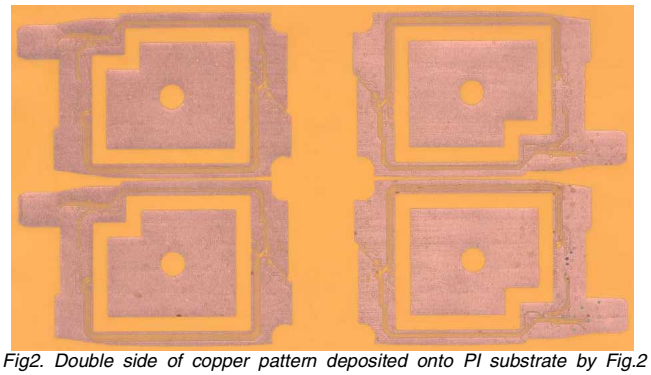
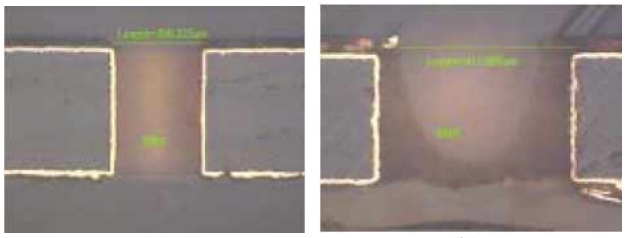


*Fig2. Double side of copper pattern deposited onto PI substrate by Fig.2 process. The copper deposits are approximately 9μm thick.*

Referring to prior reports, it was difficultly to ideally finish metallization of these via hole. It's because these inside walls were not readily accessible to processing solutions [8,9].Recently, we have designed a novel electroless plating system for metal deposition. During electroless plating, electrolyte passed through the hole not only by diffusion and surface convection, but also by force circulation flow. The vertical cross section of metallic via hole on PI substrate was observed in Fig.3. In usually, the ratio of classic process was 3:1.However, the amazing result was accomplished with almost perfect ratio of 1:1, thickness of surface metal, and thickness of inner metal of hole. The detail data compared with different radius of micro holes was demonstrated in the table1. In the table 1, it was clearly observed that the thickness of inner metal of via was perfectly to different radius.



(a) (b)

*Fig3. Vertical cross section o f (a) 200μm diameter and (b) 420μm vias on 250μm thick substrate which is processed using process of Fig.2.*

**Table1. The detail data compared with different radius of micro holes was demonstrated in this table**

| Thickness / Radius of holes | Surface Metal Thickness(um) | Inner Metal Thickness of via-Holes(um) | Ratio |
|---|---|---|---|
| 0.20 mm | 8.56 | 8.32 | 0.97 |
| 0.24 mm | 8.76 | 8.14 | 0.93 |
| 0.30 mm | 8.21 | 8.77 | 1.06 |
| 0.34 mm | 9.72 | 8.61 | 0.89 |
| 0.42 mm | 9.67 | 8.87 | 0.92 |

## *Reliability Testing*

In our prior study [5], the ink-jet printed circuit had been verified following the testing standard of IPC 6013. These examinations were included peeling test, peeling stress, adhesion capability, thermal test, thermal stress, hot oil test and soldering test. In this study, we further examined the impedance testing, flexure-angular testing, and its stability during electroless plating.

### *Electroless Plating Stability*

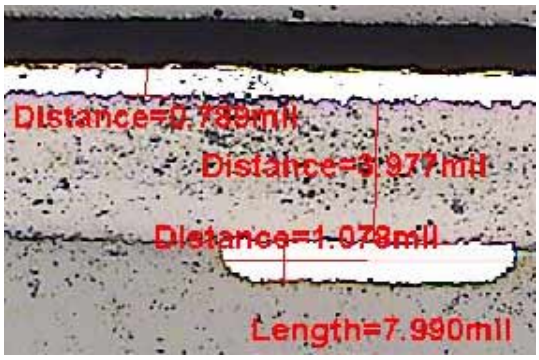
The quality of electroless plating stability is related to the plating location in solution bath. When the sample near the solution surface, it will be contaminated due to the plating solutions reacted with $CO_2$ in air, and form the side product of sodium carbonate. It resulted that non-uniform deposition of copper on substrate. The solution is simply to place two dummy plate (or substrate) to block the interface between the solution surface and sample, to avoid from the penetration of $CO_2$ into plating solution directly.

**Table. 2 Stability verification for electroless plating, the design value is 20 Ω, eight samples at same plating condition were proceed.**

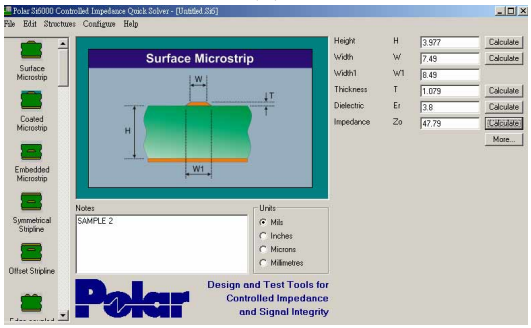
| Sample# | Variation |
|---|---|
| 1 | -0.62% |
| 2 | 4.35% |
| 3 | 4.35% |
| 4 | 2.69% |
| 5 | -0.62% |
| 6 | -5.59% |
| 7 | -7.25% |
| 8 | 2.69% |

## *Impedance Testing*

The electronic reliability of circuit boards was traced by impedance calculation. All experiment data were analyzed by Polor Si6000 Coltrolled Impedance Quick Solver form Unimicron company. The vertical cross section of test circuit was showed in the fig.4 (a). In the Fig.4 (a), the circuit line with, circuit thickness and substrate thickness were 7.99 mil, 1.078 mil and 3.977 mil, respectively. The actual impedance data was 48.02 ohm considerably closed to ideal data 47.79 ohm, within a variation of 0.4%, as Fig.5 (b)..




**(a)**

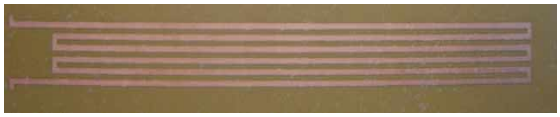



**(b)**

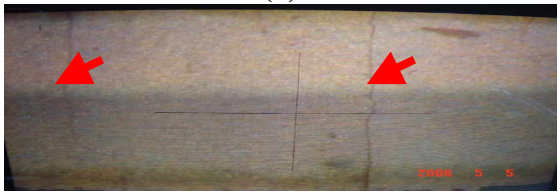
*Fig4. (a) The vertical cross section of test circuits, (b) The result of impedance calculation using commercials equipment.*

### *Flexure-Angular testing*

For flexure-angular test, a standard apparatus follow the IPC IPC 6013-3.6.1 & 3.6.2 specification was constructed. In the Fig. 5(a), the line width and metal film thickness were 1 mm and 8 μm, respectively. During the flexure-angular verification, the circuit will has chance of cracking if inappropriate treated the polyimide surface, as in the Fig5. (b). In the future, we will dedicate to further modification of the polyimide interface, by some physical treatment method like plasma, before the forming of polyelectrolyte multi-layers, to enhance its bonding strength with substrate.



**(a)**



**(b)**

*Fig5. (a) Cu metal test key was manufactured by prior process for flexure-angular verification; (b) the defects of metal circuit were formed after*

*flexure-angular verification.*

## Conclusion

In recent year, the environmentally-friendly process is demand immediate for printed circuit boards (PCB). In this paper, a novel and simple process to manufacture multilayer PCB was proved. A double-sided flexible substrate with insulating material and connection holes was accomplished by this new improvement. By testing of IPC 6013 standard, the aspect ratio of thickness for metal foil and metal forming in hole was ideally near to 1. In the impedance examination, the actual data was considerably closed to ideal data, within a variation of 0.4%. These results and improvement are helpful to fabricate high performance metal circuit on multilayer flexible substrate with holes by our process. However, the brittle metal film still was a major challenge. In the future, we will dedicate to further modification of the polyimide interface, by some physical treatment method like plasma, before the forming of polyelectrolyte multi-layers, to enhance its bonding strength with substrate.

## Reference


1. Hidber, P. C.; Helbig, W.; Kim, E.; Whitesides, G. M. Langmuir, **1996**, 12, 1375-1380.
2. Shah, P.; Kevrekidis, Y.; Benziger, J. Langmuir **1999**, 15, 1584-1587.
3. K.F. Teng and R.W. Vest, *IEEE Electron Device Lett.*,**199**8, 9, 591.
4. Kevin Cheng , Ming-Huan Yang, Wanda W. W. Chiu, Chieh-Yi Huang, Jane Chang , & Tai-Fa Yin, Macromolecules Rapid Communication, 2005, 26(4), 247-264.
5. M. H. Yang, S. Chiu, C. W. Wang, C. J. Lin,Chang, Cheng, ""Pattern Recognition and Analysis for Circuit Fabrication by Ink-Jet Printing", J. Imaging & Science Technology, accepted, 2006.
6. Wang, T. C.; Chen, B.; Rubner, M. F.; Cohen, R. E. "Selective Electroless Nickel Plating on Polyelectrolyte Multilayer Platforms", Langmuir, 2001, 17, 6610-6615.
7. Ming-Huan Yang, Chung-Wei Wang, Jane Chang & Kevin Cheng, "Circuit Fabrication by Ink-jet Printing on Hybrid-multilayer Polyelectrolytes "1st Inter. Conf. on Digital Fabrication Technologies, USA, 2005, p.72-75
8. D. B. Moser, *Printed Circuit Fabrication*, 1997, *20(2)*, 20-.
9. C. F. Coombs, Jr., Editor-in-Chief, *Printed Circuits Handbook*. New York: McGraw-Hill, **1996.**


## Author Biography

*Ming-Huan Yang received his Master degree in Chemistry from National Cheng Kung University in 2002. He is now a system integration engineer in the Printable Science Department, Display Technology Center of Industrial Technology Research Institute at Taiwan. His research interest covers industrial ink-jet printing processes development especially in PCB and display fabrication.*