High Performance Nanomaterial-based Inorganic Printed Semiconductor

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Abstract

The opportunity to deliver unprecedented material and device performance by utilizing unique properties of nanomaterials has generated tremendous interest in both the academia and the industries. In this work, we demonstrate the successful synthesis and printing of quasi-two and three-dimensional (D) inorganic oxide semiconductors with controlled morphologies on a number of device substrates via an environmentally-benign process. Compared to previously reported data of similar nature, a high Hall-effect mobility (~ 50cm^{2}V^{-1}s^{-1}) is obtained with our nanomaterial-based inorganic printed semiconductor. Using these nanomaterials, a rapid printing process has been developed to strategically pattern features in the millimeter to submicrometer length scale regimes. We show also the seamless integration of these nanomaterials to obtain high performance electronic devices, for example thin-film field-effect transistors (TFTs) with the printed semiconductor as the active channels. Excellent device performances with high field-effect mobilities, μ_{eff} > 20cm^{2}V^{-1}s^{-1}, and respectably high drain current on-to-off ratios, $I_{ON/OFF}$ > 10^4, are obtained with our TFTs.

Introduction

The significant impact brought upon by realization of all-printed electronics via the additive patterning routes as compared to traditional subtractive patterning approaches cannot be over-emphasized.[1-3] However, such a realization requires not only a good electrical conductor and a high dielectric-constant insulator but also a high-performance printable semiconductor, which currently presents a major technical challenge – in particular, printable semiconductors of inorganic nature that are derived through low-temperature fabrication routes and simultaneously insensitive to oxygen/carbonaceous contaminants from the ambient.

Typically, inorganic semiconductors which exhibit intrinsic carrier mobilities larger than its amorphous counterparts and organic materials are highly preferred and deemed to form the basis for future high-performance micro- and macro-electronics. This is especially true in applications, for example, which involved advanced display technologies that require reasonably good performance switches for addressing the active matrices.

Exploring, designing and creating materials at the nanoscale could potentially lead to applications that achieve exceptional performance – possibly allowing more efficient and less expensive manufacturing processes. Printable inorganic semiconductors based on nanomaterials, which derive from low-temperature solution routes and exhibit reasonably high charge mobilities, could likely provide a viable solution to bridging the missing gap in achieving the goal of all-printed electronics. In this respect, semiconducting metal oxide nanomaterials - in the form of 2- and 3-D geometries - appear as promising candidates. Intrinsic zinc oxide (ZnO) certainly serves as one of the promising candidates due primarily to its high optical transparency, tunable electrical and optical properties, and inertness towards oxygen/carbonaceous contaminants from its operating environment. Numerous techniques have been reported to synthesize ZnO nanostructures - nanowires, nanorods, nanowalls and nanobelts.[4-6] Nevertheless, harnessing the unique potential of these ZnO semiconductor nanomaterials to obtain high-performance electronics requires both consistent productions and subsequent seamless process integration.

Here, we first show the successful synthesis of an enriched spectrum of quasi-two and three dimensional ZnO semiconductor over multiple length scales on a number of device platforms. Next, we demonstrate manipulation of these nanoscale entities into forming millimeter and submicron-sized features and their integration to obtain high-performance TFTs.

Experimental

The ZnO nanostructures were synthesized consistently in a customized home-built system. The structural morphologies of the as-synthesized ZnO nanostructures were investigated using a field-emission scanning electron microscope. X-ray diffraction (XRD) measurements of the nanostructures were performed using the Cu Kα line at room temperature in the ambient. The Hall measurements of the nanostructures were performed at room temperature in dark ambient using the van der Pauw techniques. The device performances of the nanostructure-integrated TFTs were investigated on a probe station linked to a semiconductor parameter analyzer (Agilent 4156C).

Results and Discussion

The low-temperature approach adopted in our work provides a versatile route to obtain a dynamic range of quasi-2 and 3D nanostructures on multiple device platforms, which include but not limited to aluminum oxide, silicon dioxide and polymeric substrates. Figure 1 shows examples of different structural properties of ZnO nanostructures obtained with our approach.

Nanostructures with diameters ~ 50 to 100 nm and submicron structures could be obtained reproducibly. As can be evidently seen in Figure 1 and 2, intricate hyper-branched structures and uni-directional nanostructures can be synthesized exclusively by tweaking the growth conditions.

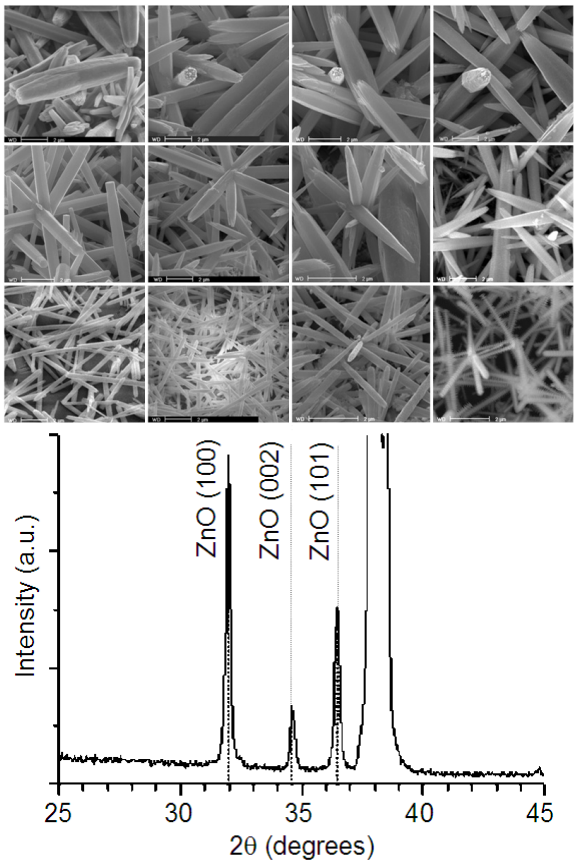

Figure 1. (Top) Field-emission scanning electron microscopy (FE-SEM) images showing the morphological evolution of ZnO semiconductor nanostructures under different synthesis conditions. (Bottom) A representative XRD spectrum showing the major crystallographic peaks of our hyper-branched ZnO nanostructures.

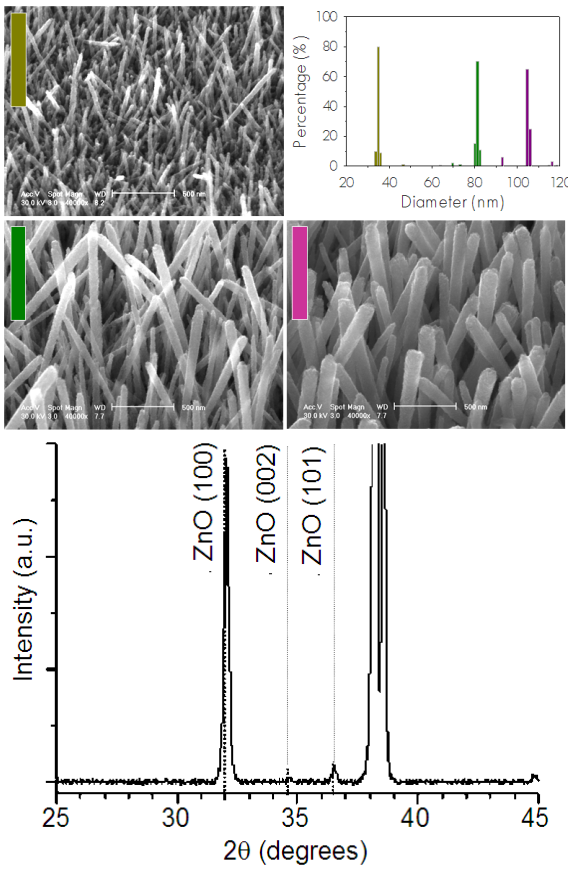

Figure 2. (Top) FE-SEM images showing uni-directional ZnO semiconductor nanostructures. The inset is a histogram showing the narrow distributions of the diameters of the nanostructures. (Bottom) A representative X-ray diffractogram showing the major crystallographic peaks of our *uni-directional ZnO nanostructures.*

These nanostructures typically present a hexagonal cross-sectional morphology, in accordance with the wurtzite crystal structure of ZnO (*c*-plane). XRD analysis further confirms their crystallographic properties – having signature diffraction peaks (lattice constants) in agreement with values reported in the standard card (JCPDS 36-1451). Interestingly, as shown in Figure 2 (Bottom), a predominant peak corresponding to ZnO (100) is observed – suggesting a majority of the 1D nanostructures aligning (vertically with respect to the substrate plane as shown in Figure 2 (Top)) along this particular crystallographic direction.

We have also investigated the carrier mobilities of our ZnO semiconductors. The Hall-effect mobilities are summarized in Figure 3. A remarkably high Hall-effect mobility of ~ 50$cm^2V^{-1}s^{-1}$ can be obtained with our printed ZnO nanomaterial-based semiconductors. The performance compares favorably with previously reported data from other printing means and vacuum-based processes – suggesting the high crystalline quality of our ZnO semiconductor. All of our ZnO semiconductors show essentially n-type behavior, in accordance with that of un-doped ZnO. An excess of Zn ions and/or oxygen vacancies are thought to contribute to the free electrons for the electrical conduction.

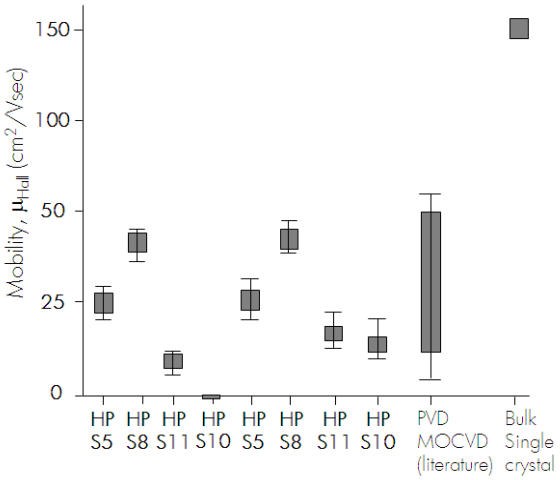

Figure 3. A comparison of the Hall-effect mobilities of our ZnO semiconductors with those reported in the literature.

Besides demonstrating the capability to synthesize high-quality nanomaterials, the ability to manipulate these ZnO nanomaterials into functional components is critical to the realization of practical applications. Next, we show patterning of these nanomaterials via our gravure printing process. Figure 4 shows FE-SEM images and optical micrographs of our gravure-printed ZnO semiconductor patterns. Notably, both images show a rather smooth surface morphology. As shown in the optical micrographs, complex and periodic features over multiple length scales can be reproducibly produced by this printing means. X-ray diffractograms (not shown) similar to those as shown earlier are observed with these samples.

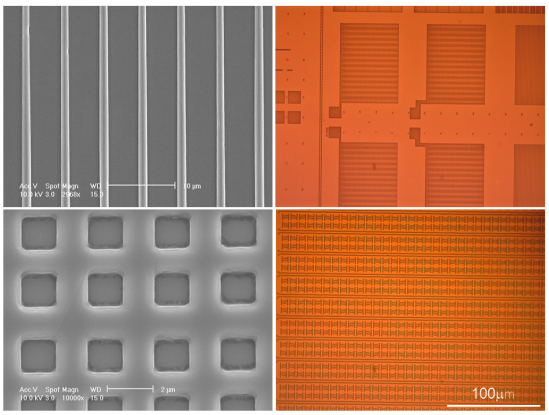

Figure 4. (Left) FE-SEM images showing the formation of submicron and micro-sized ZnO semiconductor via the gravure printing process. (Right) Optical micrographs showing larger footprints of the printed ZnO patterns. The scale bar applies to both optical micrographs.

The seamless process integration of nanomaterial-based ZnO semiconductor is critical to the realization of high-performance all-printed electronics. In particular, ZnO-TFTs could provide a very promising high-performance yet low-cost substitute and key component for next-generation optoelectronics and flat-panel display respectively.

Figure 5 (Left) shows a pixel-addressable matrix consisting of 32 by 32 arrays of TFTs while a 3D schematics is shown on the right delineating the architecture of our test-bed – a back-gated TFT employing heavily-doped silicon as the gate electrode and silicon dioxide as the gate dielectric.

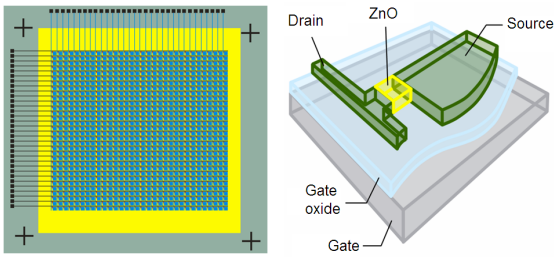

Figure 5. (Left) A 32 × 32 arrays of ZnO-TFTs. (Right) A 3D schematics showing the critical components of our ZnO-TFT.

Figure 6 shows a collection of $I_{ds} - V_{ds}$ profiles of ZnO-TFTs with different channel lengths under the influences of different gate voltages V_{gs}. As observed in each profile, the drain current I_{ds} at respective source-drain voltage V_{ds} increases with increasing V_{gs}; suggesting *n*-type conduction of the active ZnO channel and hence *n*-FET operation. Nearly all of our ZnO-TFTs show 'hard' saturations at higher V_{ds}. The *I-V* trends behave similar to classical MOSFET, suggesting pinch-off mechanism in operation in these devices.[7-8]

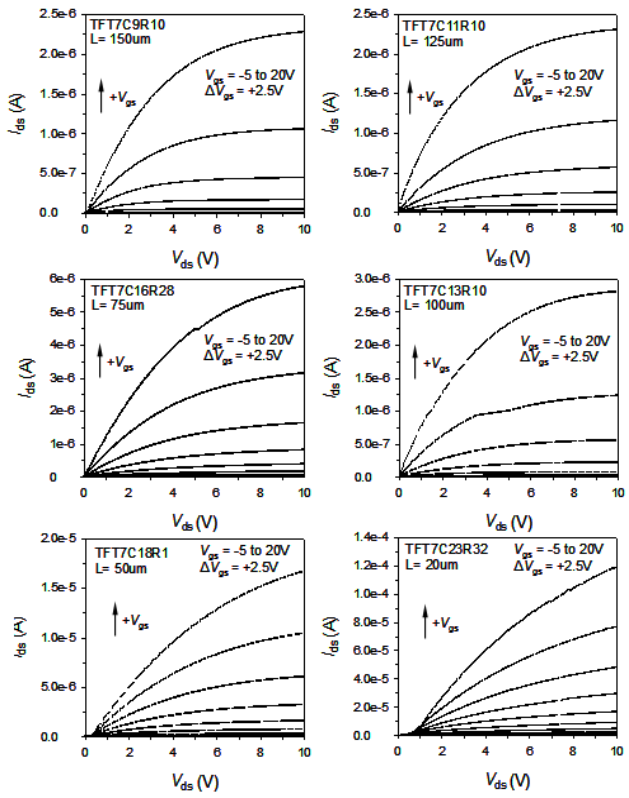

Figure 6. $I_{ds} - V_{ds}$ curves of TFTs with different channel lengths employing ZnO nanostructures as the active channels.

Significantly higher field-effect mobility (> 20 $cm^2V^{-1}s^{-1}$) could also be observed in our ZnO-TFTs. Figure 7 shows an example of such a TFT (with L = 10 μm). Similar to other ZnO-TFTs, the drain current I_{ds} at respective source-drain voltage V_{ds} increases with increasing V_{gs}; again suggesting similar device operational mechanism. dI_{ds} increases with increasing V_{ds} but does not enter into 'hard' saturation region within the measured V_{ds} window at higher V_{gs} (≤ 10V). From the corresponding transfer characterisitcs at various V_{ds}, the threshold voltage V_{th} is estimated to be ~ 6V and the subthreshold slope is calculated to be ~ 6V/decade, with an on-to-off current ratio $I_{ON/OFF} > 10^2$.

Considering the linear region, where V_{ds} is small, and assuming charge-sheet approximation,[7]

$$I_{ds} = \mu_{eff} C'_{ox} (W/L)(V_{gs} - V_{th})V_{ds}$$

where μ_{eff} is the field-effect mobility, C'_{ox} the capacitance of the active channel, W the channel width and L the channel length, the correponding field-effect mobilities of ZnO-TFTs were calculated and shown in Figure 8. In general, the field-effect mobility increases with decreasing channel length for a channel width maintained at 200 µm.

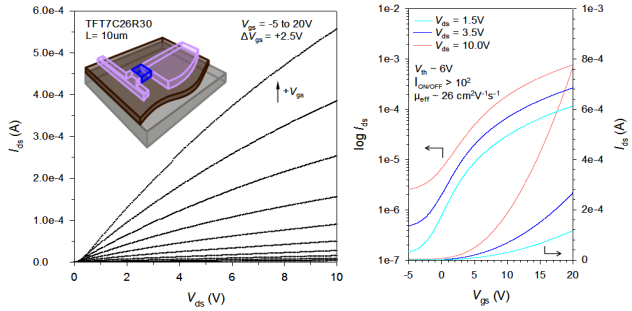

Figure 7. Ids – Vds curves of a TFT employing nanomaterial-based ZnO semiconductor between the source and drain electrodes. The transfer characteristics is shown on the right.

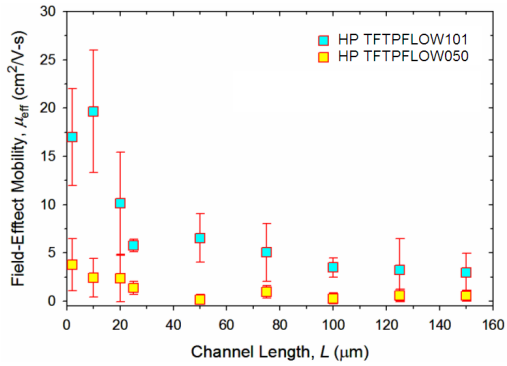

Figure 8. The effects of channel lengths on the field-effect mobilities of ZnO-TFTs. The statistical data at each channel length represents a sampling size of 5 – 10 devices.

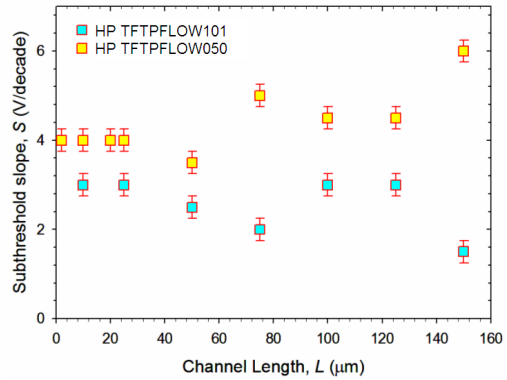

Figure 9. The effects of channel lengths on the subthreshold slopes of ZnO-TFTs.

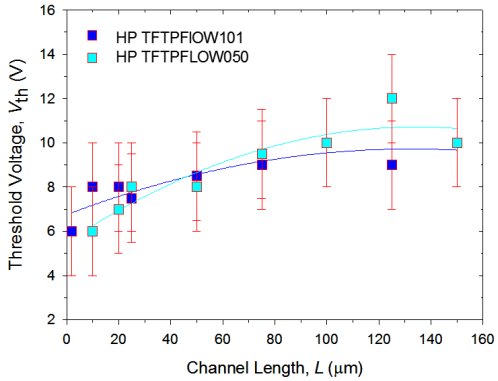

Figure 10. The effects of channel lengths on the threshold voltages, V_{th}, of ZnO-TFTs.

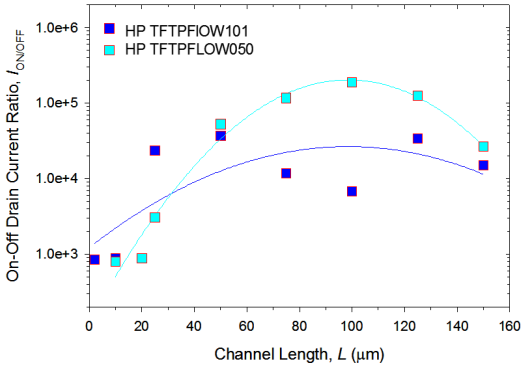

Figure 11. The effects of channel lengths on $I_{ON/OFF}$ of ZnO-TFTs.

The influences of channel lengths on the subthreshold slopes of the TFTs are revealed in Figure 9. As observed from the transfer characteristics in Figure 7 and others (not shown), the subthreshold slope, S, is exponentially related to V_{gs}. A steep subthreshold slope is highly desirable for the ease of switching the TFT to off-state. Our TFTs typically fall in the range of 1 – 6 V/decade, with an average S ~ 3.5 V/decade. A high ZnO-SiO_2 interface trap density could be attributed to the large S and is expected in our devices. However, the rather insensitivity of S over multiple channel lengths is in accordance to conventional wisdom and should only be a function of temperature (which was kept constant in our case). It is expected that optimization of the ZnO integration process could lead to a lower S, approaching that of current MOSFET.

As expected and shown in Figure 10, the threshold voltages of our TFTs decrease with decreasing channel lengths. The approximate threshold voltages were determined by the extrapolated intercepts of the linear portions of the I_{ds}- V_{gs} curves with the V_{gs}-axes - giving the approximate values of V_{th}. Although the linearly-extrapolated threshold voltage is slightly higher in reality than the "$2\psi_B$" V_{th} due to inversion-layer capacitance and other effects, the present approach serves to show the desired trend which is in accordance to previously reported literature. As shown in the plots, our ZnO-TFTs operate in the enhancement-mode.

Figure 11 shows the trend of on-to-off I_{ds} ratios with respect to channel lengths. Our ZnO-TFTs show respectable $I_{ON/OFF}$ ratios > 10^3 for $L > 10$ μm. These are required for proper operation of the TFTs as electrical switches in various applications. Further investigations are required to fully elucidate the observed phenomena.

Conclusion

In conclusion, we have demonstrated synthesis of high carrier mobility ZnO semiconductor via a low-temperature route at atmospheric pressure. Complex and periodic features over multiple length scales have been demonstrated using our gravure printing process. High-performance TFTs have been further demonstrated while incorporating these nanomaterials-based ZnO semiconductors. The exhibited performance, low-temperature processing techniques (< 350ºC) and intrinsic tolerance of these nanomaterials towards oxygen/carbonaceous contaminants from the ambient could potentially afford many favorable electronic applications.

References

1. B. A. Ridley, B. Nivi and J. M. Jacobson, *Science* 286, 746 (1999).
2. http://www.it-strategies.com/Spectrum/2004/12.htm.
3. H. Sirringhaus, T. Kawase, R. H. Friend, T. Shimoda, M. Inbasekaran, W. Wu, and E. P. Woo, *Science* 290, 2123 (2000).
4. H. T. Ng, B. Chen, J. Li, J. Han and M. Meyyappan, *Appl. Phys. Lett.* 82, 2023 (2003).
5. H. T. Ng, J. Li, M. Smith, P. Nyugen, A. Cassell, J. Han and M. Meyyappan, *Science* 300, 1249 (2003).
6. W. Z. Pan, Z. R. Dai and Z. L. Wang, *Science* 291, 1947 (2001).
7. H. T. Ng, J. Han, T. Yamada, Y. P. Chen, P. Nguyen, and M. Meyyappan, *Nano Letters* 4, 1247 (2004).
8. Y. Taur and T. H. Ning, Fundamentals of Modern VLSI Devices (Cambridge University Press, 1998).

Author Biographies

Hou-T Ng received his B.Sc (Honors) and Ph.D. in Chemistry from the National University of Singapore (NUS). He specializes in the area of nanoscale science and nanotechnology, particularly in nanostructure synthesis, assembly and nanodevices integration. Prior to joining HPL of the Hewlett-Packard Company, he was a senior research scientist and a project lead of the nanoelectronics and nanophotonics research group at the Center for Nanotechnology, NASA Ames Research Center.

Alfred Pan received his Ph.D. in Materials Engineering from the University of Illinois (Urbana-Champaign). He has been involved with thermal ink jet printing and other non-impact printing technologies since joining HPL in 1984. He had engaged in the R&D in IC processing technology in Philips Research Lab prior. His interests as a project manager in HPL have been in the emerging technologies including power sources for portable devices and nanotechnology. He holds 37 US patents