Large Area Distributed Electronics

Robert Reuss, Defense Advanced Research Projects Agency, Microsystems Technology Office, Arlington, Virginia, USA

Abstract

Microelectronics and, particularly, silicon integrated circuit microelectronics, has produced amazing capabilities over the last 40 years. There are numerous indicators of this, but best summarized as "Moore's Law." While more transistors/ cm^2 is the driving force, the microelectronics-based display industry has, for over a decade also explored alternate directions – larger and larger "chips" and/or alternative substrates. Thus, displays have grown from several in^2 to several ft^2 while the number of transisors/cm^2 has remained small. Further, major R & D investment has been made in migrating from a glass substrate "chip" to a plastic one in order to achieve increased functionality (again without increasing the transistors/ cm^2).

The relatively low cost manufacturing process used for displays has created significant interest in applying this form of microelectronics to other classes of problems. An example is an image array. Here the amorphous TFT can also be used as a light sensor. This leads to digital x-rays with many advantages over the conventional film based methods. The sensor function might also cover other parts of the EM spectrum to provide a large area IR imager or RF antenna array (communications and radar). Other sensor techniques would provide the capability to monitor stress or corrosion while integration of actuators would lead to the capability to not just monitor the environment, but to respond to it (modification of a property in response to a stimulus).

To accomplish such sensor applications, more transistors/ cm^2 is not the issue. Rather the ability to cost effectively fabricate modest numbers of integrated devices ($<10^5$) over large areas ($>ft^2$) is essential. Even then, other attributes may also be required (such as flexible substrate). Perhaps the most demanding feature that has not been developed by either the integrated circuit or display industries is a high performance TFT.

Transistor performance is determined by materials properties and critical dimensions. Microelectronics progress has been based on the favorable material characteristics of silicon (and its oxide) and the drastic scaling (from 10's of microns to tenths of microns) that has been achieved. Cost effective manufacture of TFTs over large areas limits both the material and dimensional properties that can be achieved and results in a 10-100x reduction in device performance. While not a significant limitation for displays, it is for applications that require performance in the MHz and higher regime.

One approach to achieving higher performance TFTs is to improve the process conditions that are currently used to fabricate poly TFTs. This might be achieved by better recrystallization and oxidation methods or by processing "off line" and then transferring onto the preferred substrate. While such methods are well known, there are still challenging technical hurdles. A novel means to circumvent many of these problems might be accomplished via printing of Si nanowires or C nanotubes as the active material of TFTs. Both materials have significant issues, which must be overcome.

DARPA is currently funding work in a variety of areas expected to impact the migration of microelectronics from "smaller is better" to "bigger is better". Status and objectives of these efforts will be presented especially from the perspective of opportunities to achieve the desired results with digital fabrication methods.

Author Biography

Dr. Robert H. Reuss joined the Defense Advanced Research Projects Agency (DARPA) Microsystems Technology Office as a Program Manager (MTO) in August 2001. He is responsible for the Large Area Distributed Macro Electronics (Macroelectronics) and Clockless Logic(CLASS) programs for the MTO. He is also responsible for the Mission Specific Processing program for the TTO. His technology interests lie in the area of application of materials and electrochemistry technologies for advanced microelectronic applications and microsystems integration.

Prior to joining DARPA, Dr. Robert Reuss was a Research Faculty member at the University of Colorado and he worked seven years for the U.S. government as a research and development manager. He joined Motorola Semiconductor Products Sector in 1981, where he led development teams in the area of evaluation and application of new device fabrication process technologies. This included rapid thermal annealing, selective epitaxial growth, silicon on insulator and maskless ion beam implantation. He also worked in strategic technology for Motorola focussing on low-power technologies aimed at reducing current drain. In 1996 he was named Director of Advanced Technology for Motorola Energy Systems, addressing the development of electrochemical capacitor technology for novel applications in wireless communications, portable power and transient power load leveling applications. In August 1997, he joined the Flat Panel Display Division. His major responsibilities included directing teams developing advanced emitter and display materials, and the acquisition and protection of intellectual property. From June 2000 until August 2001, he worked as a strategy and external research manager for the Semiconductor Sector of Motorola.

Dr. Robert Reuss received a Ph.D. in Chemistry from Drexel University in 1971. Dr. Reuss is an elected Member of Motorola Science Advisory Board, Senior Member of IEEE and a past chairman of the Phoenix Chapter of IEEE Waves and Device Societies. He has published over 50 papers and has been awarded 12 U.S. patents.