The Current of CCD Image Sensor Development

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Abstract

First, basics of CCD image sensor will be shortly reviewed. Second, the super CCD will be presented, and its characteristics are discussed in comparison with a conventional ITCCD. Third, the topics of current developments will be discussed. Hitherto, the main theme of developing CCD image sensor has been on how to reduce the pixel size, especially for DSC applications. Already, the pixel size has become about 2-μm squire, and a pixel number has increased over 5 millions which makes the resolution equal to that of a film camera. Now, the pixel number competition will be on the final stage. The next challenges will be shift to the technologies for enhancing sensitivity, widening dynamic range and making a high frame rate movie from a mega-pixel imager. New technologies for realizing such requirements will be introduced, which are a dual pixel structure for widening the dynamic range and a horizontally signal charge mixing architecture to output a high frame movie.

Basics of CCD Image Sensor

The concept of a charge coupled device (CCD) is storing and transferring charge packet in a depleted semiconductor layer.[1] Figure 1 shows a cross section and channel potential profiles of a popularly used 4-phase driving CCD. The charge transfer is controlled by 4-phase pulses applied on the transfer electrodes, and the charge packets are transferred in the n-type buried channel layer without interacting with the Si surface in which a large number of electron trap levels are distributed. As shown, the CCD acts as an analog shift register, in which signals are expressed with electron numbers in charge packets. The heart of CCD is on transferring all electrons stored in a potential well to the next well completely, which is called the complete transfer mode. The complete transfer mode makes the CCD to be the best architecture for an image sensor application, because an electron number in a well is preserved against fluctuations of voltage and current. Therefore, the CCD has extremely high signal to noise ratio (S/N). A block diagram of a CCD image sensor is shown in Figure 2, which is called as the interline transfer CCD (ITCCD), and is the most popular for applying camcorders and digital still cameras (DSC).The vertical transfer CCD's (VCCD) are light-shielded, and act as an analog frame memory. Charge packets integrated in the photodiodes are transferred into the VCCD's by opening the transfer gate. The charge packets in the VCCD's are transferred to the HCCD in parallel, and are transferred to the output circuitry serially and output one after another. In case of progressive scan, the signal packets in all pixels should be transferred into VCCD simultaneously and output with making up one frame. Another readout type is the interlace scan, which separates the frame image into two fields. At the first field, signal packets in the odd lines are readout, and those in the even lines are readout at the second field. While the interlace scan fits the conventional TV format such as NTSC, it isn't applicable to the mechanical shutter less DSC because of time difference between two fields. A cross section of ITCCD pixel is shown in Figure 3. Incident rays are focused on a photodiode surface through a color filter and a photo-shield window by the micro lens. The photodiode comprises two key technologies, i.e. the vertical overflow drain and the buried photodiode. The former has a flat p-well on reverse biased n-substrate, which protects a image signal from a excess charge diffusion caused by strong light, and prevents the invasion of unfavorable electrons (noise and smear) diffusing from the substrate. The latter has p+ surface layer which keep the thermal equilibrium condition, and suppresses the noise electrons thermally generated in the Si surface by $2n_i / p_s$ (p_s is the surface hole density and n_i is the intrinsic carrier density).

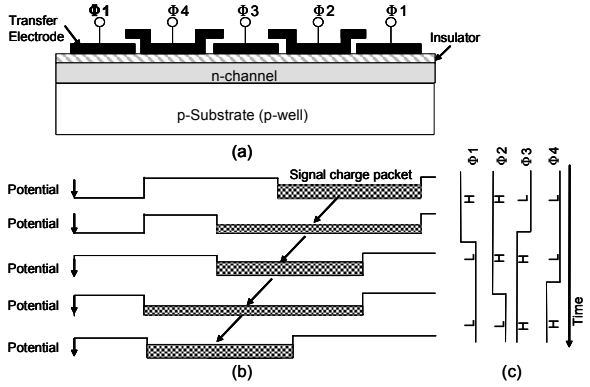

Figure 1. Four-phase CCD (a) Cross-section (b) Channel potential profiles under applying the 4-phase pulse set of (c)

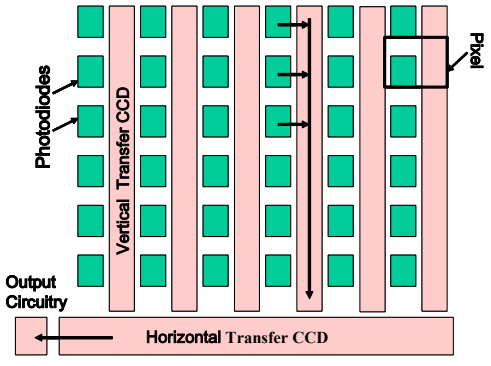

Figure 2. Block diagram of ITCCD

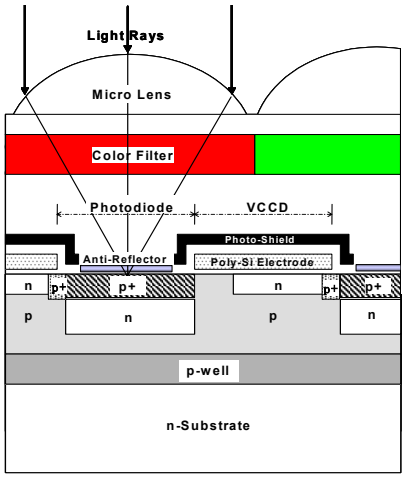

Figure 3. A pixel cross-section of ITCCD

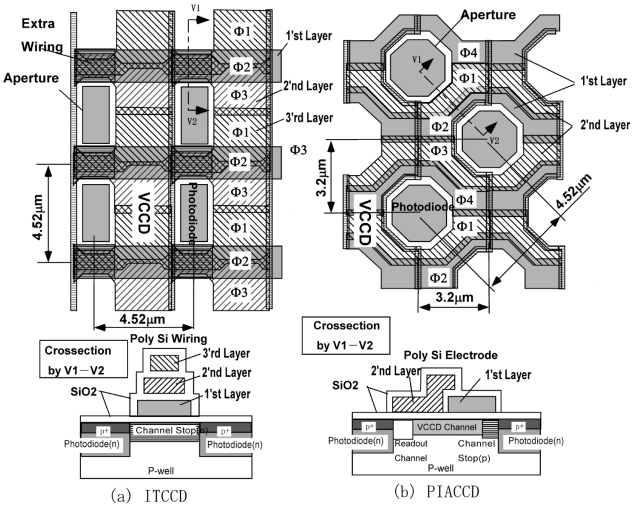

Figure 4. Pixel pattern layout of (a) ITCCD and (b) PIACCD.

Super CCD (Pixel Interleaved Array CCD)

As previously mentioned, ITCCD has been developed for the interlace scan applications such as camcorder. Recently, the main application field has shifted to DSC. In case of DSC application, the progressive scan is suitable, because it can shoot objects simultaneously without a precise mechanical shutter. As shown next, the pattern layout of ITCCD fits to the interlace scan, but it isn't basically suitable for the progressive scan, because the progressive scan essentially needs one transfer stage composed of three electrodes or more in a pixel. Figure 4 (a) shows the pattern layout of ITCCD. The extra wirings to supply transfer pulses to every VCCD electrode waste an active area in the pixel. For minimizing the wiring number, a three phase VCCD's are often used with a three layer poly-Si electrode as shown, which needs a sophisticated fabrication process. The pixel interleaved array CCD (PIACCD nicknamed as Super CCD) has been developed as an image sensor suitable for the progressive scan, which can be fabricated with a standard double layer poly-silicon technology.[2] The pixel pattern layout of PIACCD is shown in Figure 4 (b). As shown, the 4-phase VCCD's are composed of double layer poly-Si electrodes of Φ1, Φ2, Φ3 and Φ4. Each VCCD channel meanders along the photodiodes and borders on the next VCCD channel without extra-wiring, which has 1.5 times larger charge handling capability than the 3-phase CCD used in ITCCD. Curves in Figure 5 are the calculated relative active areas in ITCCD and PIACCD for pixel sizes with using the design rule shown in the figure. PIACCD enlarges the relative active area in the pixel by 1.3 times against ITCCD. The saturation voltage V_{SAT} of PIACCD is also enlarged about 1.3-times, because It is roughly proportional to this active area. In Figure 4 (b), the octagonal regions are photodiodes, and the gray area is an aperture opened above each photodiode. The 1.3-times enlarged equilateral photodiode has an advantage to gather more light rays passing through on-chip micro-lens than the oblong aperture of ITCCD.[3] The resolution characteristics of PIACCD differ from that of ITCCD.

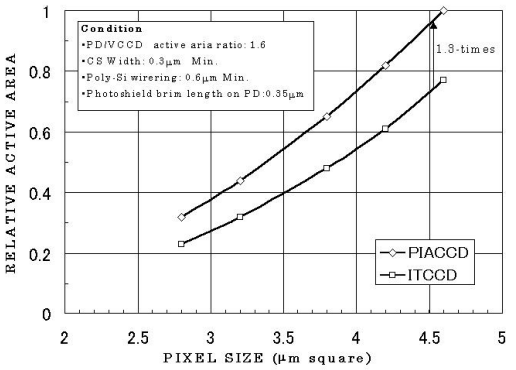

Figure 5. Relative active area for pixel size.

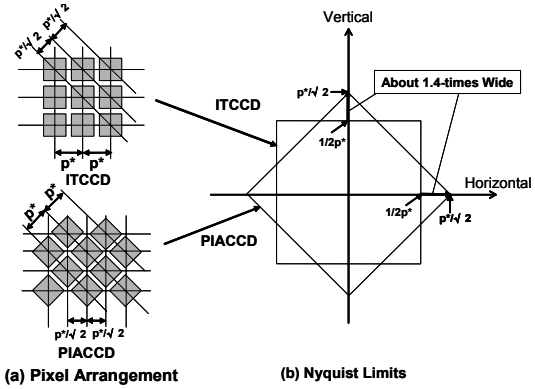

Figure 6. (a) Pixel arrangement and (b) Nyquist limits.

Figure 6 (a) shows the pixel arrangements of both the sensors. The horizontal and vertical pixel pitch in ITCCD is p, and that of PIACCD is $p/2^{1/2}$. As the pixel pitch means the spatial sampling pitches, the Nyquist limits of ITCCD and PIACCD are given as $1/(2p)$ and $1/(2^{1/2}p)$, respectively, in the horizontal and the vertical axes as shown in Figure 6 (b). It means that PIACCD heightens the

resolution by $2^{1/2}$ in the horizontal and the vertical directions. However, in the 45-degree tilted directions, this supremacy moves to ITCCD. On the other hand, it is reported that the human eyes are most sensitive for vertical and horizontal fine patterns, and the high frequency spatial power spectrum of nature scenes concentrate in the vertical and horizontal directions, as shown in Figure 7(a)[4] and Figure 7(b), So, the resolution characteristics of PIACCD fit both properties of the human eyes and natural scenery.

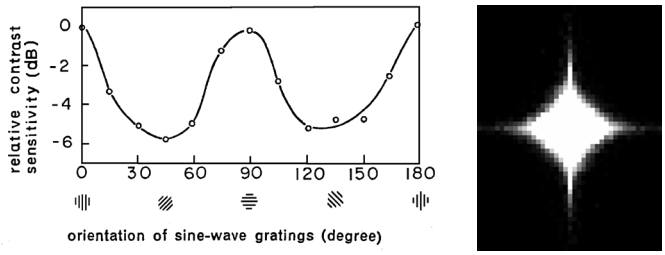

Figure 7. (a) Spatial response of the human eye, (b) Average spatial power spectrum distribution of about 500 scenes.

Current Development and Future Prospects

The development of CCD image sensor has been focused in increasing the pixel number to heighten the picture resolution. Generally, the pixel number increase accompanies pixel size reduction. The pixel size reduction lowers the sensitivity, and narrows the dynamic range by the same reduction factor. Already, the pixel size has became about 2μm squire, and a pixel number has increased over 5 millions which makes the resolution comparable to that of a film camera. Therefore, the pixel number competition will be on a final stage. Next, the new development themes will be discussed.

High Resolution Still and High Frame Rate Movie

In DSC system, it has become a sales point that the high grade movie such as high frame rate VGA can be played back on a TV or PC screen. As number of pixels increases over 3 millions, it becomes difficult to make the high grade movies only by extracting the video lines which can be easily done by reading out only the selected lines. But the line extraction doesn't decrease the horizontal pixel number in each video line. In case of 3M pixel PIACCD (2816 pixels (H) X 1060 lines (V)), the number of lines is decreased by half (530 lines) with every second line addressing. However, the horizontal pixel number is too large to make the high frame rate VGA movie. So, the horizontal pixel number reduction is the key technology to make the high quality movie. The architecture which can mix the same color signal packets in a horizontal line has been developed, which is composed of a CCD line memory (LM) bounded on the final VCCD stage and multi-phase HCCD, e.g. 4, 6 or 8-phase.[5] Block diagram of the PIACCD having the charge mixing circuitry is shown in Figure 8. The number of transfer stages of HCCD is reduced by half to transfer the mixed charge packets without increasing the HCCD driving frequency twice. Signal charge packets stored in LM are selectively transferred into HCCD by applying high level clock on the just linked HCCD electrodes. The charge packet is transferred only under the condition that LM is low level and the HCCD electrode is high level. The mixing process is shown in Figure 9. Each the first selected charge packet in HCCD is transferred toward left in the figure so far as the electrode bounded the LM site where the charge packet to be mixed is stored in. Next, the charge packets kept in the LM are transferred into the HCCD to be mixed with the partner charge packets. As a result, each color signal packet of G, R and B is mixed with the neighboring same color signal, and the signal sequence in the horizontal line becomes as 2G-2R-2G-2B-2G-2R-2G-2B----. With this process, a real time movie of 1408 pixels (H) × 530 lines (V) can be output at 30 fps with 36MHz data rate. The charge packet mixing is also applicable to the vertical mixing between video lines. Figure 10 shows an example of combination of both the charge mixing, i.e. vertical and horizontal. In this case, each the color signal output is enhanced by four times. So, the mixed signals have 4-times higher sensitivity, which is especially helpful to monitor and shoot dark scenes.

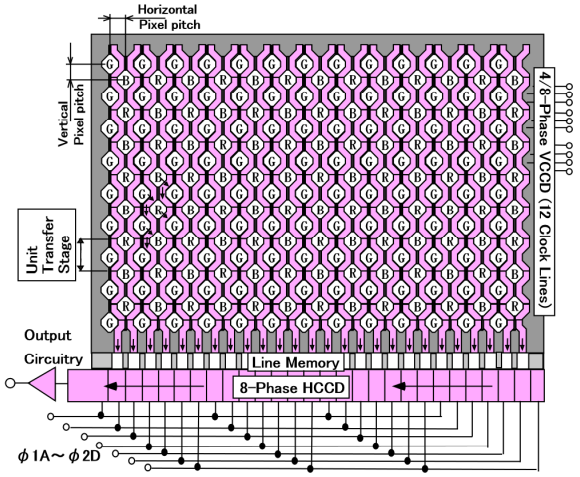

Figure 8. Block diagram of PIACCD having the charge mixing circuitry.

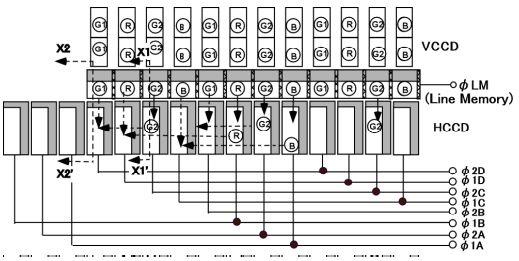

Figure 9. Charge packet mixing process.

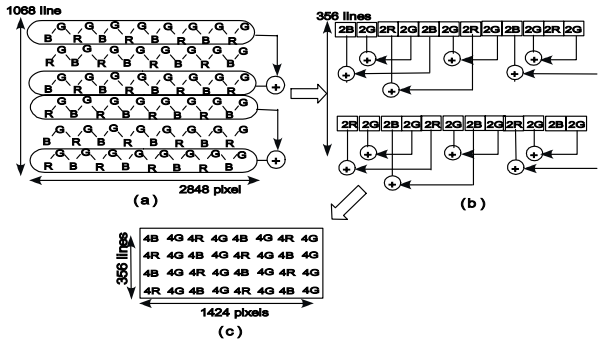

Figure 10. Combination of vertical and horizontal charge mixing.

Wide Dynamic Range and High Sensitivity

The dynamic range of the pictures taken by a DSC is extremely narrow in comparison with that of a film camera which has very wide latitude. The wide dynamic range for DSC means the wide saturation exposure which is provided with low sensitivity as shown in Figure 11. But the high sensitivity is the most important performance for image sensors, especially when shooting dark scenes. The solution that the wide dynamic range and the high sensitivity go together is in combining the high sensitivity characteristics and the low sensitivity characteristics. As an approach to realize this concept, a pixel having two photodiodes has been developed, where the photodiode is divided two areas, i.e. one for a high sensitivity large area and the other for a low sensitivity small area, as shown in Figure 12.[6]

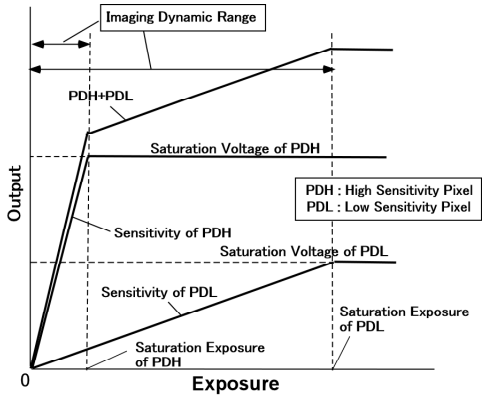

Figure 11. Principle of widening dynamic range.

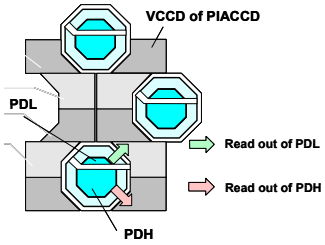

Figure 12. Dual photodiode pixels for wide dynamic range.

The imaging signals picked up at the high sensitivity photodiodes and that of the low sensitivity photodiodes are readout individually, and both of the images are compounded in the ISP with appropriate signal processing. The dynamic range is determined by the saturation exposure of the low sensitivity photodiodes. Another method, which arranges large pixels and small pixels alternately in an imaging area, has been also developed. In this method, the large pixels cover the high sensitivity and the small pixels contribute the wide dynamic range. The advantage of this method is in the adaptability to lens variations. So, it has been applied to the single-lens reflex (SLR) DSC named S3Pro.

Future Prospects

The pixel reduction will be continued as yet. The key technology is in how to keep the sensitivity, for example, an optimization of on-chip micro optical systems. The overlap-less electrodes technology (to be published), may be an answer, because it could make the on-chip optical layer thin, and it can make fine pitch CCD electrodes easily. The compatibility between a high resolution still and a high definition (HD) movie will be remarkable, which requires a new design to increase frame rate. The solution for this requirement may be in parallel signal readout technologies. Obviously, lowering the power dissipation is also very important. The key point to lower the power dissipation will be in the low voltage driving of CCD and the output circuitry. the CCD image sensor technologies hereafter will be expanded into various directions for enhancing performances and creating new functions to meet the system requirements.

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Author Biography

Tetsuo Yamada received B.S and M.S. degrees from Shizuoka University (1973), and Ph.D. in electronic engineering from Tohoku University (2002), Japan. In 1973 he joined Toshiba Corp., where he was engaged in development of CCD imagers. In 1996, he joined Fujifilm Microdevices Co., where he has continued his work on CCD imagers. He is currently deputy general manager in Electronic Device Laboratories, Fuji Photo Film Co. He received the national grand invention awards for the invention of “Solid-state imager with vertical overflow drain”, 1990, and “Walter Kosonocky Award” (2001) for the best paper of solid state imaging (IEEE Journal of Solid-State Circuits, Vol. 35, No. 12, pg. 2044, 2000). He is a member of the IEEE Electron Devices Society.