

An ASIC Design for Managing Thermal Inkjet Heater Array Chip with Integrated Power Drivers and Logic Addressing

Jian-Chiun Liou, Chun-Jung Chen and Wen-Chien Liu

K200/OES/ITRI

Industrial Technology Research Institute

Chutung, Hsinchu, Taiwan, R. O. C.

Abstract

A thermal bubble jet printhead design suitable for high speed and long life printing has been developed. It combines micromechanics including heating actuators, temperature sensor, channels and nozzles with a smart CMOS circuit including D Flip-Flops signal-processing along with bi-directional data transfer and 12V power amplifiers in a printhead chip. The asymmetric HV device structure (HV only apply on the Drain side, not source side) is recommended for lower Ron and higher current drive purpose. All of the jets of the printhead are controlled by very few input lines: a pulse shape (ENABLE), a data line (DATA), a bit shift clock (BIT SHIFT), a state clearing pulse, 5-volt supply for the logic devices, a higher voltage for energizing the heater resistors, and a ground line. The study for application-specific integrated circuit (ASICs) within the inkjet system controller has been finished. Some inkjet process calculations are sufficiently time-urgent and/or extensive that it makes sense to design an ASIC to manage these tasks, we have fabricated a chip size 9000um×8000um printhead beyond 400 nozzles have a 5 pl. ink drop volume.

Introduction

The major customer requirements for printing system are high print quality, high speed, available colors, low cost, reliable hardware, and excellent software support. Thermal inkjet printing has several advantages compared with other technologies; low cost, high resolution, low noise, ease of color printing, and portability. The inkjet printhead is the key element in the inkjet printer because it determines the print quality, print speed, and maintenance cost.

In this study, we propose a new integrated fabrication method for the smart multiplexer thermal inkjet printhead utilizing silicon micromachining techniques. The printhead has beyond 400 nozzles. To provide a multiplexed function requiring only a limited number of line between the printer and print head, resistor current flows through a voltage line

and a ground line shared by other resistors in its quadrant. The resistors are individually addressable to provide unlimited pattern permutations, by a serial data stream fed from the print head. Here a shift register is employed to shift a token bit from group to group of AND gates drive individual power switches to individually fire a jet, Jet selection is thus a combination of the shift register selection of its group and the data for that group. Such an arrangement allows one data line to the TIJ device to provide data to all of the jets. The TIJ method has some advantages, such as: it is suitable for high speed printing because it is easy to array the heater and nozzle in high density, and the cost per jet is low due to the decrease of the number of components because the logic control circuit is easy to integrate in the head chip.² To achieve high speed quality printing, high resolution, small ink drop, and long array TIJ printhead is fabricated by using LSI process and Si micro-machining technology, Figure 1. Integrated multiplexer inkjet chip level process flow, with a current pulse of less than a few microseconds through the heater, heat is transferred from the surface of heater to the ink. The ink becomes superheated to the critical temperature for bubble nucleation, for water-based ink, this temperature is around 300°C. When the nucleation occurs, a water vapor bubble instantaneously expand to force the ink out of the nozzle.

Design of Multiplexer Inkjet Chip

Integration of logic function is enabling TIJ-based products to move ever further up-market.³ Figure 2 illustrates the concept of the smart printhead. The depicted integrated circuit TIJ transducer array serves beyond 400 jets and includes data interfacing, jet addressing, drop generation power pulsing, and bidirectional operation. The chip also includes output features that facilitate the electronic management of an assembly of multiple chips into larger arrays. The illustrated TIJ chip design allows beyond 400 jets to be operated with less than ten input lines.⁴

The logic circuit is first translated into an inkjet chip CMOS circuit and the initial layout is done. We design and

analyze the circuit for DC and transient performance by using the circuit-level simulation program, SPICE, and then compare the results with the given design specifications.

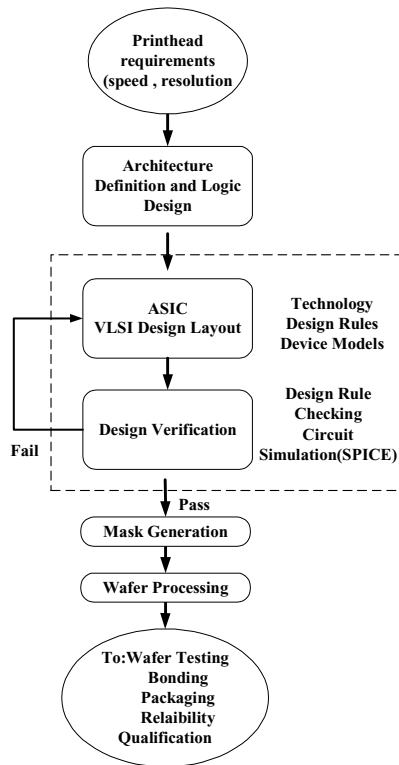


Figure 1. Integrated multiplexer inkjet chip level design flow

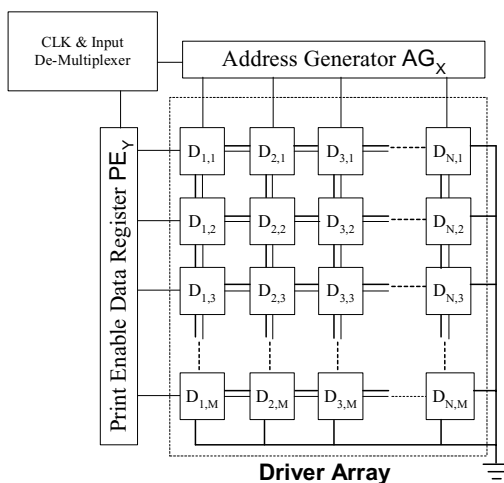


Figure 2. The concept of the smart printhead

Fabrication Process

A smart CMOS circuit including D Flip-Flops signal-processing along with bi-directional data transfer and 12V power amplifiers in a printhead chip. The input signal include "DATA · CLK1 · CLK2 · CTRL · SETB". Design flow is more complex than traditional driver on inkjet chip, the research step is follow : first, ASIC design for addressing jets, second, simulation for multiplexer in inkjet chip, final, according to simulation device size result for chip layout, then tape out pre-process for CMOS circuit and post process for inkjet process. The smart printhead total process flow is shown in Fig 3. It is based on a 0.5 μm CMOS process. The physical design rules of 0.5 μm 2P2M 12V/12V, (Double Poly Double Metal, V_{ds}/V_{gs}) high voltage process and MIXED-MODE process. The asymmetric HV device structure (HV only apply on the Drain side, not source side) is recommended for lower Ron(turn on resistance of MOSFET) and higher current drive purpose.⁵ The NMOS devices in the n-well technology are formed in the lightly doped p-substrate, while the PMOS devices are formed in the more heavily doped n-well. The starting material is a heavily doped <100> p⁺ wafer with a thin (5-10 μm), lightly doped p-type epitomical layer at the surface. For AlSiCu deposition and patterning processes as metal 1, then intermetal dielectric deposition and via patterning, TaAl (29 Ω/\square) for the heating resistor and Al(7000 \AA) for the interconnection line were sputter-deposited and patterned by wet chemical etching. Si₃N₄ (4000 \AA)/SiC (2500 \AA) and Ta (4500 \AA) were then deposited by plasma-enhanced chemical vapor deposition and sputtering, respectively. The heater actuator sides of the firing chamber and the ink feed channel are defined by a polymer barrier layer. This barrier layer is preferably made of an organic polymer plastic that is substantially inert to the corrosive action of ink and is conventionally deposited upon substrate and its various protective layers. To realize the desired structure, the barrier layer is subsequently photolithographically defined into desired shapes and then etched. In this study the barrier layer has a thickness of about 15 micrometers after the printhead is assembled with the orifice plate.⁶

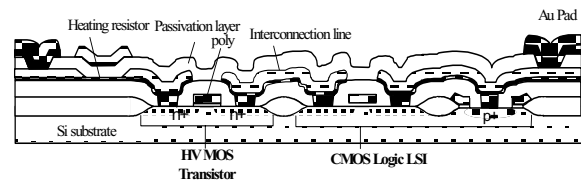
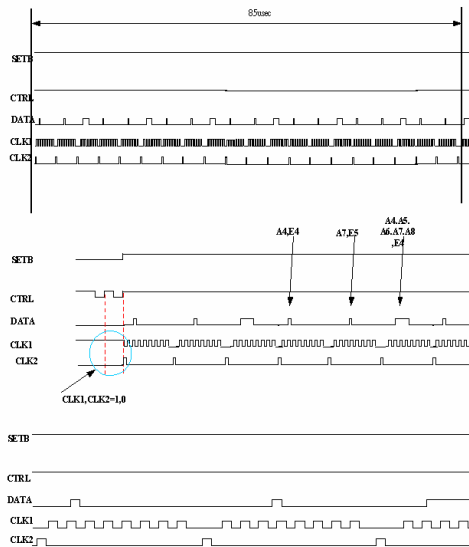


Figure 3. Fabricated a printhead chip

The digital circuit is realized by 0.5 μm 2P2M CMOS technology with 12V power supply. The acquisition time of SPICE simulation approaches 85 μsec , as shown in Fig 4. All jets will firing must 85 μsec , and SETB, CTRL, DATA, CLK1, CLK2 signals control addressing jets.



Note. SETB: initial set up condition
CTRL: type mode set up
DATA: select nozzle information
CLK1: scan DATA
CLK2: latch DATA (series in and shunt out)

Figure 4. SPICE addressing simulation

Output stage of the multiplexer inkjet printhead SPICE Simulation program. It is important for MOS Driver monitor, I-V curve. The program is show as:

```
* this is a circuit used by logic055 model tt
***ext oes
.options post=2 probe
.lib '05hv12v10.1' TT_12A
* Definition for project OPPAD
.PARAM W=10u H=10u
R1I32 OUT VDD7V R=0
M1I35 OUT OP 0 GND NA12V L=1.8U W=100U AS='W*H'
AD='W*H' M=6
V1 VDD7V 0 7V
V2 OP GND 12V
.DC V1 0 12 0.01 v2 0 12 1
.PRINT I(M1I35) I(R1I32)
.MEASURE DC IRR PARAM='(V(OUT))/I(R1I32)'
.MEASURE DC RMOS PARAM='V(OUT)/I(M1I35)'
.END
```

Figure 5 is shown MOS I-V Curve SPICE simulation result. It is a power MOS device character.

In the simulation, used logic and high voltage model to fit the logic CMOS device and MOS driver device W/L size, must to find optimal size.

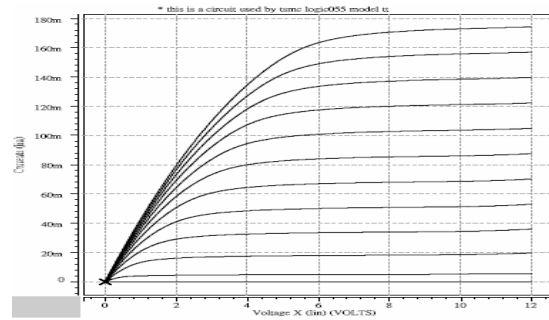


Figure 5. MOS I-V Curve SPICE simulation

Performance Comparison

In this study, the most different from traditional direct drive type and driver on chip type function work is the belong printer logic signal process down load to the inkjet printhead. Many advantage is shown the performance, include reduce signal pulse delay time, and enhance the nozzle, in opposition, enhance the resolution of integrated multiplexer in inkjet printhead. This comparison shows that the developed multiplexer have improved performance for several aspects, among them to address more and more jets for few connect pad, to increase the nozzles of printhead and to enhance print speed. During the testing, the multiplexer inkjet printhead ejected more than 50 million droplets continuously. No noticeable cross-talk among chambers was observed during the ejection testing for the multiplexer inkjet printhead. However, further experiments need to be carried out for the detail study of the micro-flow phenomena in the micro-chamber, for the extended reliability test and to control more and more jets for few connect pad to fit high print speed.

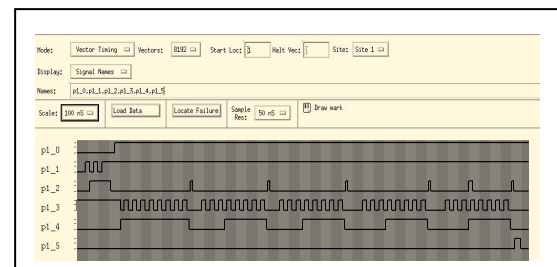


Figure 6. The signal analysis observe

In the signal analysis equipment, we observe the ASIC input and output relationship is shown in Figure 6. The output signal is match to the designed function. A input signals waveform concept that can be used with TIJ to address each jet. The depicted integrated circuit TIJ transducer array serves 432 jets and includes data interfacing, jet addressing.⁷ The fabricated printhead Figure 7. Current-Voltage characteristic is shown in Figure 9, we illustrated current instability phenomenon by measuring IV characteristics using different bias sweeping methods. For

High Voltage NMOS Driver forward measurement from $V_{ds}=0V$ to $V_{ds}=20V$ at each gate bias, while the V_{gs} was varied from $0V$ to $12V$. So, to maintain considerably that V_{th} as follow. Figure 11 is shown the V_{th} (sub-threshold) of a enhancement-mode n channel MOSFET drive.

- (1) MOSFET at sub-threshold region I-V characteristics:
when a device operated at sub-threshold region $V_G = V_{th} - (V_{th} - 0.6)^8$

$$I_D = \frac{W}{L_{eff}} \mu C_i \left(\frac{n_i}{N_A} \right)^2 \left(\frac{a}{\beta^2} \right) (1 - e^{-\beta V_{D_s}}) e^{\beta \phi_s} (\beta \phi_s)^{\frac{1}{2}}$$

If V_{th} not enough, I_D leakage increases exponential once a q/kT ($=0.026V$).

- (2) The temperature will decrease V_{th} of device.
In a printhead chip, $N_B = 3 \times 10^{15} \text{ cm}^{-3}$, temperature effect $(dV_{th}/dT) = -3 \text{ mV}/^\circ\text{C}^9$
- (3) ESD leakage of electricity current at least lower 0.5 A @ $V_D = 10V$, or an off case more than $200k \text{ V}$.
- (4) The lowest V_{th} calculating: Swing 90 mV/dec , the V_{th} of at least 0.5 (Swing area range) $+0.9$ (temperature effect) $= 1.4V$ satisfies the above demand.⁸
- (5) To suggest 1: $V_{th} > 1.4V$ and in the meanwhile, $I_{off} \leq 0.5 \text{ A}$ @ $V_D = 10V$, $V_G = V_{th} - 1.4V$
- (6) To suggest 2: estimating V_{th} Implant: $B_{11} 3e12 \text{ cm}^{-2}$, $25keV$, Dry-SiO₂ drive-in V_{th} implant that will cause “n” to reduce, to make the R_{on} of MOS rise.

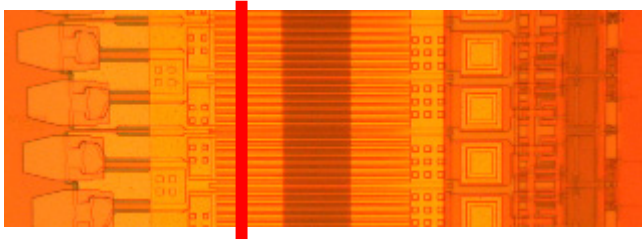


Figure 7. Fabricated a printhead chip

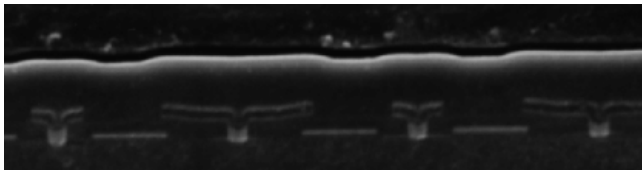


Figure 8. SEM cross section of MOSFET driver

The MOS driver in inkjet printhead that we have designed Drain、Source、and Gate, The drain will be supply high voltage 12 V , so the metal area is bigger than source, the SEM cross section of MOSFET driver is shown in Figure 8, Figure 9. is a multiplexer inkjet head chip test key.

Figure 10 is shown a output characteristic of a enhancement-mode n channel MOSFET drive, Figure 11 is shown a V_{th} (sub-threshold) of a enhancement-mode n channel MOSFET drive, the value is match to simulation

result. In droplet observation, the test results described of the multiplexer inkjet printhead verify that the problem of satellite droplet has been eliminated as shown in Figure 12. Thermal bubble droplet ejection sequence measure, Delay Time on from $2-2.8 \mu\text{sec}$ ~ $6.4-7.8 \mu\text{sec}$ at power voltage $6-8 \text{ V}$.

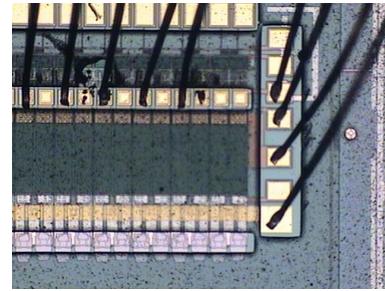


Figure 9. Multiplexer Ink-Jet Head Chip test key

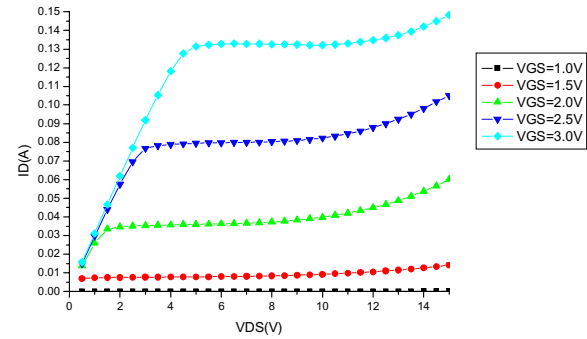


Figure 10. Output characteristic of a enhancement-mode n channel MOSFET drive

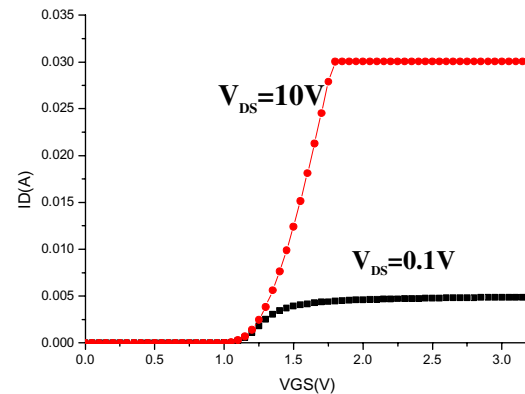


Figure 11. V_{th} (sub-threshold) of a enhancement-mode n channel MOSFET drive

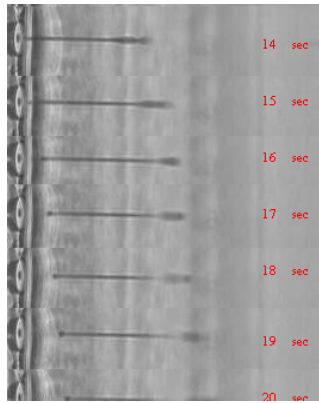


Figure 12. Thermal bubble droplet ejection sequence

Conclusion and Future Works

A smart long-lifetimes bubble jet printhead has been proposed and demonstrated to operate. The multiplexer printhead integrated inkjet nozzle arrays by a standard CMOS process and using micro machining technology (MEMS). Integration of CMOS and enhancement mode devices, power switches, and the TIJ heater transducer allows logical functions to also be performed on-chip. This capability is used in the illustrated design to address individual jets with even fewer input lines than matrix addressing. Only eleven input lines are needed to address a large number of jets, for example, jets even more and high print speed.

Reference

1. M. O'Horo, J. O'Neill, E. Peeter, S. Vandebroek, "Micro Electro Mechanical System Technology for Commercial Thermal Inkjet Document Output Products", Proceedings Eurosensors X, pp. 431-435, September 1996.
2. R. R. Allen, J. D. Meycr, and W. R. Knight, "Thermodynamics and hydrodynamics of thermal ink jets," Hewlett-Packard J., vol. 36, no. 5. pp. 21-27, May 1985.

3. J. Chen and K. D. Wise, "A high-resolution silicon monolithic nozzle array for inkjet printing," IEEE Trans. Electron Devices, vol. 44, no. 9, pp. 1401-1409, Sep. 1997.
4. Xerox Paolo Alto Research Center, "Thermal ink jet technology" circuit & devices, JULY 1997, 8755-3996/97/\$10.00©1997 IEEE.
5. W. Hawkins et al., Device Research Conference Digest, 1990, 1992.
6. T. Courtney, R.E. Drews, V. I. Hull, D. R. Ims and M.P. O'Horo, "Print Element for Xerox Thermal Ink Jet Print Cartridge" in Color Hard Copy AND Graphic Arts III, J.Bares (Editor), Proc. SPIE Vol. 2171, pp.126-130(1994).
7. P.H. Chen, W. C. Chen, and S. H. Chang, "Bubble growth and ink ejection process of a thermal ink jet printhead," Int. J. Mech. Sci., vol. 39, no. 6, pp. 683-695, 1997
8. S.M.Sze, Physics of Semiconductor Devices, 2nd Edition, pp.470-474.
9. ibid, pp.451-453.
10. Jian-Chiun Liou, Chien-Hung Liu, Chun-Jung Chen, "A Bubble-Jet MEMS printhead-Integrated with CMOS De-Multiplexer", The 15th Annual IEEE/SEMI Advance Semiconductor Manufacturing Conference and Workshop, pp. 413-419, May. 2004.

Biographies

Jian-Chiun Liou joined the Printing technology Development and Manufacturing Section of OES/ITRI in 1999. He received his M.S. degree from Institute of Electronic of National Taiwan Ocean University, Taiwan. He interest lies in the ASIC design, MEMS technology and integration of inkjet printhead processes.

Chung-Jung Chen joined the Printing technology Development and Manufacturing Section of OES/ITRI in 1990. He received his M.S. degree from Department of Power Mechanical Engineering of National Tsing Hua University, Taiwan. He interest lies in electro-photography, media handling of printer and magnetic damper. He is the department manager of printing Device Department in OES/ITRI.