Method For Forming Cu Metal Wires by Micro-dispensing

Part II: Application and Testing

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Abstract

Classical electrically conductive pattern manufacturing method likes screen-printing and photolithography are complex and long time delivery. A method for forming metal wires by directly micro-dispensing pattern is provided, which includes the steps of self-assembly surface treatment, micro-dispensing catalyst pattern on the substrate, and forming metal wires by electroless plating. This methodology has been realized for an 8051 single chip circuit with metal lines less than 100 μm wide. The result has been verified by IPC 6013 standard for flexible substrate. After six thermal shock cycles from room temperature to 288°C and three runs of hot oil tests at 260°C, the circuit can still operate satisfactorily at 12 MHz clock frequency of LED text display device. In this study, an imposing vibration method during ink-jet printing of catalyst is also proposed to reduce the line width and improve blurring behavior. The variation of line width was improved from ±10% to ±3% in characteristic frequency operation.

Introduction

In the past, screen-printing and photolithography have been the predominant methods of imaging in PCB manufacturing processes. These techniques have served the industry well and provided the desired image resolution at an acceptable cost. However, these methods suffer from the drawback of being analogue processes and hence require conversion from a digital data file to converted printable image via initial production of a screen or photo tool. This adds cost and time delays to the preparation of boards particularly for prototype and short run board production.

Direct-write technologies offer the potential for low cost materials-efficient deposition of metal. Inkjet printing, as a derivative of direct-write processing, offers the additional advantages of low capitalization, very high materials efficiency, elimination of photolithography, and non-contact processing.[1]

Some prior report had been on the inkjet printing of metal organic decomposition inks with nano-particle additions or organic metal precursor. Near-bulk conductivity of printed and sprayed metal films has been achieved for Ag and Ag nanocomposites,[2] But this kind of method faces the challenge of poor adhesion between metal film and substrate, and typically it needs a high temperature (~300C) sintering post-process to forming the thin film metal with good electric characteristics. It limits the application area, especially for flexible substrate.

The novel process is developed to form metal wires, includes the steps of appropriately treating the surface properties of the substrate to improving the adhesion between the metal and substrate; microdispensing the catalytic pattern for forming metal film, and depositing metal on the catalytic pattern on the surface of the substrate by an electroless plating process. In this study, we successfully demonstrate an ink-jet forming circuit by this process for a 12MHz, 8051 single chip operations. The ink-jet forming circuit is proven to have excellent adhesion and good conductivity for various substrate applications (e.g., BT, PET, Glass, FR-4, PI). Even though after extreme thermal cycle thermal cycle (288°C, 6 times) and hot oil test (260°C, 3 times), the metal circuit still exhibited good adhesion and electric characteristics.

For the requirement of high-density circuit, the via-hole diameter varied with the circuit density. Typically, the diameter of via hole is about 100 μm for screen-printing fabrication. However, as the via-hole diameter decreases further down to 30-50 μm, for the high-end application of chip on flexible (COF), screen-printing is no longer suitable for its low yield rate. In this study, we also introduce the feasibility of forming metal in inner wall of via-hole by ink-jet printing.

Fabrication Process

The ink-jet system followed Yang's apparatus and recipe.[3] Where the patterning method includes the steps of providing a substrate; microdispensing a catalytic pattern for forming

metal wires; and depositing metal on the catalytic pattern on the surface of the substrate by an electroless plating process. In order for the metal to adhere onto the substrate and to improve the surface properties of the substrate, the substrate surface has to be appropriately treated (i.e. modification treatment) before microdispensing. The process changes the surface properties by forming a self-assembled monolayer (SAM) interface on the substrate surface. The substrate surface is thus endowed with selective absorption abilities and can effectively absorb a catalytic agent. Detail fabrication process can refer to Yang.[3]

Result

Figure 1 is an 8051 single chip circuit made by this SAMs-Ink Jet Catalyst-Electroless Plating fabrication process. The circuit image was designed by commercial software PROTEL 99. It presented the circuit pattern on FR-4 substrate, and had soldering the electric components and 8051 chip on this ink-jet fabrication substrate. This board can input letters and show them in a LED display.

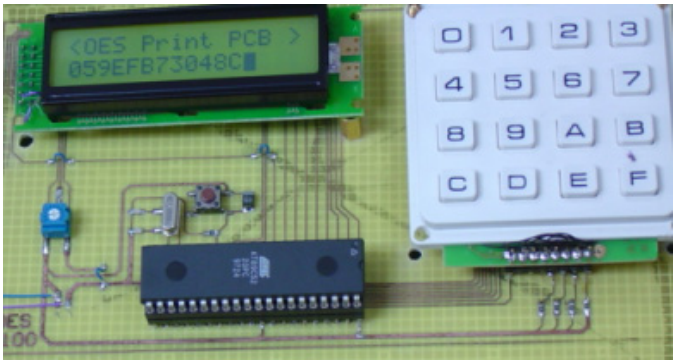

Figure 1. A printed circuit for 8051 single chip with input and LED display. Circuit pattern that had ink-jet catalyst and electroless plating process. Function testing of 8051 chip, the input letters can display in a LED display.

IPC 6013 Standard Testing

IPC 6013 covers qualification and performance requirements of flexible printed wiring. In this standard, the flexible printed wiring may be single-sided, double-sided, multilayer, or rigid-flex multilayer. All of these constructions may or may not include stiffeners, plated-through holes, and blind / buried via. In this study, the ink-jet printed circuit in Fig. 1 had verified follow the testing standard of IPC 6013, as shown in Table 1. To verify the adhesion capability, the 3M-tape peeled at vertical direction presented excellent adhesion between circuit and flexible substrate, no trifles left at tape was observed. An important requirement of circuit quality is the resistance of thermal cycle, especially during the soldering procedure. Here the thermal stress tested in 288°C, six times and immersed the circuit in 260°C hot oil three times also approved. The details can see Table 1.

Table 1. An Environmental Testing Results Follows the IPC 6013 Standard for Fig. 1 Circuit Pattern.

Testing Item	Results	Testing Conditions
Peeling test	Pass	3M tape
Thermal stress	Pass.	288°C, 6 times
Hot oil test	Pass	260°C, 3 times
Soldering test	Pass	Soldering tin on circuit
Peeling stress	Excellent adhesion which can not peel the metal line to be tested	

An important requirement for electric circuit is the small edge growth along metal line. Observed in high optical magnification for Fig. 1, we found the edge blurring was exist, as indicated in Fig. 2. The essential physics explained by Deegan's[4] theory was that as a drop landing on substrate, a pinned contact line induces an outward, radial fluid flow when there is evaporation at the edge of the drop. The contact is pinned then there must be a flow that replenishes the liquid that is removed from the edge. Under this assumption for this study, we also found metal nuclear will largely accumulate at line edge along the printing line direction as the catalyst drop dried and make non-uniform reduction reaction rate of copper along line profile in electroless plating. As shown in Fig. 2, it was observed that the copper line edge has thicker edge forming because the contact line of printing catalyst was pinned at the line edge, and made more metal nuclear accumulated to cause faster reduction reaction in plating.

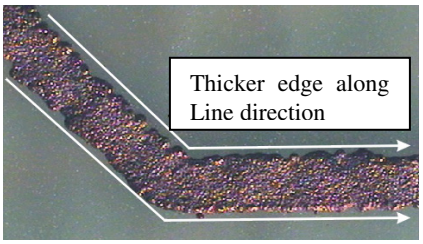

Figure 2. The growth behavior observed in line edge.

To overcome this problem, we used an actuator device to vibrate the drop surface and make opposite external force to the capillary force, which drives the solute separate at periphery. Besides, this acoustic streaming behavior will change the vapor pressure near drop surface. It resulted faster evaporation rate and reduced the probabilities of particles toward to periphery boundary, and led to an excellent flat polymer film[5] and small variation in the line width. Figure 3 show the relation between the line width variation and the frequency of the actuator. After imposing vibration energy during ink-jet printing of catalyst, the line width reduced from 172 um down to near 140 um in same process. Besides, the blurring behavior was also inhibited. The variation of line width was improved from ±10% to ±3%, as marked circle in Fig. 3.

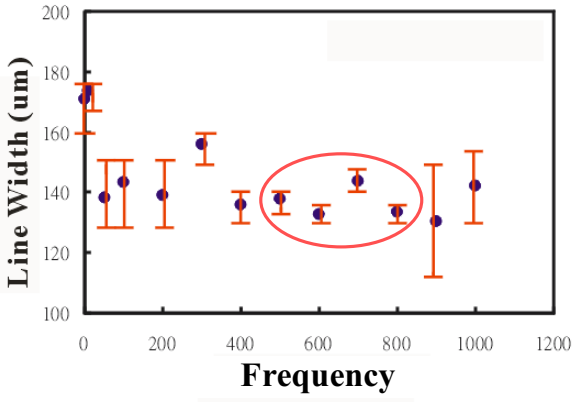

Figure 3. The line width variation varies with different frequency.

Based on the Yang's process and the vibration improvement method, Figure 4 shows the high-density circuit board. In Fig. 4, the major pattern composed by circle pad, square pad, and narrow metal wire. Where the copper metal line was formed by ink-jet catalyst, and then electroless plating operated on the FR4 substrate. The line width is less than 100 μm and the thickness is near 12 μm. Overall fabrication time was only about three hours, most of the time was spent on the thickness required, for example, 2 hrs for about 12 μm. Key factors are the plating bath concentration, bath temperature, pH stability, additives, and plating time. In our work, we kept all the factors constants except the plating time.

To extend the application, how to form the metal layer on the via-hole inner wall by micro-dispensing method was an important consideration. For the high density multi-layer circuit board, the via hole diameter will decrease down to 30-50 μm in future, the screening printing is not suitable for its low yield rate. Emerging process method is urging for market expectation. The steps of forming the metal layer of via holes are the same as the steps of forming the metal wire, except the catalyst patterning method. In the beginning, we have verified the feasibility of forming metal in the inner wall of via-hole by ink-jet printing process. In the Fig. 5, the metal layer has successfully formed in the inner wall of via hole whose diameter is from 0.2035 mm to 0.073 mm. Based on the diameter of the via hole and the depth of the hole, the nozzle size should be applicably chosen to prevent overflow or underflow. Simultaneously, accommodating drop number is selected to get the optimum result.

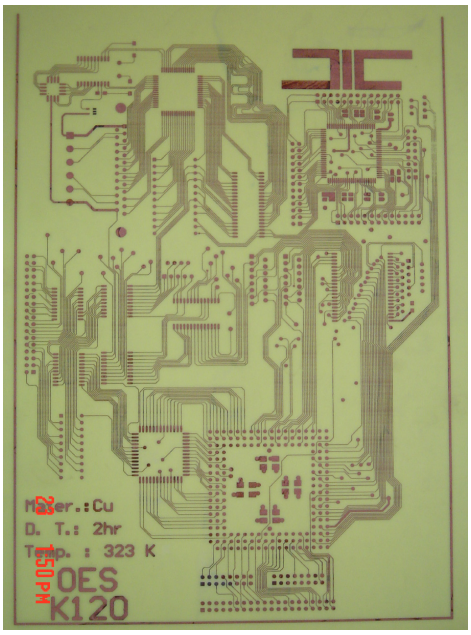

Figure 4. A flexible high-density circuit where the substrate was FR-4.

The ink-jet printing method could successfully form the metal layer of via-hole, and connect the front side and back side of substrate. However, the flatness around the hole need more study for improving its reliability. In this paper, the ink-jet printing process has proved the potential to form inner metal film for via hole. Design new printing route to prevent the ink accumulation and tuning the electroless plating process to improve the plating anisotropy growth problem are further study directions.

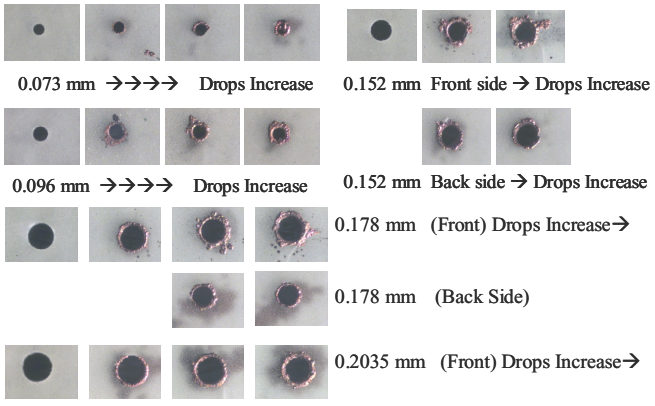

Figure 5. The metal layer have formed in the inner walls of the via holes with different diameters.

Conclusion

In summary, we demonstrated the patterning of multilayer electric circuits on various flexible substrates via combining three technologies: the self-assembly of polyelectrolytes, the ink-jet printing of catalyst and the electroless metal plating. This study found that this novel modification procedure gave excellent selection capability and adhesion with different substrates. And this method is versatile and inexpensive, produced highly conductive metal lines, and the thickness can be controlled from sub-micro to about 35 μm. To our knowledge, this is the first time that such a technology has been successful in forming an electronic circuit passing IPC standard, and shown to successfully drive a commercial 8051 chip.

Further study will focus on solving the thin film morphology problem, to prompt the electric characteristics. The key factors considered in the future are the catalyst distribution during printing, the interface property design between the PAH layer and catalyst, the drying mechanism of the catalyst, and a more fine tuning control over the electroless plating parameters. And, another important point is the ink-jet stability control. Reducing the satellite drops and the drop position deviation could significantly improve the line width variation and reliability of the product.

References

1. K.F. Teng and R.W. Vest, *IEEE Electron Device Lett.*, 9, 591 (1988).
2. Thshihiko Oguchi, Keiki Suganami, Taizo Nanke and Toshikatu Kobayashi, "Formation of Precise Electrically-Conductive Pattern Using Metal Colloid I-J ink", *NIP 19: International Conference on Digital Printing Technology*, 656-659 (2003).
3. *Ming-Huan Yang, Wanda W. W. Chiu, Jane Chang & Kevin Cheng,* "Method for Forming Cu Metal Wires by Microdispensing Pattern, Part I: Self Assembly Treatment & The Ink-Jet Process", accepted by *NIP20*: International Conference on Digital Printing Technologies, 2004.R. D. Deegan, *Phys. Rev. E 61*, 475 (2000).
4. Katsuyuki Morii and Tatsuya Shimoda, "Film Formation by Inkjet Behavior of Inkjet Droplets", *Japan Surface Science*, 24(2), 90-97 (2003).

Biography

Wanda W. W. Chiu received her Master degree in Mechanical Engineering from National Cheng Kung University in 1996. She is now a system integration engineer in the Printing Technology Division, Opto-Electronics and Systems Laboratories of Industrial Technology Research Institute at Taiwan. Her work has primarily focused on the industrial ink-jet printing processes development, especially in color filter, PWB, MEMS device fabrication by ink-jet printing. E-Mail : wandachiu@itri.org.tw