A Study of Electrophotography Process for Manufacturing Printed Circuit Board

Hideo Aoki, Naoko Yamaguchi and Chiaki Takubo
Toshiba Corporation, Kawasaki-shi, Japan

Koji Imamiya, Toshiaki Yamauchi and Hiroshi Hashizume
Toshiba TEC Corporation
Mishima-shi, Japan

Abstract

Cost down of printed circuit boards (PCB) is one of critical issue for electronic components and semiconductor packages. A new wiring process using electrophotography technology is reported in this paper. The new process provides mask-less manufacturing and cost down capability for PCB. Cu wiring patterns can be formed by printing toner including metal fine particles and electroless plating in which metal particles work as catalyst. Insulating layer is also available in the same way by resin toner without metal particles. Repetition of patterning of insulating layer and wiring layer builds up multi-layer structure of PCB.

The optimization of electrostatic charge of toner including metal particles and quality of electroless plating on patterned layer is needed. Therefore, relationships between charge of toner, electroless plating ability and contents of metal particles are clarified. Furthermore, forming insulating layer and multi-layer structure is investigated. Using samples made by the new technology, some basic reliability evaluations for PCB and soldering demonstrations are also carried out.

Electrophotography process with electroless plating is confirmed to have a good ability for mask-less PCB manufacturing in electronic component applications.

1. Introduction

The percentage of PCB cost in electronic components is increasing recently because of the needs of finer tracing design of PCB forced by higher density and miniaturization of electronic components. Therefore, cost down of PCB will greatly affect product competitiveness of electronic components. One of conventional manufacturing process of fine tracing PCB is known as “fully additive method”. In fully additive method, photosensitive resin applied on base substrate firstly. Plating resist for desired circuit pattern is developed with the corresponding exposure-mask. After depositing catalyst, electroless plating forms metal conductive layer. Finally by lifting off the plating resist, circuit pattern is obtained. In this process, many exposure-masks are needed because each layer needs mask. They have severer impact on cost and turn around time, from circuit design to product.

In terms of investigation of mask-less circuit patterning, inkjet and electrophotography technology have been reported with metal particles such as silver ink.[1,2] In general, inkjet process needs control of wettability and adhesion on base material or substrate, sometimes it may needs certain special surface treatment. On the other hand, electrophotography process has some difficulties because it needs management of Coulomb force especially in case of direct metal toner printing. Not so many researches with electrophotography approach have been reported.

In both technologies, direct metal wiring with metal particles provides relatively higher resistance as circuit trace and relatively lower adhesion to substrate comparing with conventional PCB. Thus there have been some limitations of direct metal printing to cover electronic components widely.

2. New Manufacturing Process of Printed Circuit Board

New wiring process, this paper proposes, is not direct metal printing method but printing toner containing catalyst for electroless plating. Toner consists of binder resin in which metal fine particle dispersed. Metal particles work as plating catalyst, in other words, seeds for electroless copper plating. By adopting electroless plating, it becomes available that circuit resistance and adhesion strength to substrate is almost same as conventional PCB. In addition, it could be taken advantage of electrophotography technology in order to mask-less manufacturing.

Figure 1 shows outline of the process flow with electrophotography and electroless plating. First step is printing wiring pattern on base sheet with toner including metal particles (seed toner). Metal particles exposed from resin surface of printed pattern have a function as seeds in electroless copper plating.

With the seeding layer, electroless copper plating forms conductive layer on the pattern. In next step, "insulator toner" with no metal particle is printed with electro-photography again. In order to obtain building up multi-layer structure, steps of wiring and insulating layer formations are repeated.

Advantages of this process are mask-less by using electrophotography, high electrical conductivity by electro-less plating, high adhesion strength by resin binder and availability of multi-layer structure.

3. Optimization of Cu Included Toner

To estimate availability of electrophotography for PCB, it is necessary to evaluate the tribo-electrical properties of seed toner including metal particles and the plating ability on printed seeding layer.

Figure 2 is SEM micrograph of seed toner. The binder resin of seed toner is epoxy resin including metal fine particles dispersed in. The metal particles work as seeds of electroless plating. Since availability of soldering is one of the major requirements of PCB use, thermal stability and adhesion strength at high temperature are important. Therefore, thermosetting epoxy resin with high Tg was selected as effective solution for PCB. From the group of metals having catalysis with Cu electroless plating, Cu was selected by reason of high catalystic activity and lower cost. In the evaluations in this paper, imaging experiment was carried out using 600dpi Multi Functional Peripherals (MFP) for office use with two-components dry toner. Toner is made by mixing and grinding process. Developer is made from toner and ferrite carrier.

3-1. Copper Contents of Seed Toner

Contents of Cu fine particles in seed toner is supposed to affect charging characteristic of toner and electroless plating quality.

Figure 3 shows experimental relationship between Cu contents and charge of toner per unit mass. As a result, lower Cu contents provide larger charge of toner and charging quantity is found to be enough for printing even at 70 wt%.
Quality of electroless plating is estimated with measuring sheet resistance of Cu plated pattern. Two different shapes of Cu particles dispersed in seed toner are evaluated. One is sphere and another is flake made by forging of the sphere particles. Figure 4 shows that the sheet resistance of sphere is higher than that of flake. In case of sphere, electrical failure (open failure) is observed at 20 wt% Cu contents. It is considered that flake has larger surface area and maximum length (effective diameter) than sphere shape. With both shapes, lower Cu contents tends to have higher sheet resistance. Lower Cu contents gives longer distance between dispersed seeds particles. In addition, Cu deposition thickness is mostly determined by plating time. Consequently, plating layer could not be continuous when distance between seeds particles is longer than the deposition thickness.

According to the experimental results, charging quantity of toner and plating quality have optimum trade off relationship with Cu contents. Making condition of seed toner for further evaluations is fixed 50 wt% Cu contents with flake shape particles.

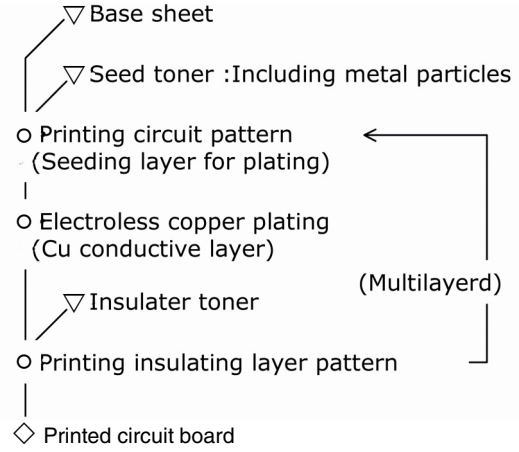


Figure 1. New Process Flow

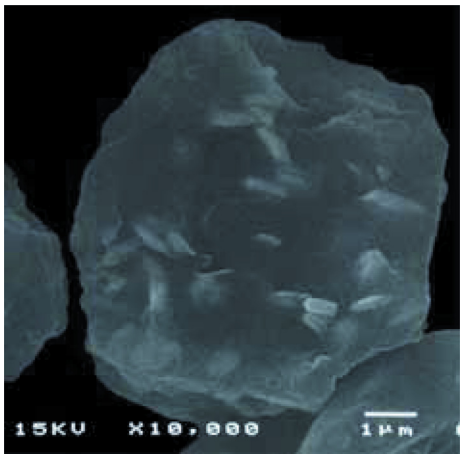


Figure 2. SEM Micrograph of Seed Toner

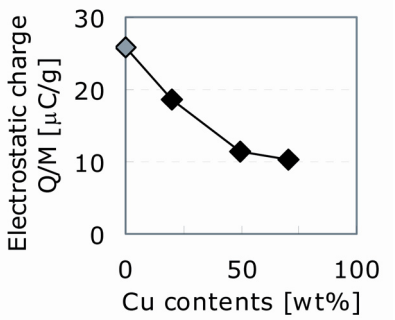


Figure 3. Plot of toner charge to Cu contents

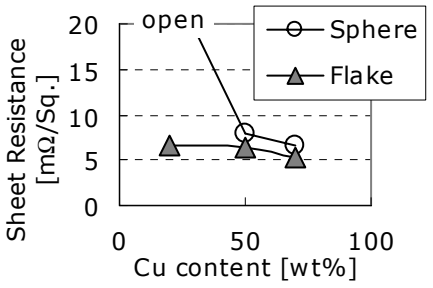


Figure 4. Sheet Resistance to Cu contents

3-2. Charge Control of Seed Toner

With normal additives formulation for conventional toner, the tribo-charge level of seed toner was very low. Thus the formulation and mixing condition of external additives, as well as the carrier formulation, was optimized. Figure 5 shows measured distribution of toner charge. In Figure 5 (a), graph of before optimization, entire charge was lower and rate of opposite charge of toner was high. After optimization of adding different external additives and change condition of carrier, as shown in Figure5 (b), entire charge of toner shifted to negative charged side and rate of opposite charge has become less than 5 count%.

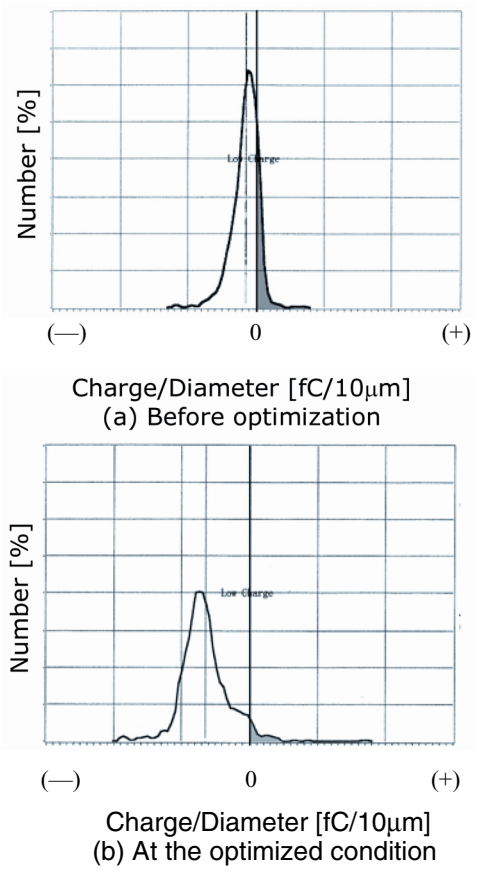


Figure 5. Electrostatic Charge of Seed Toner

3-3. Resolution of Lines

The toner at the optimized condition was printed on plane paper. Figure 6 shows the printed lines whose width and pitch are 120μm and 300μm, respectively. The image quality is very close to conventional black toner with little fog. The reducing of blur near lines is expected by further controlling of the toner size distribution in mass production. Therefore the line and space of circuit pattern printed by seed toner was proved to have resolution availability determined by resolution of electrophotography printer.

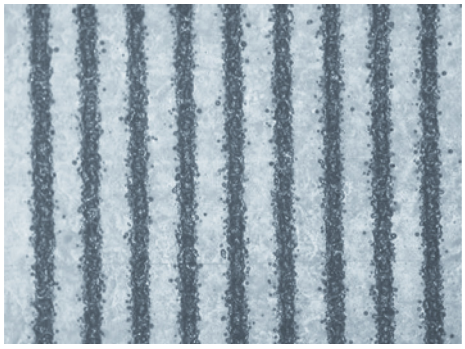


Figure 6. Printed Lines on Plane Paper (0.3 mm Pitch)

4. Insulating Layer and Multi-layer Structure

4-1. Flatness of Insulating Layer

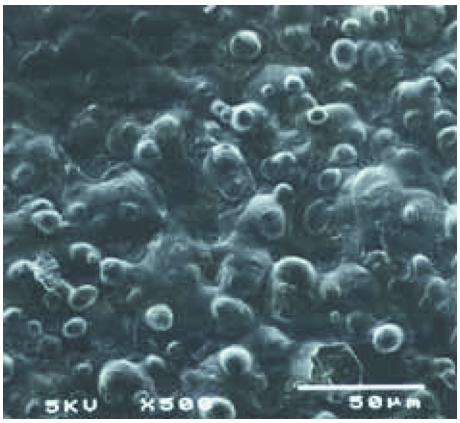
To form insulating layers of PCB, the enough thickness and flatness are required in order to obtain sufficient insulation and to prevent the corrosion caused by exposing metal to the moisture in open air. Thus it is necessary to ensure flatness and coating efficiencies without pinhole of the printed insulating layer.

Insulator toner, which is made of uncured epoxy resin in thermo-plasticity stage, is used for printing insulating layer. By heating, the toner begins the chemical reaction that transforms through in liquid state to in crosslinked and cured solid state. Relation between heating temperature in fusing process and the flatness of insulating layer has been evaluated.

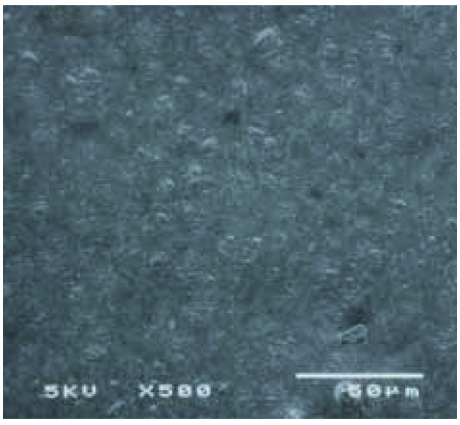
Figure 7 shows SEM micrographs of printed insulating layer, fusing at 100°C in (a) and at 160°C in (b). When fusing temperature was low, the surface was uneven because toner was not enough melted. However, the surface by heating at 160°C was almost flat and any pinhole was not observed. Figure 8 shows the measurement data of roughness, Ra ≅ 2.3 μm by fusing at low temperature (100°C) and 0.6μm at high temperature (160°C). Since Ra of base sheet is about 0.2μm, the toner binder of fusing temperature at 160°C wet and spread over the sheet well. In this measurement, Ra was calculated every length of 100μm, because the base sheet has undulation with a cycle of about 1mm.

The good flatness of printed layer is due to that this epoxy resin has low viscosity less than 1 Pa-s at 150°C. That is, by selecting an epoxy resin that has low viscosity at the

fusing temperature, a flat insulating layer can be formed without any pinhole.



(a) Fused at Low Temperature (100°C)



(b) Fused at High Temperature (160°C)

Figure 7. SEM Micrograph of Printed Insulating Layer

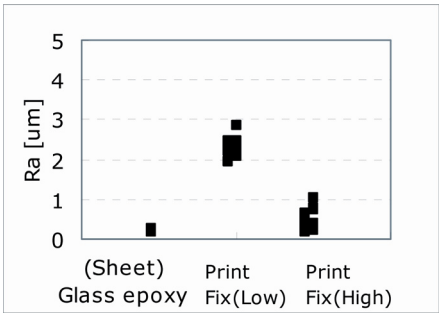


Figure 8. Measurement Plot of Roughness

4-2. Multi-layer Structure

Multi-layer structure using the new process is also investigated. Figure 9 shows samples of two layers of copper; (1) The 1st Cu layer was formed on glass epoxy base sheet. (2) Insulating layer was coated over the 1st Cu layer and the base sheet. The dark area in photograph is the 1st Cu layer under the insulating layer. The white area in the illustrated picture is "via-hole" pattern, an opened area in the insulating layer. Therefore, a part of the 1st Cu layer is seen through the via-hole as bright area in the photograph. (3) The 2nd Cu layer is patterned on them. The photograph is an example that the 2nd Cu layer is printed with doughnut's hole shape. Two Cu layers are connected by electroless Cu plating through via-hole as shown in illustrated picture.

Note that the two Cu layer structure formed by this method had good electrical connection in electrical resistance measurement.

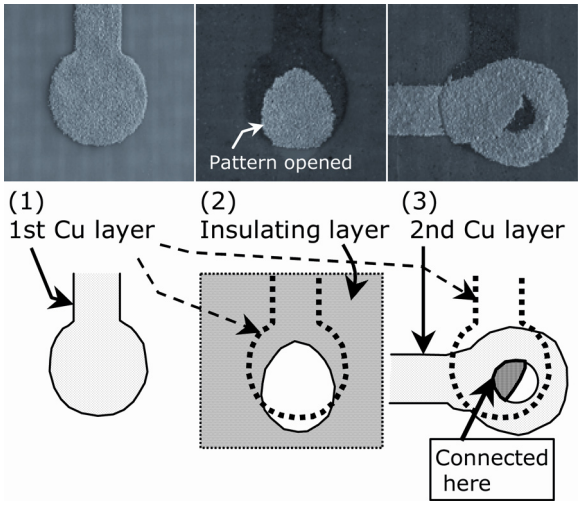


Figure 9. Multi-layer structure

5. Wiring Reliability

5-1. Reliability test

The basic reliability of wiring and insulating layers was evaluated. Test samples have Cu lines, whose width and thickness of Cu plating are 0.15mm and 5µm, respectively. The thickness of insulating layer coated on is about 20µm. The base sheet is glass epoxy of 50µm thickness.

The sheet resistance of lines is 3 – 4 mΩ/sq., corresponding to the specific resistivity about 2µΩ-cm, which is good enough even if compared with pure Cu. This means that the plating ability of the pattern with seed toner is quite good.

The wiring reliability tests as shown in Table 1 were carried out. The pass or fail was judged by electrical resistance (pass criteria is less than 10% resistance change) and visual inspection with microscope to find crack, color change, dendrite and so on. All samples passed as results of the examinations. In the high temperature bias test (electro-chemical migration test), sufficient insulation was provided and no metal dendrite was observed, with the samples whose line pitch and space between lines are 0.3 mm and 0.15 mm, respectively.

The tests clarified the good adhesion strength between the base sheet and Cu lines. Moreover, the insulating layer has no failure such as pinhole, crack and delamination of

interfaces of insulating layer/base sheet and insulating layer/Cu lines.

Table 1. Wiring Reliability Test Results

Reflow test	260°C peak, 8 times	10/10 OK
Moisture absorption reflow test (JEDEC Level 1)	260°C peak, 8 times (85°C / 85%, 168h)	10/10 OK
High temperature storage test	150°C, 1000 hours	10/10 OK
Temperature cycle test	-55 / 125°C, 1000 cycles	10/10 OK
High temperature bias test	85°C / 85%, 20V, 1000 hours	10/10 OK

5-2. Soldering Ability

Test chip assembly on PCB samples made by the new process was carried out in order to evaluate the soldering ability. The samples have area array bonding pads in 350μm pad pitch and patterns of daisy chains to examine electrical interconnection with test chip. The 15mm sq. size test chip has 1030 solder bumps. The chip is connected with the PCB through conventional Pb free solder reflow process (the peak temperature 260°C) with flux. Figure 10 shows the cross section of the connected bumps between the test chip and the PCB.

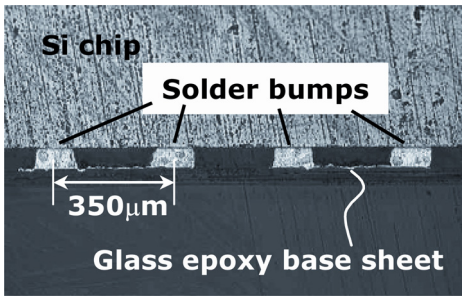


Figure 10. Flip Chip Assembly

Test chip assembly was ensured by electrical resistance check of daisy chains and by observation of fracture mode by solder distractive test. As a result, all bumps on 10 samples had good connection. Thus PCB by the new process has good soldering ability and enough adhesion in high temperature of solder reflow process.

6. Conclusion

New manufacturing process for printed circuit board (PCB) using electrophotography technology has been investigated.

1. By controlling the electrostatic charge of seed toner, 0.3mm pitch lines could be printed with the 600dpi printer.
2. Applying electroless Cu plating process, the specific resistance of printed wiring pattern was about 2 μΩ-cm.
3. The insulator toner, consist of uncured epoxy resin, formed insulating layer with flatness of Ra ≅ 0.6μm by fusing at 160°C.
4. Connection between 2 Cu layers was realized, which provides the process for multi-layer structure.
5. The new PCB has good reliability and soldering ability for electrical components.

References

1. P. Calvert, "Inkjet Printing for Materials and Devices", Chem. Mater. 2001, vol.13, pp.3299-3305
2. Paul H. Kydd, "Electrostatic Printing of ParmodTM Lectrical Conductors", IS&Ts NIP 14 (1998)

Biography

Hideo Aoki received the B.E. and M.E. degrees in mechanical engineering science from the Tokyo Institute of Technology, Tokyo, Japan, in 1984 and 1986, respectively. He joined Toshiba Corporation, Kanagawa, Japan, in 1986, where he was engaged in development of semiconductor packaging. He is a Senior Specialist in the Advanced Packaging Development Group, Semiconductor Company, Toshiba Corporation.