Flexible Image Codec For Image Printing

Chih Chien Lin, Chien Long Kao, Chieh Yi Huang, Jun Cheng Su,
Yung Kuo Ho and Chia Hsien Cheng
Opto-Electronics & Systems Laboratories
Industrial Technology Research Institute
HsinChu, Taiwan

Abstract

In a digital printing system, it is necessary to equip with a high-performance image codec module for the requirement of high image resolution and processing speed. A DWT (Discrete Wavelet Transform)-based image encoding and decoding technique that is commonly adopted for high-performance image application is proposed. A parallel processing mode, that uses an arbiter to make a continuous data propagation between DWT and multiple Entropy Coders, is the kernel idea of the technique. In this scheme, the role of the arbiter is to decide the propagation path of the Code Block data between DWT and one of the Entropy Coders. In addition, an efficiently managed strategy of the Code Block is another crucial design for improving the encoding and decoding speed. As a result, a high-performance hardware codec and speed-tuning module are implemented. The flexibility and high performance can be achieved with this implementation by manipulating optimal balance between cost and performance in various applications of image codec.

Introduction

Digital Images are usually compressed after transforming related pixel data into frequency domain by DFT (Discrete Fourier Transform), DCT (Discrete Cosine Transform) or DWT (Discrete Wavelet Transform) and so on. Among those transforming methods, DWT is the most efficient way to match up the following Arithmetic coding procedure. Its operation characteristics are spatial in distribution different from DFT and DCT. In addiction to above, DWT are formulated with a discrete convolution filter without actually requiring whole image pixel data, but instead only block-base data are needed. Its one of the advantages is to consequently avoid the block-effect that DCT used to subject to and caused image distortion. For instance, a JPEG file format is a typical example of using a DCT algorithm inside. In this paper, JPEG2000 is chosen as an illustration of advanced still image compression technology based on DWT.

The kernel part of image compression consists of DWT, Quantizer and Entropy coder, which contiguously processes those image block data called Tile. During these coding procedures, the data represented as Code Block are extracted from previous DWT transforming coefficients which are ordered in such a way that the contribution from the LL,HL,LH and HH sub-bands appear in that order. Then they send them to the Arithmetic coder for further process which uses each mutual independent Code Block as a minimum operation unit. This unique characteristic of each Code Block makes it possible to use multiple Entropy coders at the same time to speed up the coding performance.

In this paper we propose a flexible architecture using an arbiter to decide which Code Blocks should be sent to any available Entropy Coder without limitation in numbers. Not only does this specific way improve the coding speed, but also gives the powerful flexibility based on enough channel numbers. Besides Code Block buffers are embedded in each one of Entropy Coders as storage for Code Block pixel data. The operations are active when any one of Entropy Coders sends a request signal to an Arbiter and let the Buffer controller inside each of Entropy Coder detect the current status of the Code Block buffers. Its functions of the Buffer controller are properly generating a data request signal to the arbiter which runs on the highest priority and acknowledges the corresponding Entropy Coders.

After sending enough Code Block data into the Code Block buffers, the following coding procedure will be repetitively started within multiple Entropy coders. Based on this flexible architecture of image codec, the image coding performance could be estimated in advance by tuning different numbers of Entropy coder as a reference parameter, to de decided before actual implementation; on the other hand, the amount of logical gate counts in hardware could be a concern as well. However, a systematic management of formatted output from each Entropy coders must exist for further processing of big quantities of code stream data. More details and flowcharts between formatted output data and buffer management will be explained in the following section. The control principle including an Arbiter, Buffer Manager as well as Coding Scheduler in those Entropy coders will also be discussed.

Coding Principle

After Wavelet transform and quantization processing, each sub-band is divided into different Layer and Band called

LL, LH, HL and HH. Within each sub-band, the Code Block contributions appear in raster order. The samples in these Code Blocks will be fed into EBCOT (Embedded Block Coding with Optimized Truncation) which consists of Tier1 and Tier2 for following-up coding procedure. Because of its complexity, EBCOT does play a very important role in deciding whole image codec performance. Therefore how to accurately analyze its compression algorithm and architecture must be also considered.

The principle of EBCOT algorithm is briefly described as below: Each Code Block data is decomposed into several bit-planes which start from MSB to LSB. And then each sample of the bit-plane is coded in a particular scan pattern starting from the top left, the first four bits form the first column, the next four bits form the second column and so on. The scan pattern continues to proceed until the whole samples of the bit-plane are completely scanned. During the coding procedure of EBCOT, each sample of each bit-plane in a Code Block would be coded in only one of the three coding passes. The three coding passes are: Significance propagation, magnitude refinement and cleanup, which successively check the current relative variables such as State variable or Sign Bit of the bit-plane on the Code Block followed by generating contexts and decision by looking up the corresponding table defined in JPEG2000 Specification document for further Arithmetic Coder processing.

Arbiter Architecture

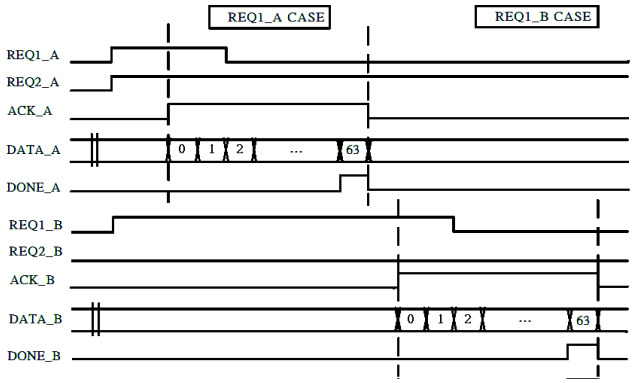

Figure 1. Arbiter data request interface

In this system architecture, an Arbiter plays the part of communicator between DWT and multiple Entropy Coders, having responsibilities for balancing data handshaking; Moreover, the amount of Entropy coders could be extended as much as possible and improve the processing efficiency of the formatted output coefficients from DWT.

The interface of arbiter is well defined according to its dataflow, which receives preliminary results from DWT first, and then dumps into a Code Block buffer embedded in each Entropy Coder. In a Code Block buffer, there is a specific structure of Ping-Pong mechanism existed, which means two storage buffers form a basic unit as a channel to request data handshaking between DWT and an Entropy Coder. For example, we have two sets of channels called Channel A and Channel B. Each one of the channels consists of two request lines named REQ1_X and REQ2_X and some other handshaking function signals such as ACK_X, DONE_X and DATA_X. (X : A,B,C….). REQ1_X represents the higher priority when two Code Block Buffers are all empty and REQ2_X represents the lower priority only when any one of them is empty. The levels of two request lines represent each buffer status whether they are ready to request data or not. While receiving request signal from any Entropy Coder, the arbiter will transmit available Code Block data corresponded with proper DATA_X signal and finally send a DONE_X signal at the end. The figure (1) shown as below indicates that the arbiter will choose the highest priority channel to be serviced while different request lines happen at the same time (REQ1_A > REQ1_B > REQ2_A > REQ2_B). In this case, REQ1_A is produced when the Ping-Pong Buffers inside the Entropy Coder are all empty and its own request line is accepted by an Arbiter because of its highest priority property.

Efficient Buffer Handling

There are two stages of memory management existed in each Buffer controller of an Entropy Coder. The purpose of the first stage is to directly take the formatted output data i.e. (a Code Block data) from Arbiter. And second stage is to decompose any one of the Code Block data into different bit-planes which consists of Sign and Coefficient buffer. However, it also implies that other State variables, Visit and Magnitude refinement variables buffers are included for encoding/decoding procedure. The figure (2) shown as below indicates that the Code Block data in each Code Block buffer would be arranged in a special pattern in order to match the whole dataflow efficiency between the arbiter and Entropy Coding Kernel Unit (Tier1).

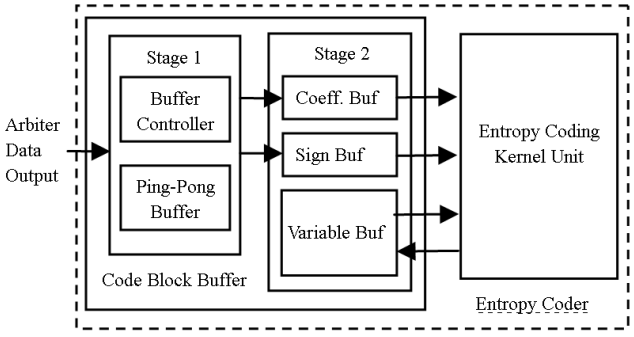

Figure 2. The code block buffer structure

Strategy of Bit-stream Management

Each Code Block data are continuously compressed into a code-stream by an Entropy Coder which processes any one of them as a basic unit. In order to achieve high processing efficiency, FIFO (Fist in First Out) is mostly used and store each processed compressed data and corresponding information of the specific Code Block data, which includes

the tile number of the current Code Block , sub-band type of the current Code Block, the start bit-plane number, total count of compressed data bytes ,MSE(Mean-Square-Error) and an unique given ID maker which differentiates each Content. All of these would be individually assigned to a specific memory location shown in Figure (3).

Due to the input data source of each Entropy Coder are dispatched by an Arbiter which uses an optimum arbitration algorithm to deal with the whole data flow efficiency. Therefore, the output sequence of each processed Code Block data would not be predictable. It is a simple way to use such a tag to identify the contents of all the Code Blocks stored in memory.

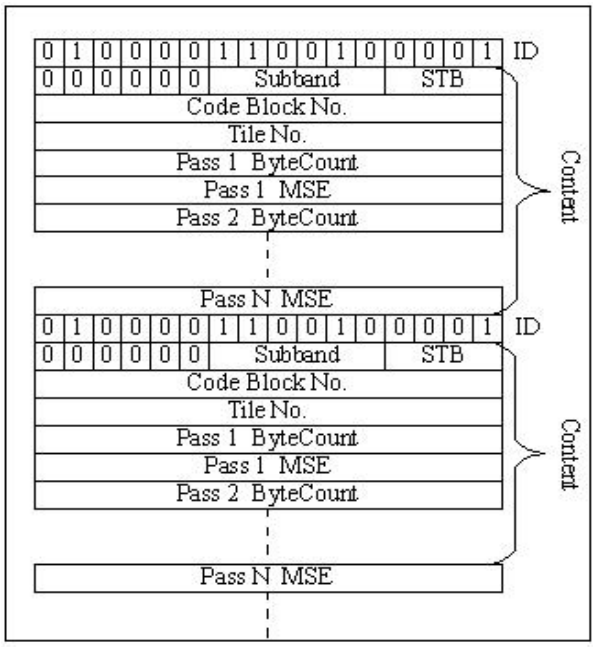

Figure 3. Code block marker storing procedure

Processing Schedule

As to the whole system architecture shown in Figure (4), the nature of pipe-line processing dataflow could have been achieved since any hardware module would be assigned to activate in any time if the Arbiter detects any possibility of sub-module having been waiting for next operation. On the other hand; this specific system architecture has come up with such advantages of flexibility which makes the designers easier to integrate and consider any limitation existed in any special application. Eventually time to market would be reduced as much as possible and demanding of unique product characteristics would be achieved in a short time. In Table (1), Image coding schedule is listed as a simple demonstration.

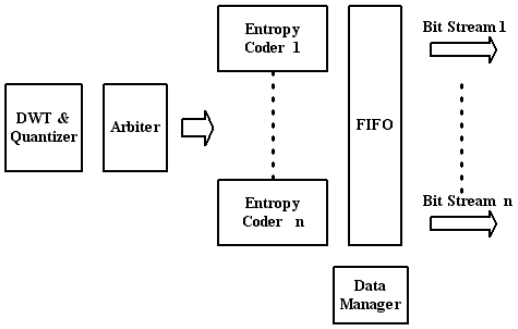

Figure 4. Flexible with multiple Entropy Coders structure

Table 1. Image coding schedule

Sch.	1st	2nd	3rd	4th	5th	6th
Image Input	Tile1	Tile2	Tile3	Tile4		
DWT		Tile1	Tile2	Tile3	Tile4	
Entropy Coder			Tile1	Tile2	Tile3	Tile4

Experiment Result

The compression throughput could be obviously promoted by using the specific architecture, but also the whole system performance could be much higher depending on how many numbers of the Entropy Coders (EC) are included. A formula shown as below could quantify the rate of final output code-stream:

$$G = D + n \times E$$

(G: Utilized Gate Counts, D:DWT Gate Counts, E: Entropy Coders Gate Counts, n: number of Entropy Coders)

In an actual experimental statistics shown in Figure (5), it demonstrates the whole system performance could achieve 11M Samples/sec by only using four Entropy Coders, which definitely complies with the basic 720 by 480 motion picture requirement based on running 40 Mhz system frequency.

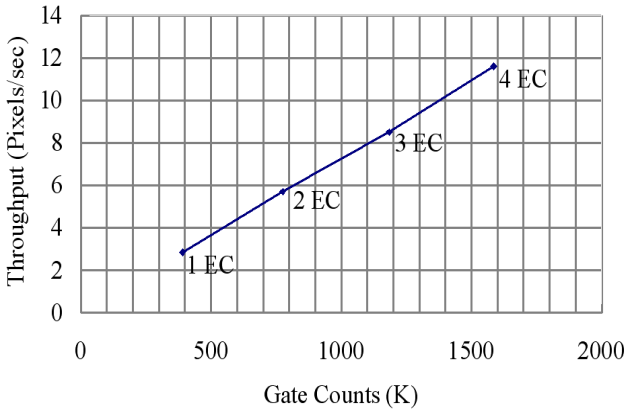

Figure 5. Results of flexible coding structure

Conclusion

In this paper, a high-performance architecture of hardware image codec with a throughput-tuning methodology for JPEG-2000 is presented. In the proposed architecture, an Arbiter is designed between DWT and Multiple-Entropy Coders to enable continuous data propagation. The number of Entropy Coders is determined by manipulating optimal balance between cost and performance. The implementation of the architecture demonstrates that the throughput is proportioned to the number of Entropy Coders. In this experimental implementation, system throughput could achieve 11M sample/sec by using four Entropy Coders. With efficient buffer handling, a specially designed strategy of bit-stream management and processing scheduling, a highly flexible image codec for image printing is proposed and demonstrated.

References

1. H.Witten, R. M. Neal, and J. G. Cleary, Arithmetic Coding for Data Compression, Communications of the ACM, Vol.30, No 6, pp. 520-540, 1987.
2. W. Pennebaker and J. Mitchell, JPEG, Still Image Data Compression Standard, Van Nostrand Reinhold, NY 1992.
3. JPEG 2000 International Standard Part I, ISO/IEC 15444-1.
4. M. Gormish, D. Lee, M. Marcellin ,JPEG 2000 Overview, Architecture, and Applications, Proc. Of IEEE International Conference on Image Processing(ICIP), Vancouver, Canada, Sep. 2000.
5. T.C.Yang, K. S, Y. Bao, C. J. Kuo, Robust Coding of images using EBCOT and RVLC, multimedia Signal Processing, 1999 IEEE 3rd Workshop, 1999, 395-400.
6. I. Moccagatta, M. Z. Coban, H. H. Chen, Wavelet-Based Image Coding: Comparison of MPEG-4 and JPEG-2000, Proc. Of thirty-third Asilomar Conference on Signals, Systems, and Computers, pp. 1178-1182, 1999.
7. D.Santa Cruz, T. Ebrahimi, An Analytical Study of JPEG2000 Fundamentals, Proc. of IEEE International Conference on Image Processing(IPIC), Vancouver, Canada, Sep. 2000.
8. D.Taubman, EBCOT: Embedded Block Coding wieh Optimized Truncation, ISO/IEC JTC1/SC29/WG1 N1020R.
9. D. Taubman, High Performance Scalable Image Compression with EBCOT, IEEE Trans. On Image Processing, July, 2000.

Biographies

Chih Chien Lin received the B.S. degree in mechanical engineering from National Chiao Tung University, Hsinchu, Taiwan in 1997, and M.S. degree in mechanical engineering from Nation Chiao Tung University, HsinChu, Taiwan in 1999. He is currently working in Opto-Electronics & Systems Laboratories of Industrial Technology Research Institute, Hsinchu, Taiwan, as an associate Engineer. His current research areas include image coding and printing system design.

Chien Long Kao received the B.S. degree in mechanical engineering from National Chung Hsing University, Taichung, Taiwan in 1998. and M.S. degree in electrical & control engineering from Nation Chiao Tung University, HsinChu, Taiwan in 2000. He is currently working in Opto-Electronics & Systems Laboratories of Industrial Technology Research Institute, Hsinchu, Taiwan, as an associate Engineer. His current research areas include image coding, integrated circuit and servo control design.

Chieh Yi Huang received the B.S. degree in electrical engineering from National Taiwan University of Science and Technology, Taipei, Taiwan in 1996. He is currently working in Opto-Electronics & Systems Laboratories of Industrial Technology Research Institute, Hsinchu, Taiwan, as an Engineer, and studying M.S. degree in electrical and control engineering from Nation Chiao Tung University, HsinChu, Taiwan . His current research areas include image coding and printing system design.

Jun Cheng Su received the B.S. degree in electrical engineering from National Taiwan University of Science and Technology,Taipei, Taiwan in 1997, and then M.S. degree in electrical engineering from National Tsing Hua University, HsinChu, Taiwan in 1999. He is currently working in Opto-Electronics & Systems Laboratories of Industrial Technology Research Institute, Hsinchu, Taiwan, as an associate Engineer. His current research areas includes Image processing and printing technology.

Yung Kuo Ho received the B.S. degree in electronic engineering from Chung Yuan Chistian University, Chung-Li, Taiwan in 1999, and M.S. degree in electronic engineering from Chang Gung University, Kwei-Shan Tao-Yuan, Taiwan in 2001. He is currently working in Opto-Electronics & Systems Laboratories of Industrial Technology Research Institute, Hsinchu, Taiwan, as an associate Engineer. His current research areas include digital integrated circuit design and printing system design.

Chia Hsien Cheng receivde the B.S. degree in electronic engineering from Kao Yuan Institute of Technology, Kaohsiung, Taiwan in 2000, and M.S. degree in electronic engineering from Southern Taiwan University of Technology, Tainan, Taiwan in 2002. He is currently working in Opto-Electronics & Systems Laboratories of Industrial Technology Research Institute, Hsinchu, Taiwan, as an associate Engineer. His current research areas include data compression and printing system design.