Jet-printed Lithography for Semiconductor Device Fabrication

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Abstract

Phase-change wax-based printed masks, in place of conventional photoresist masks, were used to fabricate a-Si:H thin-film transistors (TFTs). Printed wax-mask features with a minimum feature size of ~20 μm were achieved using an acoustic-ink-printing process. Both discrete and matrix addressing structured bottom-gate TFTs with source-drain contacts overlapping the channel were created using a four-mask process. The TFTs had I-V characteristics comparable to photolithographically patterned devices, with mobility of 0.6-1 $cm^2/V \cdot s$, threshold voltage of 2-3 V, and on/off ratios exceeding 10^7 for devices with channel lengths below 50μm. The wax-mask process was also used to fabricate self-aligned TFT devices, eliminating the source-drain contact overlap constraint.

Introduction

Due in large part to the complexity of photolithographically-based processing techniques, the cost of large-area active-matrix liquid crystal displays and image sensors is prohibitively expensive. By simplifying the fabrication method, process steps such as large-area coverage of spin-on photo resist,[1] pattern definition, and resist pattern development can be eliminated in order to lessen the cost and complexity of fabrication. A method such as direct writing is an ideal alternative to conventional photolithography;[2-4] a technique such as jet printing would allow low-cost TFT fabrication by combining small printed features and large-area coverage.

The use of laser printed toner etch masks has been demonstrated in fabricating a-Si:H TFT transistors,[5-7] although the laser printed features do not allow for reasonable resolution in a display or imager array. The use of ink-jetted liquids to directly write etch masks is a practical alternative to printed toner. Jetted liquids, though, still possess inherent difficulties. For example, when liquid drops are put onto a surface the droplet configuration is largely determined by its wetting properties. Typically small wetting angles are required to obtain good adhesion to a surface but this condition allows the liquid to spread and form relatively large features. On the other hand, if the liquid does not wet the surface due to a high surface energy a large contact angle will form resulting in small drop features but these printed droplets may adhere poorly. Neither situation is desirable in semiconductor processing – the former increases the feature size and the latter gives unreliable patterning.

The use of a phase-change media circumvents many of these problems. A material slightly above its liquid/solid phase transition temperature may be ejected from a jet-printing nozzle; the droplet solidifies quickly upon contact onto a cooler surface. The feature size will then depend more on the cooling rate and less on the materials wetting properties since a frozen droplet cannot spread. In this situation, the feature size may be controlled by the substrate temperature permitting materials with high wetting properties to be used to create a small feature size.

The use of jetted etch mask also addresses problems of direct writing of metals.[8] Jetting most metals for semiconductor processing is unrealistic due to their high melting temperatures. For example, refractory metals such as Cr are commonly used as gate metals in TFT fabrication. The ejection of liquid Cr at 1900°C from a printhead would be impractical in conventional jet-printing processes. A more functional approach is to deposit the thin-film material and subsequently use an etch-mask process to define the device structures as in a conventional TFT process flow. This article describes a method for fabricating a-Si:H TFTs using jet-printed phase-change materials to define the mask features in place of conventional photolithography. The printed mask process described is capable of 20 μm feature sizes, which can enable the fabrication of arrays with 200 μm^2 pixels.

Experimental

Jet-printing of the phase-change wax was accomplished with a nozzleless printhead in which ejected droplets are formed by an acoustic wave.[9] The acoustic ink printing (AIP) process achieves small print features by ejecting small drop volumes in the order of 2-3 picoliters while an additional degree of control in printed feature size is obtained through the use of phase-change waxes. In the case of the Kemamide-based wax used as a mask material, the variation of printed line resolution was strongly dependant on the substrate temperature. By controlling the rate of cooling for the ejected droplet, printed minimum feature sizes were varied from as small as 20 μm to as large as 40

μm by simply changing the substrate temperature over a 20°C range.

Insulated-gate thin-film transistors were fabricated on four-inch glass substrates using a three-layer wax-mask process. Mask layers were used to define the gate metal, active device island, and source-drain metal contacts. A bottom gate Cr electrode configuration was employed. First, a 100 nm thick Cr film was deposited onto glass that was then patterned using the Kemamide-based wax ejected from an AIP printhead. Next, a 300 nm thick Si_3N_4 layer followed by a 50 nm a-Si layer and a 200 nm Si_3N_4 layer were deposited over the Cr gate creating the Si_3N_4/a:Si/ Si_3N_4 (NSN) device stack. Fixing the substrate position and offsetting the mask imagefile, which enabled layer-to-layer registration to within 10 μm, accomplished the mask alignment. Next, the active device island features were define by wax printing followed by a wet-chemical etch to define the island features.

Following the island definition, the top nitride layer was defined using a self-aligned process in which spin-on photoresist was applied onto the glass/Cr gate/NSN-island structures. In this step, the mask aligner is bypassed since a blanket UV exposure through the back of the transparent glass substrate defines the top nitride feature self-aligned to the Cr gate. The top nitride was then etched away and a 100 nm thick n^+ Si layer was deposited followed by the Al source-drain contact metal deposition to complete the device stack. The source-drain metal was defined by printed mask patterning and the device was completed by removing the exposed n^+ Si layer by plasma etching using the source-drain contacts as etch masks. The process flow is shown in Fig. 1.

Results and Discussion

By using the process flow described in Fig. 1, working TFT devices were fabricated and tested in comparison to transistors made by conventional semiconductor device processing. These transistors had gate widths and lengths ranging from 40-370 μm. The output characteristics of a TFT device with dimensions W/L = 370 μm/140 μm (40 μm overlap gap) fabricated by printed wax-masks are shown in Fig. 2a. The threshold voltage for these devices were measured to be ~2-3 V with the gate voltage varied from 0 V to the maximum drain voltage, V_D = 15 V. Figure 2b shows the transfer characteristics for devices with a W/L = 130 μm / 40 μm (20 μm overlap gap) having a measured mobility between 0.6 to 0.9 $cm^2/V \cdot s$ and an on/off ratio of 10^7. Except for the slightly high gate leakage current, the resulting device performance was comparable to a-Si:H TFT devices fabricated using conventional photolithographic techniques. It is probable that the higher gate leakage is due to poor isolation of the device island structure during the device fabrication. A possible remedy for reducing the leakage is by isolating the island structure better with the top nitride using a via contact to the bottom gate electrode.

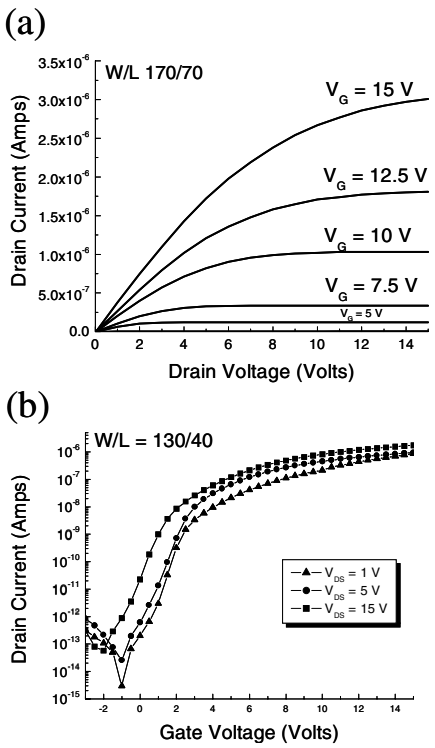

Figure 1. I-V curves for a TFT fabricated by using printed etch masks.

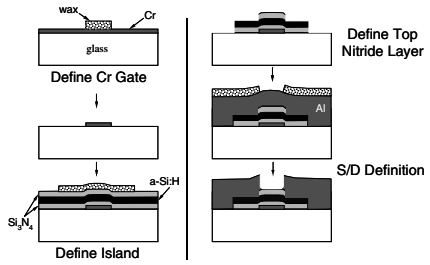

Figure 2. Process flow for printed etch mask TFT fabrication.

As a demonstration for fabricating TFT arrays, interconnected TFTs were made using the wax-mask patterning technique. Arrays of 64×64 pixels were fabricated using the same process described in making the discrete devices with common gate and drain electrode configurations having a 40 μm channel width and 80 μm channel length. Figure 3 shows an optical micrograph of an array of transistors processed using the printed wax masks with a pixel size of ~300 μm.

The transfer characteristics for a typical transistor, Figure 4, had mobility of ~0.8 $cm^2/V \cdot s$, threshold voltage of ~1 V, and on/off ratio of 10^8, similar to the performance of the discrete TFT devices. The functioning array demonstrates the feasibility of printed mask patterning as a viable alternative to conventional photolithography processes. The feature size obtained by inkjet printing and the compatibility of the wax material to conventional

semiconductor processing offer substantial advantages in process simplification and cost reduction in the fabrication of large-area TFT arrays.

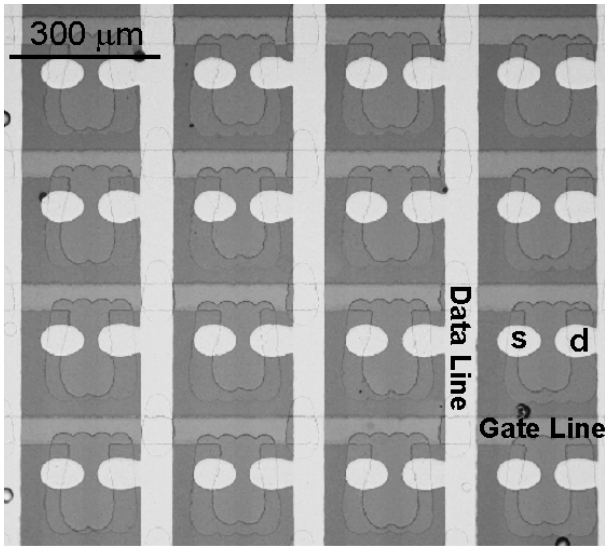

Figure 3. Optical micrograph of a transistor array with 300 μm pixels.

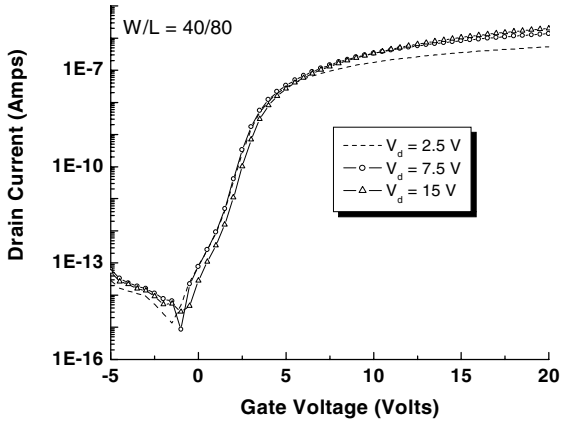

Figure 4. Transfer characteristics for an active-matrix addressing array transistor with mobility of ~0.8 $cm^2/V \cdot s$

Conclusion

Bottom-gate electrode TFTs were fabricated using a four-mask layer process incorporating ink-jet printed wax masks. Device characteristics for the fabricated TFTs were comparable to conventionally processed TFTs having a threshold voltage of 2-3 V, mobility of 0.6-1 $cm^2/V \cdot s$ and on/off ratios of 10^7 for devices with gate lengths less than 50 μm. A self-aligned process was also used to fabricate discrete TFT devices without a source/drain overlap constraint. Finally, 64×64 matrix addressing TFT array structures were fabricated using the printed wax-mask in place of conventional photolithography.

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Biography

William S. Wong received his B.S. degree in Mechanical Engineering from the University of California at Los Angeles in 1990 and a Ph.D. in Materials Science from the University of California at Berkeley in 1999. Since 2000 he has worked in the Palo Alto Research Center in Palo Alto, CA. His work has primarily focused on the materials integration and processing, including amorphous silicon TFT processing and InGaN laser diode device integration. He is a member of the Materials Research Society and the International Microelectronics and Packaging Society.