Gray Resolution Enhancement Anti-aliasing Technology (GRET) for High Speed Printing

Yee S. Ng
NexPress Solutions
Rochester, New York, USA

Abstract

In order to improve the output image quality of binary text and graphics (even for binary information that are buried within a document which also has gray level information), a gray level resolution enhancement anti-aliasing method (GRET) that uses feature extraction and a rule-based decision matrix for edge enhancement (anti-aliasing) with multi-level (LED) output printing capability in a electrophotographic system is described. A pipelined architecture (with a conflict resolution priority-sorting scheme in the decision matrix) was used to enable all the decision operations to be performed at the same time (for efficient high-speed operation) and was implemented in an ASIC. Further, a scalable multiple chip architecture with overlapping pixels at the end of the image segments was created to enable enhancement operation for wider width and higher speed printing.

Introduction

Edge enhancement methods [1-6] have been used to reduce stairstepping and aliasing of lower input resolution binary text and graphics in printers in order to improve output image quality. Either higher addressability system[4] or system with gray level capability [5, 7] can be used in the output printer to implement the edge enhancement methods. However in some imaging cases, there are also high contrast text and graphics embedded within binary and gray level halftones that can benefit from edge enhancement method as well. An anti-aliasing method with gray level LED printing output capability[5] (GRET) that can improve the output image quality of high contrast text and graphics (even for information buried within gray level information – such as gray level halftone) is discussed here. An architecture that is scalable to very high speed operation with overlapping GRET components is also discussed [8]

GRET Anti-aliasing Method

The input data to the printing system may consists of high contrast (or binary) text and graphics that may also be buried within gray level information (such as gray level halftones). In Figure 1, we show the block diagram that reflects the basic Grey Resolution Enhancement Anti-aliasing Technology (GRET). The data is first buffered by a 9-lines FIFO. The input data goes through a 3x3 window which has a gray value detect function to determine whether there are values within the window that are not high contrast or close to binary. In parallel with that window function, there are two other functions, (1) a Data conversation function that change the incoming data into binary data via a threshold function for further anti-aliasing image enhancement processing and (2) a bypass function that passes the original data with a time delay. The output of the gray detect function (with a time delay) determines whether the system takes the bypass input values or the enhanced modified values.

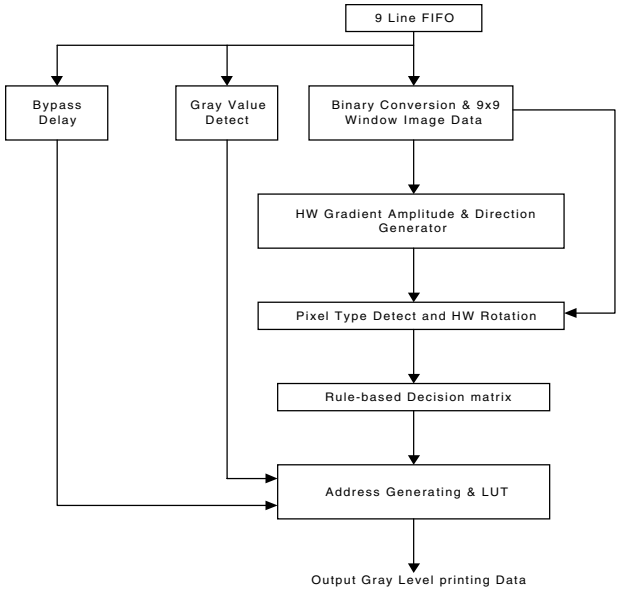


Figure 1. Block Diagram for GRET

For high speed operation, the binarized data was held temporarily by a 9x9 image data window which via a hardware LUT, generates pixel gradient amplitude and gradient direction data (eight directions {north, north-east, east, south-east, south, south-west, west, north-west} and a zero direction when there is no gradient direction change) in one clock cycle. The current pixel direction data (for the center pixel) was then used to trigger a hardware data

rotation for the pixel values, gradient direction and gradient amplitude; so all the selected eight direction's data (values, amplitudes and directions) are all folded into one set for further processing in order to save time and hardware space. These pixel values, gradient directions and amplitudes are used for a rule-based decision matrix [5] for an anti-aliasing function. The decision matrix have multiple rules (with different priority that execute at the same time in one clock cycle as shown in Figure 2) that determine what suggested location (or types) of the current pixel is. There are situations that the current pixel may fit multiple locations (or type), but the higher priority rule wins. The output of the decision matrix points to suggested enhanced data value via a LUT that output a gray value for printer exposure. Whether the printer will take the enhanced data value versus the original data value depends on the outcome of the gray value detect function mentioned earlier. (GRET) functions like this have been implemented in an ASIC for high-speed operation.

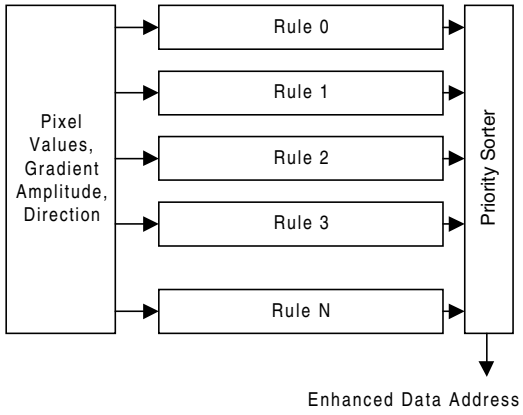


Figure 2. Decision Matrix with Priority Sorting

High Speed Scalable Architecture

For even higher speed or wider width operation, an architecture[8] has been created that can use multiple GRET components in an overlapping function as shown in Figure 3. As an example, we use a four data line segments approach here for higher speed operation. In this case, each input data line of N pixels/line is divided into four line segment of equal line length {(N/4) + 8} for easier parallel processing. Pixels 5 to (N-4) of the input data line are the enhanced pixels after GRET enhancement processing. This approach can be expanded to more segments for even wider width and higher speed operations. This architecture is scalable to two-dimensional operation and can be used for display output versus printer output.

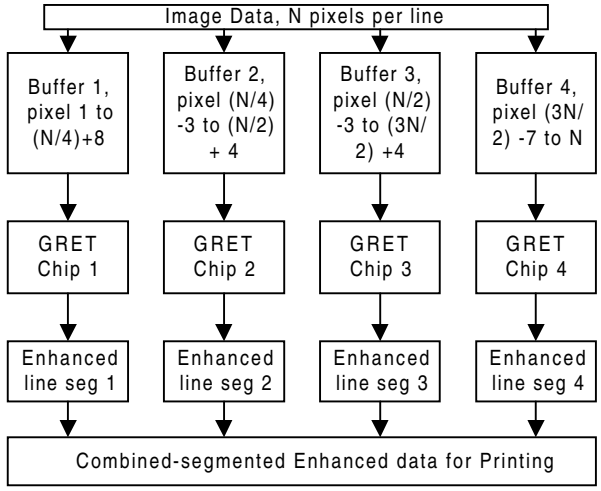


Figure 3. Multiple Chip Module approach for GRET in High Speed Printing

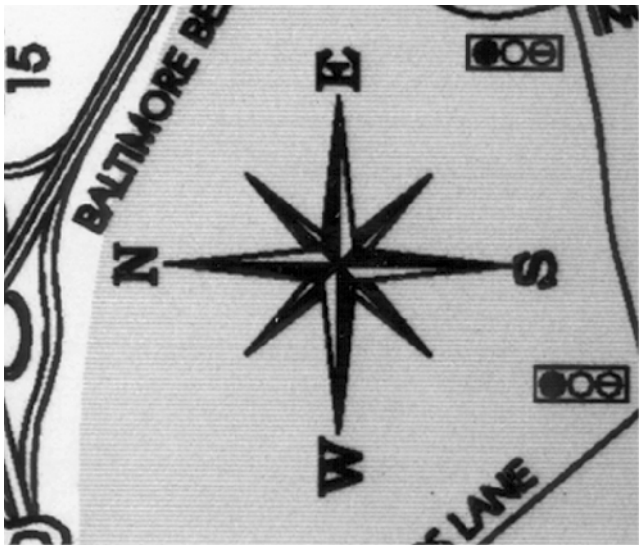
Results

As an example, we show in Picture 1 below: a screen display of an input binary text image on the left and the GRET enhanced gray level text image on the right. Aliasing has been reduced for the text. The values for the output LUT of the GRET was tuned for the output multiple-level exposures and the electrophotographic process in order to produce line widths visually similar to that of the original binary input (with reduction in aliasing).

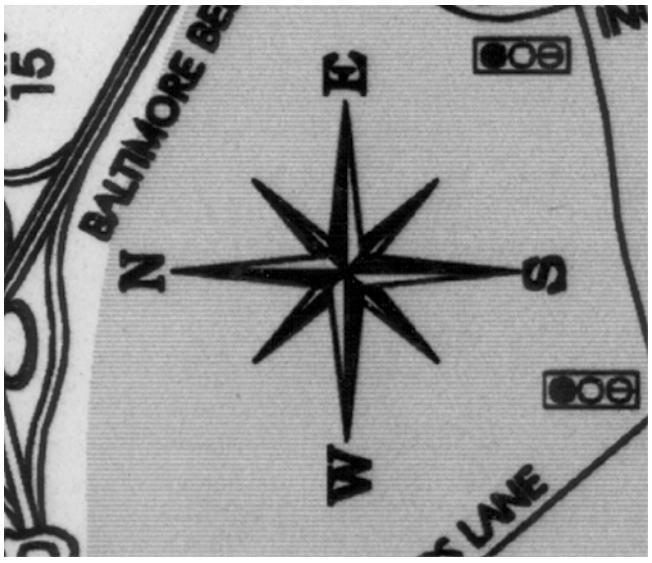
Picture 1. Screen Display of Anti-aliasing with GRET

In Picture 2 below, we show a magnified view of a printed image that uses binary graphics buried within gray level halftone picture. Aliasing of some of the graphic elements

on the image is observable. In Picture 3 below, we show a magnified view of the GRET enhanced printed image (from the same input file used for Picture 2). Aliasing on the high contrast binary graphics elements have been reduced without changing the structure and tone of the gray level halftone elements. This GRET system also works well with binary graphics elements (that need anti-aliasing) that are buried within binary halftones.

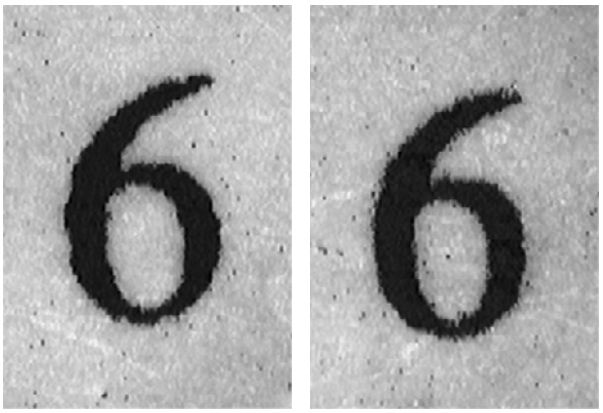


Picture 2. Magnified view of Binary text and graphics within multiple-level halftones



Picture 3. Magnified view of GRET enhanced text and graphics within multiple-level halftones

In Picture 4, we show on the left a magnified view of a binary character "6" printed at 600 dpi using dry electrophotography and on the right the same letter with GRET enhancement and printed using the same multiple-level LED printhead at high speed. As you can see, the aliasing on the character has been reduced and the text quality has improved. The line width and the general intend of the font has been preserved.



Picture 4. Magnified view of printed 600 dpi character. Binary text on the left and GRET enhanced text on the right

Conclusion

A gray level resolution enhancement anti-aliasing method (GRET) that uses feature extraction and a rule-based decision matrix for edge enhancement (anti-aliasing) with multi-level (LED) output printing capability in a electrophotographic system is shown to reduce aliasing of binary text and graphics elements (even those buried within multiple level halftones) in input images. A pipelined architecture (with a conflict resolution priority-sorting scheme in the decision matrix) was used to enable all the decision operations to be performed at the same time (for efficient high-speed operation) and was implemented in an ASIC. Further, a scalable multiple chip architecture with overlapping pixels at the end of the image segments was created to enable enhancement operation for even wider width and higher speed printing.

References

1. Charles C. Tung, Piec-wise Print Image Enhancement for Dot Matrix Printers, U.S. Patent 5,005,139 (1991).
2. James C. Y. Lung, Edge Enhancement Method and Apparatus for Dot Matrix Devices, U.S. Patent 5,029,108 (1991).
3. A. L. Frazier, J.S. Pierson, Resolution Transformation Raster-based Imaging System, U.S. Patent 5,134,495 (1992).
4. A.L. Frazer, J.S. Pierson, Interleaving Vertical Pixels in Raster-based Laser Printers, U.S. Patent 5,193,008 (1993).
5. Yee S. Ng, Hurjey Yeh and Michael Pickup, Resolution Enhancement System for Combined Binary and Gray Scale Halftone Images, U.S. Patent 5,450,531 (1995).
6. Yee S. Ng, Resolution Enhancement System for Binary Images, U.S. Patent 5,502,793 (1996).
7. Yee S. Ng, Hieu T. Pham, Hwai T. Tai and Eric K. Zeise, Gray Level Printing method with Embedded Non-Uniformity Correction using a Multibit LED Printhead, IS&T's 47 Annual Conference Proceeding, pg. 622-625 (1994).

8. Yee S. Ng, Glenn R. VanLare, Richard T. Fischer, Resolution Enhancement System for Digital Images, U.S. Patent 6,021,256 (2000).

Biography

Yee S. Ng received his B.S. degree in Engineering Physics from the University of Illinois, his M.S. degree in Electrical Engineering and a Ph.D. degree in Physics from the Pennsylvania State University. He joined Eastman Kodak Research Laboratory in 1980. He was a Kodak Distinguished Inventor and holds > 78 U.S. patents. His work has primarily focused on color proofing, electrophotographic processes, image rendering/ enhancement, image quality issues, electronic writer and image data path development. He was a Science Associate and a Project Chief Engineer in Kodak before joining NexPress Solutions LLC as a Chief Engineer in 1999. He is a member of IS&T, IEEE, APS, the New York Academy of Sciences and the American Association for the Advancement of Sciences. He was awarded the IS&T's Chester Carlson award in year 2000.