

Organic Semiconductor Thin-Film Field-Effect Transistors

C. D. Dimitrakopoulos, J. Kymissis, and S. Purushothaman
IBM Research, T. J. Watson Research Center, Yorktown Heights, New York

Abstract

Pentacene is the best performing organic for thin-film field-effect transistor (TFT) applications and its performance rivals that of a-Si:H.[1] We show how to fabricate pentacene TFT with source and drain electrodes lithographically patterned, before the deposition of the pentacene layer on them, and concurrently achieve performance equal to that of TFT fabricated with the reverse layering sequence. We also present a novel method for subtractive patterning of the pentacene layer that does not affect its transport properties. Earlier results on high performance organic TFT at low operating voltage are also presented.

TFTs comprising an organic semiconductor layer have been the focus of considerable research activity starting about 15 years ago.[2,3] Such devices based on conjugated polymers, oligomers or other molecules have been fabricated and studied in the past. The mobility of the organic semiconductor thin films is low compared to crystalline Si. However, the demonstrated performance of organic TFT rivals that of hydrogenated amorphous silicon (a-Si:H) TFT. Reviews of the progress in mobility of organic TFT have been published recently.[4,5] Two classes of organic semiconductors have exhibited the best TFT performance accompanied by good environmental stability: end-substituted thiophene oligomers and pentacene. α,ω-dihexyl hexathiophene (DH6T), first introduced in organic TFT by Garnier et al.,[6] is a conjugated oligomer that exhibits a pronounced capacity for self-assembly in close-packed configurations. The highest values of field effect mobility (μ) reported for DH6T films range from 0.07[6] to 0.13[4] $cm^2 V^{-1} s^{-1}$.

Pentacene-based thin film transistors have produced the highest field effect mobility values reported for organic TFT, which in some cases approach 1 $cm^2 V^{-1} s^{-1}$ with an on/off current ratio of 10^8.[7] These values of mobility and on/off ratio are similar to the ones reported for hydrogenated amorphous silicon (a-Si:H) TFT. However, the operating voltage required to achieve such high performance from pentacene devices is too high (a voltage swing from -100 to +100 V is required). This shortcoming can be demonstrated by comparing the subthreshold slopes of a-Si:H devices (about 0.5 V/decade) and those of pentacene-based TFT, which are about 5-12 V/decade or higher. We have studied the gate voltage dependence of mobility in pentacene devices, and used our understanding to demonstrate high performance pentacene TFTs exhibiting high mobility, good current modulation and excellent subthreshold slopes at low operating voltages.[1,8] For this purpose we employed relatively high dielectric constant metal oxide films as gate insulators. Furthermore, we developed a room temperature fabrication process that enabled us to grow such devices on transparent plastic substrates.[1] The typical device configuration used in our previous work is depicted in Figure 1A. Gold source and drain electrodes were vapor-deposited on pentacene through silicon membrane masks. Pentacene films were deposited using vacuum sublimation. Further details on the vacuum chamber configuration and deposition conditions can be found in reference 4. Relatively high dielectric constant gate insulator layers were deposited on substrates with Pt gate lines using rf magnetron sputtering in the case of barium zirconate titanate (BZT),[1] or were spin-coated by means of a Ba, Sr, Ti isopropanol/acetic acid solution in the case of barium strontium titanate (BST).[8] The latter films were additionally annealed at 400 °C in O_2.

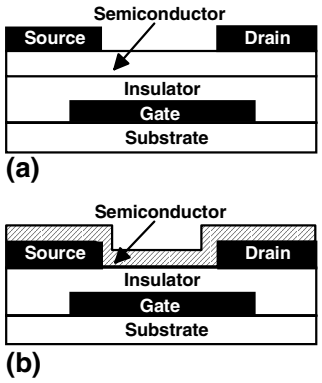

Figure 1

In order to achieve mobilities of about 0.5 $cm^2 V^{-1} sec^{-1}$ in pentacene TFTs employing a SiO_2 gate insulator with thickness in the range of 0.1 μm, a gate voltage close to 100 V is required. Figures 2a and 2b show the dependence of field effect mobility, μ, on the charge per unit area at the semiconductor side of the insulator, Q_s, and the gate field, E, respectively. The black circles correspond to a pentacene-based device with a 0.12 μm thick SiO_2 gate

insulator, thermally grown on the surface of a heavily doped n-type Si wafer that acts as the gate electrode. The dotted black circles correspond to a similar device, which, however, employs a 0.5 μm thick SiO_2 gate insulator. The mobilities for the SiO_2-based devices are calculated at the saturation regime and are then plotted vs. the maximum V_G used in each gate sweep. That V_G is varied from –20 to –100 V. V_D is kept constant at –100 V during all sweeps, in order to eliminate any effects that source and drain contact imperfections might have on our results. The mobility increases linearly with increasing Q_S and E and eventually saturates (Fig. 2a,b). Q_S is a function of the concentration of accumulated carriers in the channel region (N). Since the accumulation region has been shown in the past to be two dimensional and confined very close to the interface of the insulator with the organic semiconductor,[9] all of this charge is expected to be localized in the first few semiconductor monolayers from this interface. An increase in V_G results in an increase in E and N. However, for the same V_G, N depends on both the dielectric constant and thickness of the gate insulator while E depends only on its thickness.

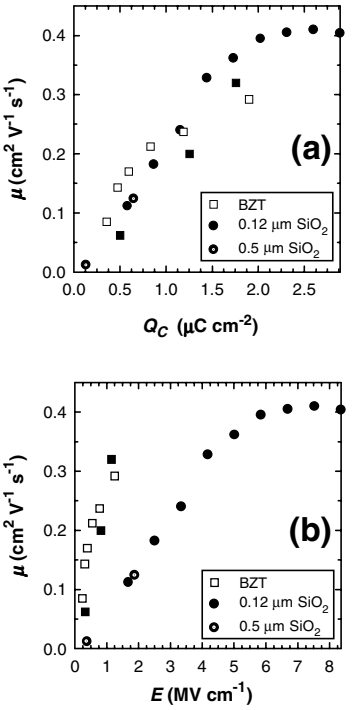

Figure 2

Using a sputtered Barium Zirconate Titanate (BZT) film as the gate dielectric, we have shown previously that N, not E, is the primary parameter involved in the mechanism that enhances the field effect mobility.[1] Using a solution processed BST film as the gate dielectric, we have also supported our previous arguments, despite the fact that a completely different fabrication process was used.[8]

The solution processed BST films had an ε about 4 times larger than that of SiO_2 (ε equal to 16 vs. 3.9, respectively) and a thickness of about 0.1 μm, close to that of the 0.12 μm thick SiO_2 gate insulator of the device corresponding to the solid black circles in Fig. 2a,b. By replacing SiO_2 with an insulator having a similar thickness but a much higher ε charge accumulation was facilitated. An accumulated carrier concentration similar to the SiO_2 case could be attained at much lower V_G, and hence E, with all the other parameters being similar. If mobility depends on N rather than E, then a high mobility should be achieved in the devices comprising the high ε gate insulator at much lower V_G, and hence E, than TFTs using a comparable thickness of SiO_2. Indeed, this is what we observe in Figure 3 which shows the dependence of I_D on V_G in the saturation region from a device using pentacene as semiconductor, BST gate insulator, aluminum gate and gold source and drain electrodes. μ was calculated from this plot to be 0.4 $cm^2\ V^{-1}\ sec^{-1}$ and I_{on}/I_{off} $3x10^5$. The gate voltage was kept below 5 V, which corresponds to a gate field less than 1 MV cm^{-1}. This is much smaller than the gate field of 6 MV cm^{-1} required in SiO_2 based devices to reach mobility of 0.4 $cm^2\ V^{-1}\ sec^{-1}$. s was approximately 0.3 volts per decade of current modulation. The threshold voltage was -2 V. L was 83 μm and W 1500 μm. Mobility values up to 0.6 $cm^2\ V^{-1}\ sec^{-1}$ were obtained from devices with smaller W/L ratios.

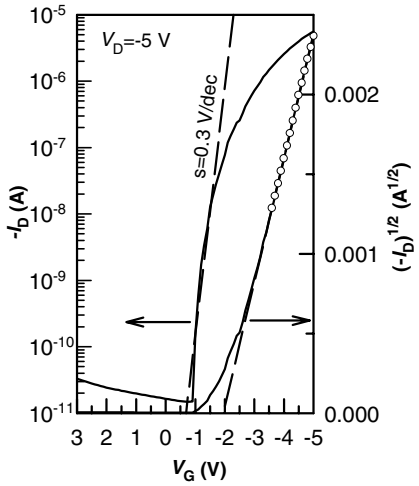

Figure 3

The squares in Fig. 2 correspond to devices comprising room-temperature sputtered BZT as gate insulator. The black squares are generated by gate sweeps while the white squares are generated by drain sweeps. The thickness of the BZT films used was between 0.12 and 0.13 μm in all devices in Fig. 2. From Fig. 2b it is obvious that the applied gate field used in BZT-based devices to obtain mobility values similar to those of the SiO_2-based devices was about four times lower compared to the fields used in the latter devices. This clearly proves that high field is not required to obtain high mobility. Thus, the gate voltage dependence of mobility in these devices is due to the higher concentration

of holes accumulated in the channel, which was achieved with the use of insulators with higher ε. Fig. 2a, which plots μ vs. charge per unit area, Q_s shows exactly that. The Q_s and N required to reach a certain mobility value is practically the same for SiO_2 and BZT-based devices although much different gate field values were required to obtain such mobility in each case. For both SiO_2 and BZT gate insulators, μ initially increases linearly with Q_s, and thus N.

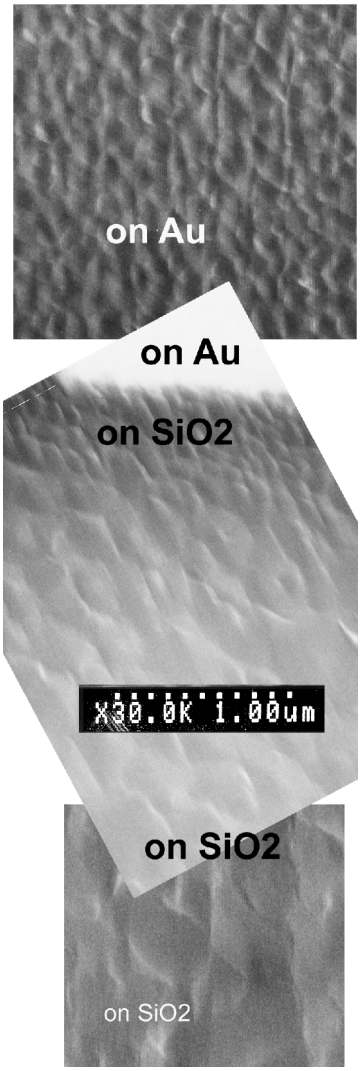

Figure 4

All steps in the fabrication process of our low voltage, rf-sputtered-BZT/pentacene-based TFT were performed at room temperature.[1] On the other hand, the sol-gel deposited BST gate insulators required annealing at 400°C, and although they produced excellent device characteristics they were not compatible with transparent plastic substrates.[8] The room temperature fabricated devices, are compatible with transparent plastic substrates. Given their operating characteristics, which are very close to the characteristics of the widely used a:Si-H TFT, they are good candidates for applications involving AM-LCD or AM-OLED displays on plastic substrates. We have demonstrated the feasibility of such applications, by successfully fabricating high performance pentacene based TFT on transparent plastic substrates such as polycarbonate requiring low operating voltages.[1]

Pentacene transistor drain-source contacts can be made in one of two configurations (Fig. 1a,b): top contact and bottom contact. Pentacene devices with the bottom contact configuration have inferior performance to devices with the top contact configuration. Consequently, most high performance pentacene TFT reported in the literature have the top contact configuration and shadow masking is generally used to pattern the source and drain contacts on top of pentacene. This is a process that cannot be used in manufacturing. A process that allows the photolithographic patterning of the source and drain electrodes on the insulator before the deposition of pentacene, according to the schematic on Fig. 1b had to be developed. Furthermore the performance of devices fabricated with such process should be similar to or better than top contact devices (Fig. 1a). Figure 4 shows the pentacene layer as it was grown on SiO_2 and on the Au electrode. The edge of the Au is marked by the border of the white area in the middle photograph (due to image contrast reasons the pentacene-covered Au is colored differently in the two top photographs). On SiO_2, far away from the Au edge, pentacene consists of fairly large grains, having sizes between 0.2 to 0.5 μm. On Au the grain size falls dramatically. Close to the Au edge but on the SiO_2 side there is a transition region where the grain size increases with the distance from the edge.

In an organic FET, the structure and contact behavior of the film formed on top of most of the electrode is not important for the performance of the device in the channel. It is the crystalline structure of pentacene at the electrode edge which causes the performance limitation of the bottom contact TFT. Right at the edge of the Au electrode there is an area with very small crystals and hence a large number of grain boundaries. Grain boundaries contain a lot of morphological defects, which in turn are linked to the creation of charge carrier traps associated with levels lying in the band gap. These defects can be considered responsible for the reduced performance of bottom contact pentacene TFT. Their elimination should result in bottom contact devices with performance similar to or better than top contact devices. Figure 5 corresponds to a typical bottom-contact pentacene TFT. The mobility calculated from this device is 0.16 $cm^2 V^{-1} sec^{-1}$. In a different device, we have used a self-assembled monolayer (SAM) of 1-hexadecane thiol to modify the surface energy of the Au electrode in an effort to improve the crystal size and ordering of the pentacene overgrowth.[10] Figure 6 corresponds to a bottom contact pentacene TFT which had its Au source and drain electrodes treated with such a SAM. SAM deposition parameters and other details will be published elsewhere. The mobility calculated from this figure is 0.48 $cm^2 V^{-1} sec^{-1}$, which is 3 times larger than the device with untreated Au electrodes. The pentacene layers for both devices were deposited in the same deposition run.

Figure 7 provides an explanation for the improvement in device performance. The pentacene grain size on the SAM-modified Au is similar to the large grains grown on the SiO_2. There is no transition region at the Au edge. The trap concentration must have beeen drastically reduced.

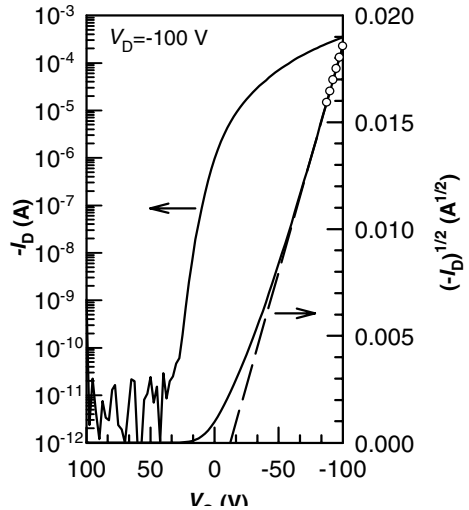

Figure 5

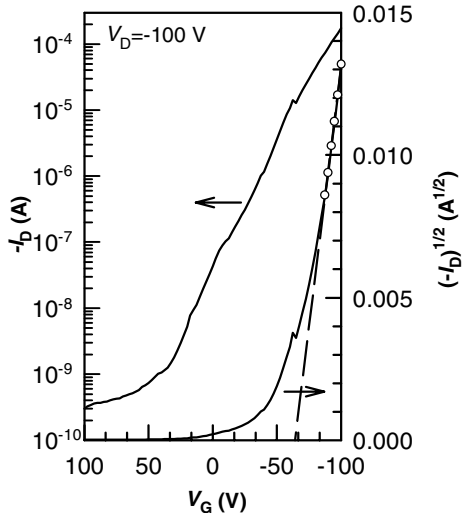

Figure 6

Pentacene is intolerant - after deposition - to exposure to the various chemicals used in typical lithographic processes. Therefore it cannot be patterned using such processes. Usually, shadow masks are used during deposition to pattern the material. Recently,[11] a technique was proposed which uses topographic discontinuities to isolate the devices. This technique requires that the semiconducting material and the photoresist remain in inactive areas, which can be a severe limitation for many applications. We have developed a subtractive technique in which pentacene is protected from the consequent lithographic steps by means of a chemically resistant layer. An 1 μm thick layer of parylene-N was used to protect the sensitive pentacene layer from solvents, etchants and other materials used in lithography. The two layer structure thus formed is then etched using a typical lithographic process. Photoresist is spun on top of the structure, and cured. The sample is then exposed through a lithographic mask to UV radiation, and developed. The structure is then etched for 30 minutes in an oxygen plasma, resulting in well defined patterns of protected pentacene on a clean substrate. Pentacene TFT made with this method had performance similar to shadow-mask patterned pentacene.

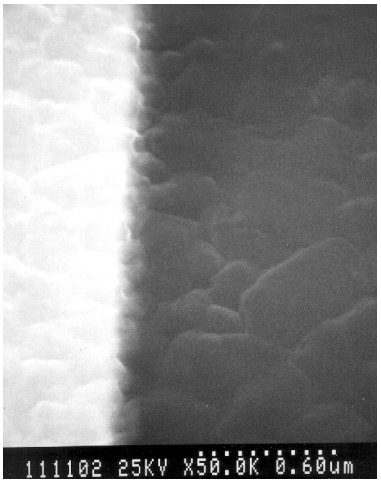

Figure 7

References

1. C. D. Dimitrakopoulos, S. Purushothaman, J. Kymissis, A. Callegari, J. M. Shaw, Science **283**, 822, (1999).
2. A. Tsumura, H. Koezuka, T. Ando, Appl. Phys. Lett. 49, 1210, (1986).
3. F. Ebisawa, T. Kurokawa, S. Nara, J. Appl. Phys. **54**, 3255, (1983).
4. C. D. Dimitrakopoulos, B. K. Furman, T. Graham, S. Hegde, S. Purushothaman, Synthetic Metals **92**, 47, (1998).
5. G. Horowitz, *Advanced Materials* **10**, 365, (1998).
6. F. Garnier, R. Hajlaoui, A. Yassar, P. Srivastava, Science **265**, 1684, (1994).
7. Y. Lin, D. J. Gundlach, S. Nelson, T. N. Jackson, IEEE Trans. Electron Devices **44**, 1325, (1997).
8. C. D. Dimitrakopoulos, J. Kymissis, S. Purushothaman, D. A. Neumayer, P. R. Duncombe, R. B. Laibowitz, Adv. Mater. **11**, 1372-1375, (1999).
9. A. Dodabalapur, L. Torsi, H. E. Katz, Science **268**, 270, (1995).
10. J. Kymissis, C. D. Dimitrakopoulos, S. Purushothaman to be published.
11. C. Py, M. D'Iorio, B. Williams, J. Fraser, M. Gao, M. Roussy. Abstracts of the MRS 1998 Fall Meeting, p 374.