

Evaluation of SOI Lock-in Pixels with Improved Modulation Contrast

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Abstract. Time-resolved imaging requires image sensors with high-speed modulation and a thick sensing layer for high sensitivity to near-infrared light and high-energy photon and particle detection. A solution is a lock-in pixel based on a silicon on insulator (SOI) with a fully depleted thick substrate; however, such pixels face challenges from degraded modulation contrast due to high parasitic light sensitivity (PLS) in the floating diffusion region. This work presents a pixel architecture that suppresses the PLS while preserving fast charge transfer by introducing a shallow buried channel and intermediate gates that enhance the lateral electric field. A prototype four-tap pixel array was fabricated using 0.2 μm SOI technology and experimentally characterized under 940 nm pulsed laser illumination. The proposed structure achieved a modulation contrast of 92.5% and PLS below 1.2% under 40 ns gate-pulse operation, maintaining stable performance up to 35,000 electrons per pulse, demonstrating suitability for X-ray and electron-beam imaging.

Keywords: CMOS image sensor, SOI detector, time of flight, parasitic light sensitivity, electron-beam detection

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1. INTRODUCTION

Lock-in pixel image sensors, which enable high-speed electronic shuttering synchronized with an optical source, are being actively developed for a variety of applications, including time-of-flight (ToF) imaging [1–10], fluorescence lifetime imaging [11–13], time-resolved near-infrared (NIR) spectroscopy [14], and non-contact heart rate detection [15, 16]. One of the key challenges for such lock-in pixels is achieving

high sensitivity in the long-wavelength region while maintaining the high-speed electronic shutter function.

To enhance sensitivity to NIR light, the authors have proposed a pixel structure that enables lock-in detection based on a silicon-on-insulator (SOI) pixel sensor [17–20] featuring a thick depletion region. The SOI lock-in pixel is designed to fully deplete a substrate thicker than 100 μm , which allows for a quantum efficiency exceeding 90% in the NIR range. Compared to recently reported structures that use multiple reflections within deep trench isolation layers [4], the proposed design offers even higher quantum efficiency. The thick absorption layer is also attractive in applications such as X-ray [15–21] and electron-beam detection [22].

However, the previous pixel structure [10] is constrained by a low modulation contrast (MC) mainly due to the high parasitic light sensitivity (PLS) of floating diffusion (FD) regions. At specific values, this leakage mechanism accounts for the measured PLS exceeding 13%, which leads to a low modulation contrast of approximately 58%. The issue arises from the fundamental potential design and cannot be sufficiently resolved by the optimization of doping energy and/or concentration. In this study, we present an SOI-based lock-in pixel with improved modulation contrast. The newly proposed structure [23] has a shallow buried channel to enhance the charge-shielding capability of FDs to improve the modulation contrast. In our previous study [23], the effectiveness of the proposed structure was verified through device simulations. This paper presents the fabrication and experimental evaluation of the proposed pixel, focusing on its modulation contrast performance. As a result, the proposed

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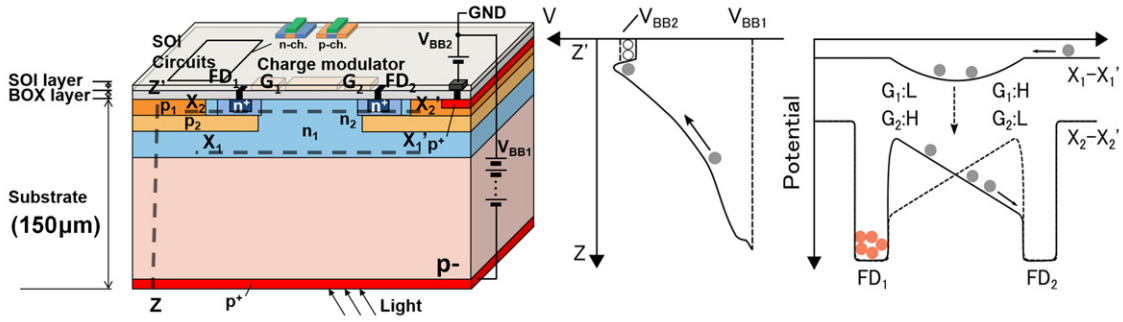


Figure 1. The SOI-based lock-in pixel structure. Concept of potential design for the proposed SOI-based lock-in detector (two-tap).

pixel achieves a modulation contrast of 92.5% with a PLS below 1.2% under pulsed operation. Compared with the conventional pixel, this corresponds to an 11.4 \times reduction in PLS and a 1.6 \times increase in MC.

The remainder of this paper is organized as follows. Section 2 describes a brief overview of the SOI lock-in pixel and the issue with the previous structure. Section 3 details the proposed pixel structure and a prototype chip. Section 4 reports the measurement results of the prototype chip. The conclusion is presented in Section 5.

2. AN SOI-BASED LOCK-IN PIXEL STRUCTURE

2.1 Overview of the SOI-based Lock-in Pixel

Figure 1 shows a conceptual diagram of a previously developed SOI-based lock-in pixel [10] and its potential diagrams. The SOI-based lock-in pixel was developed based on SOI pixel technology [17], where the substrate is used as a sensing layer. For high sensitivity and fast response, the thick substrate is fully depleted by applying a substrate bias (V_{BB1}). Similar to SOI pixel technology [17], the SOI-based lock-in pixel exhibits inherent radiation hardness [24, 25] due to the thick substrate. The combination of this feature and high-speed lock-in operation (viz., electronic shuttering) is attractive for applications such as time-resolved X-ray imaging [21] and high-speed direct electron detection [22].

The modulation gates are formed on top of the buried oxide (BOX) layer using $n+$ or $p+$ layers, which serve as the source/drain active layers in standard SOI transistors. This SOI gate structure allows modulation of the channel potential, thereby enabling charge modulation functionality. The center gate (G_c) is biased to a constant negative voltage while the modulation gates (G_1 , G_2 , G_3 , and G_4) are driven with negative gate pulses (e.g., -7 V to -3 V), creating a buried channel beneath the gates. In particular, when the modulation gates are set low, the front-surface potential is pinned to the front-surface bias, V_{BB2} . The n_1 layer also plays an important role in preventing leakage current between the front-side p -type layers (p_1 and p_2) and backside p -type substrate. The p_1 layer is formed beneath the BOX layer to suppress generation current and back-gate effects, ensuring the stable operation of SOI circuits [17]. The p_2 layer creates a potential barrier under $n+$ layers (FDs) to suppress the PLS.

2.2 Conventional Pixel Structure and its Issue

Figure 2 shows the four-tap implementation of the SOI lock-in pixel and its corresponding simulated potential distributions. As described previously, the conventional structure exhibits significant PLS. This issue primarily arises because the buried channel (n_1) is located relatively deep within the substrate, and a highly doped n_2 region is required to connect the buried channel to the FDs. The high doping concentration in the n_2 region weakens the potential barrier formed by the p_2 layer. This results in a residual connection between the buried channel and the FDs even when the corresponding modulation gate is turned off. As a result, signal electrons generated under off-state gates or near the pixel edges can leak into unintended FDs, leading to large PLS.

The device simulation results in Fig. 2(b) explain this behavior. Electrons generated at positions A and B are correctly collected by FD₁, whereas electrons generated at C, D, and E are incorrectly collected by the off-state FD due to the insufficient potential barrier. Figure 3 shows an example of the measured modulation characteristic of the conventional pixel. The results were obtained using a 100 ps short-pulse light source at 930 nm, and the modulation gates were set at 40 ns. The outputs of the four taps (G_1 – G_4) are plotted along with their sum. It can be seen that each tap exhibits a constant offset of approximately 13% of the total signal even when the corresponding modulation gate is off. This offset represents PLS since some electrons generated within the pixel are partially collected by the off-state FDs. This leakage mechanism accounts for the measured PLS exceeding 13%, which leads to a low modulation contrast of approximately 58%.

3. PROPOSED PIXEL AND FABRICATED CHIP

3.1 Proposed Pixel Structure

The proposed SOI-based lock-in pixel was developed to suppress PLS and improve modulation contrast. In this design [23], the buried channel structure of the conventional pixel is significantly modified. The central region of the n_1 layer is removed, and an additional n_3 layer with lower implant energy is introduced to form a shallower buried channel. This structural change enhances controllability of the potential by the modulation gates and allows the p_2 barrier under the FDs to be formed more effectively.

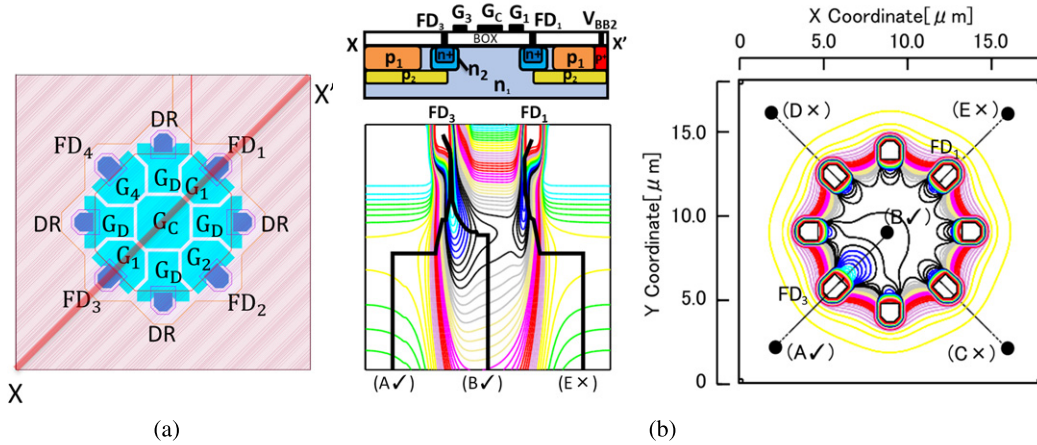


Figure 2. The SOI-based lock-in pixel in the previous design: (a) pixel layout with four floating diffusions (FD₁-FD₄) and transfer gates (G₁-G₄); (b) simulated potential cross-section along X-X' showing the buried channel (n_1) and a weak barrier under the p_2 region. Electrons from positions A and B (✓) are correctly collected while those from C-E (x) leak to other FDs, causing PLS.

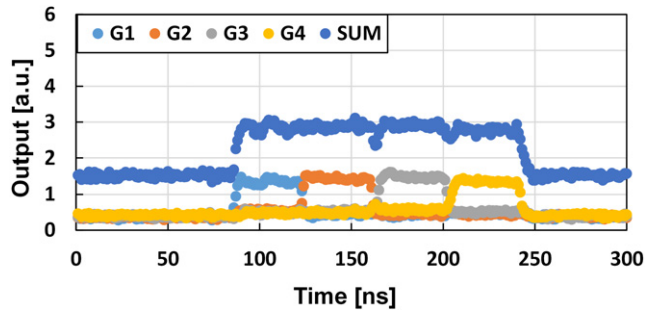


Figure 3. Modulation characteristics of the previous structure. A short-pulse light source with approximately 100 ps width and 930 nm wavelength was used. The gate-pulse width was set at 40 ns. A large PLS was observed as an offset.

However, a shallow buried channel weakens the lateral electric field near the surface, which is essential for high-speed charge transfer in lock-in operation. To address this issue, the proposed pixel also introduces intermediate gates (G_{C1} - G_{C4}) between the center gate (G_C) and the modulation gates (G_1 - G_4) as shown in Figure 4(a) [23]. These intermediate gates smooth the lateral potential distribution in the buried channel and generate a lateral electric field as shown in Fig. 4(b). Figure 5 shows simulated one-dimensional and two-dimensional potential distributions with and without the intermediate gates. Without the intermediate gates, a small potential dip appears due to the weakened fringing field. The dip is eliminated by introducing the intermediate gates, resulting in a smoother potential profile and a stronger lateral electric field. This enables high-speed charge transfer while maintaining low PLS.

The timing diagram of the proposed pixel in a four-tap ToF operation as an example is illustrated in Figure 6. The modulation gates (G_1 - G_4) are sequentially turned on in synchronization with the incident light pulses while the intermediate gates (G_{C1} - G_{C4}) are also driven with

slightly delayed pulses relative to their neighboring modulation gates.

Although the shallow buried channel and intermediate gates effectively improve the modulation contrast and suppress PLS, potential trade-offs should be noted. To form the shallow channel, the proposed pixel requires one additional mask and process step. In addition, driving the intermediate gates may slightly increase power consumption; however, this increase can be limited because the required switching speed of the intermediate gates is lower than that of the modulation gates. Another possible issue is that the proposed structure requires careful alignment between the n_1 and p_2 layers, which can affect yield. For this issue, further investigation is necessary to optimize the layout, doping profiles, and driving pulse voltages.

3.2 Implemented ToF Sensor Chip

Figure 7 shows the die micrograph of the implemented ToF sensor fabricated using 0.2 μm SOI technology. The pixel array consists of 70 (H) \times 170 (V), with a pixel pitch of 18 μm \times 18 μm . The sensor integrates a four-tap gate driver (G_1 - G_4 , G_D), the pixel array, vertical and horizontal scanners, and a column-parallel readout circuit with correlated double sampling. After column-wise signal scanning by the H-Scanner, analog signals are externally digitized using a 14-bit analog-to-digital converter.

4. EVALUATION RESULTS

4.1 Output and PLS Under DC Illumination

The photoresponse of the proposed SOI-based lock-in pixel was measured under DC illumination to evaluate the linearity of each tap and to assess the PLS. A 940 nm laser operating in DC mode was used as the light source. Figure 8 shows the measurement results, where one modulation gate was set high while the others were set low. The outputs represent the average of 885 pixels. A clear difference between the high-state and low-state tap outputs was observed. Table I

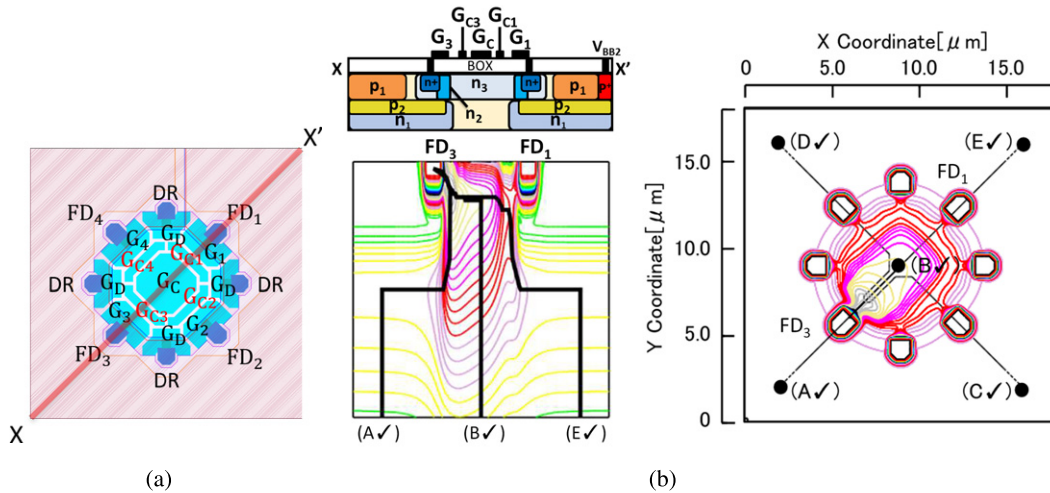


Figure 4. SOI-based lock-in pixel in the proposed design: (a) pixel layout with four floating diffusions (FD₁–FD₄) and transfer gates (G₁–G₄); (b) simulation result.

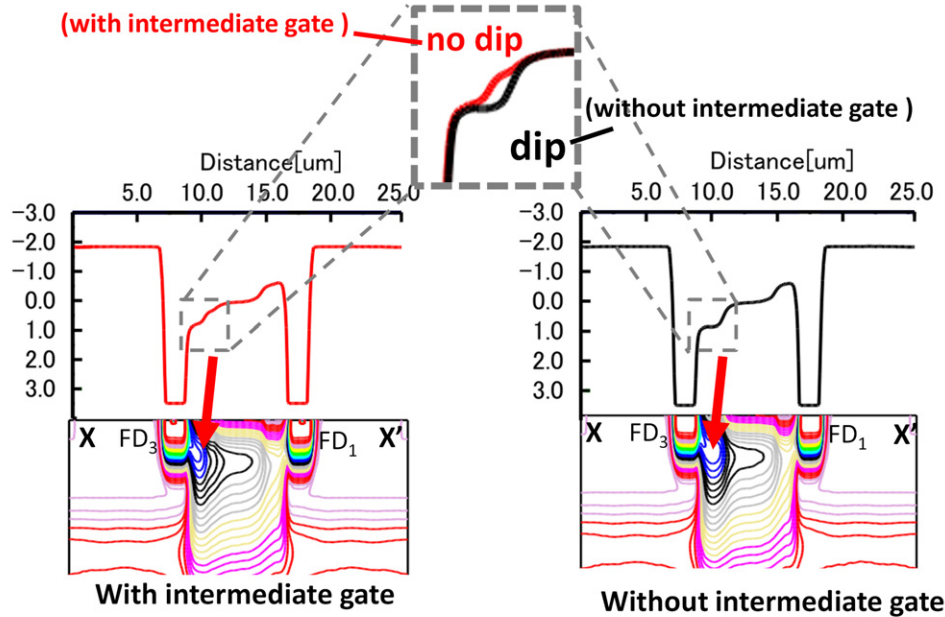


Figure 5. Simulated potential distribution along the transfer path. Red (solid): with intermediate gates; black (dashed): without intermediate gates. Without intermediate gates, a local potential dip appears and the lateral field is weak. With intermediate gates, the potential transition becomes monotonic and the lateral field is strengthened, enabling faster charge transfer.

summarizes the resulting PLS values for each condition, showing that the PLS was effectively reduced to below 2.9%. Notably, when only G_2 was turned on, the PLS was further suppressed to as low as 1.13%. The PLS variation among taps may occur due to differences in the potential barrier under the gates when they are turned off. One possible cause is the mask alignment error between the doping layers, such as p_2 and n_2 . This issue will be further investigated and optimized in future layout revisions.

The measurement results of dark current at 27°C are summarized in Table II. The measured dark currents are 8.5×10^4 , 8.9×10^4 , 6.7×10^4 , and 8.4×10^4 e^-/s for G_1 ,

Table I. Summary of the PLS values for each tap calculated under static DC illumination conditions.

| ON gate | G_1 | G_2 | G_3 | G_4 |
|---------|-------|-------|-------|-------|
| PLS (%) | 2.89 | 1.13 | 2.86 | 2.27 |

G_2 , G_3 , and G_4 , respectively. Here, the conversion gain is assumed to be $10 \mu V/e^-$. During the measurement, a modulation gate pulse of 40 ns with a repetition period of 520 ns was applied. Since the sensor operates in global-shutter

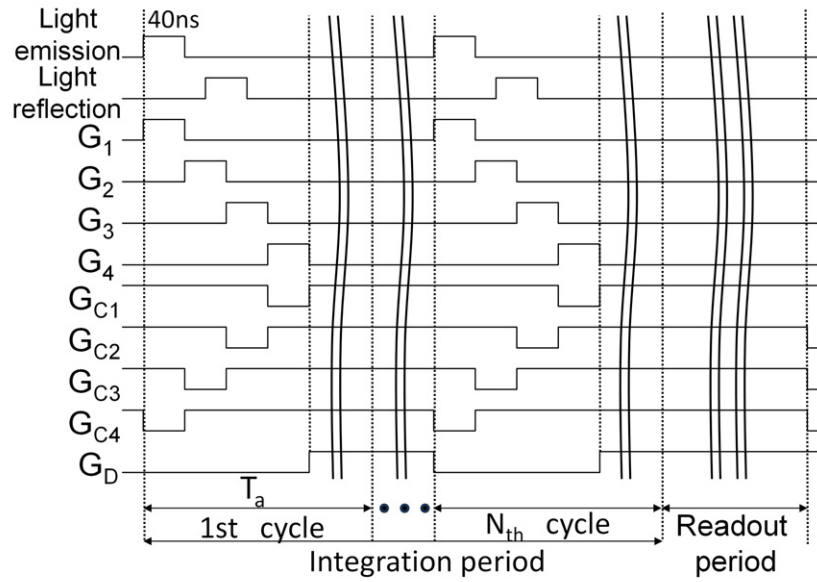


Figure 6. The timing diagram for the four-tap lock-in pixel with intermediate-gate-assisted operation.

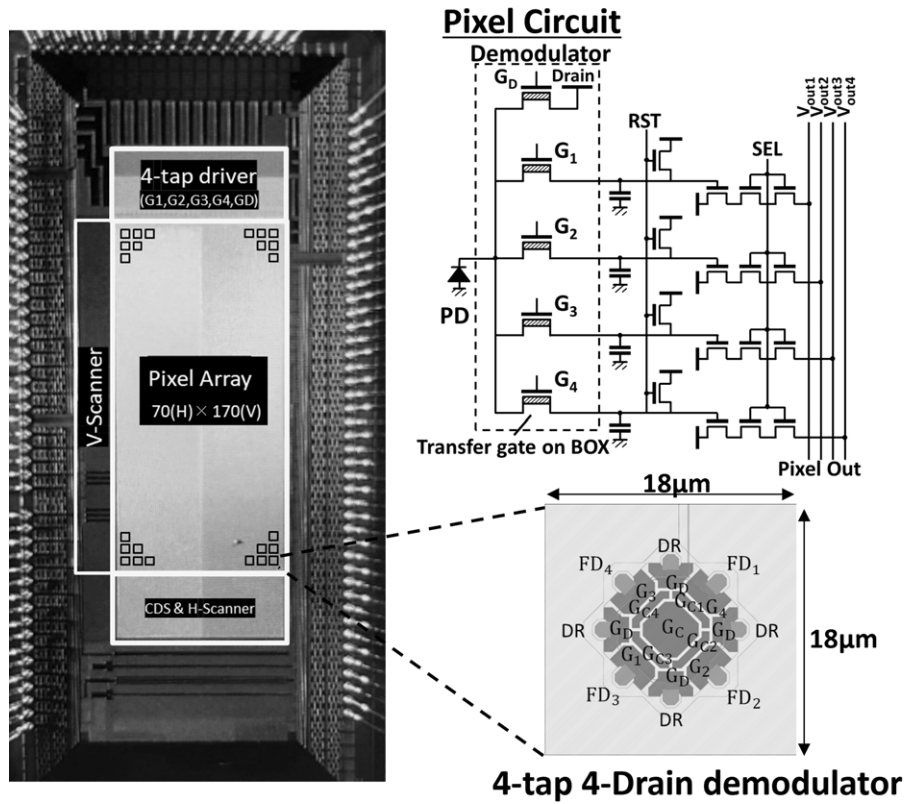


Figure 7. Prototype chip photograph, pixel circuit, and demodulator.

mode, the dark current generated in the FD region is also included in these results.

4.2 Modulation Contrast Characteristics

The modulation characteristics of the proposed pixel were evaluated under pulsed illumination. A 940 nm short-pulse laser (LDB-160B, Tama Electric Inc.) with a pulse width of 100 ps and a repetition period of 520 ns was used as the light

Table II. Estimated FD-hold dark current for each tap obtained from the mean slope of FD voltage decay during light-off intervals (assuming $CG = 10 \mu\text{V}/e^-$).

| Gate | G_1 | G_2 | G_3 | G_4 |
|--------------------------|-------------------|-------------------|-------------------|-------------------|
| Dark current (e^-/s) | 8.5×10^4 | 8.9×10^4 | 6.7×10^4 | 8.4×10^4 |

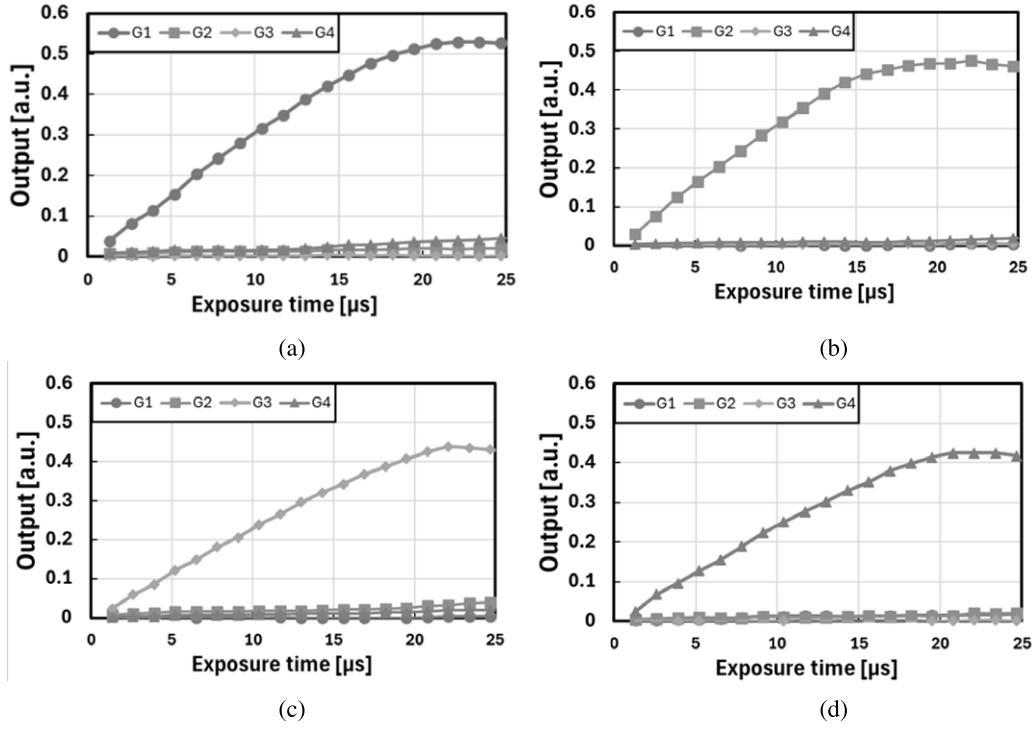


Figure 8. Measured photoresponse under DC illumination where only one modulation gate is set high in each condition during the accumulation phase: (a) G_1 is high; (b) G_2 is high; (c) G_3 is high; (d) G_4 is high. All other gates are set low. The gate G_D is set high during the readout phase.

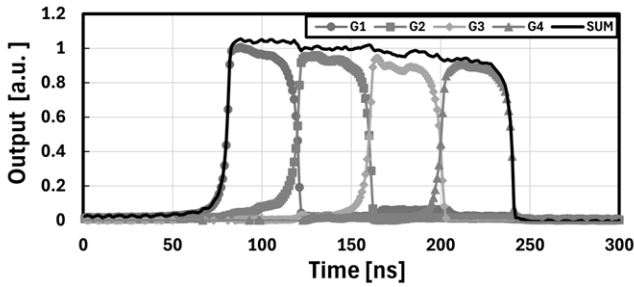


Figure 9. The modulation characteristics in the intermediate-gate-assisted condition (normal operation as shown in Fig. 6).

source. The laser trigger delay was scanned from 0 to 300 ns in steps of 1 ns, and the modulation gate pulse was set at 40 ns. To demonstrate the effectiveness of the intermediate gates, two operation conditions were evaluated: intermediate-gate-assisted operation (normal operation as shown in Fig. 6) and non-assisted operation (where the intermediate gates are set low during the accumulation phase). The measurement results are shown in Figures 9 and 10, respectively.

Under the intermediate-gate-assisted operation, high-speed modulation was observed and the outputs of off-state gates corresponding to PLS remained low. In contrast, the non-assisted operation showed slow modulation, particularly at the rising edges of the modulation characteristics. The rising edges in the modulation characteristics correspond to the falling edges of the light pulse and the associated photocurrent response, suggesting that the low-speed

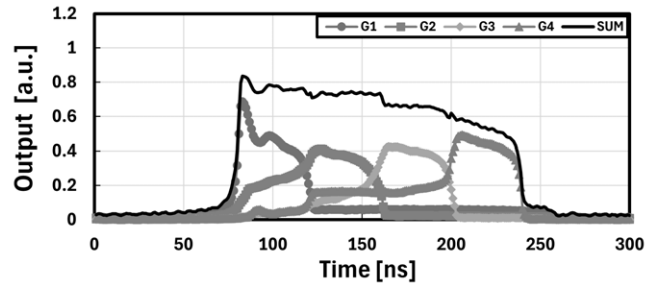


Figure 10. The modulation characteristics in the non-assisted operation (where the intermediate gates are set low during the accumulation phase).

operation may result from a weakened lateral electric field operation.

The average PLS from the modulation characteristic with the intermediate-gate-assisted operation was 1.2%, and the modulation contrast, defined later in Eq. (1), was measured to be 92.5%. In the non-assisted operation, the average PLS increased to 5.2% and the modulation contrast decreased to 43.9%. These results are better than those of the previous structure, demonstrating that the combination of the shallow buried channel and intermediate-gate-assisted operation enables both high-speed modulation and low PLS.

The modulation contrast is calculated as follows:

$$MC = \frac{1}{4} \sum_{i=1}^4 \left[\max \left(\frac{2S_i - S_{SUM}}{S_{SUM}} \right) \right], \quad S_{SUM} = \sum_{k=1}^4 S_k, \quad (1)$$

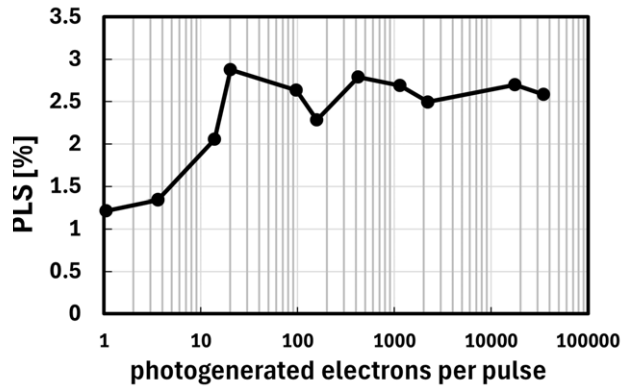


Figure 11. Average PLS of the four taps as a function of the number of photogenerated electrons per pulse.

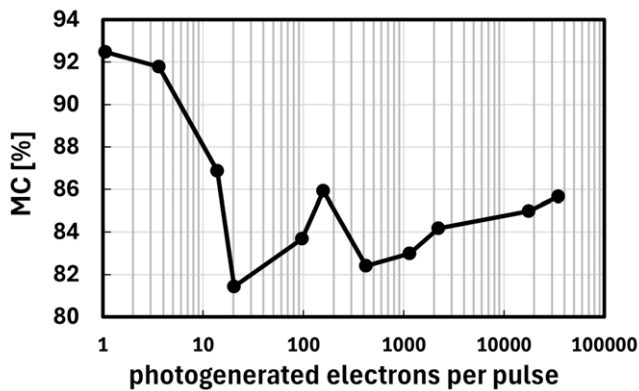


Figure 12. Measured MC versus photogenerated electrons per pulse.

where S_i is the output of the i th tap and S_{SUM} is the sum of all four tap outputs. Unlike [26], our sensor employs a four-tap modulation scheme using short light pulses (i.e., not a 50% duty cycle). Therefore, we adopted the extended definition shown in Eq. (1), following the approach of [10].

4.3 Modulation Characteristics at High Signal Levels

In applications such as X-ray or electron-beam detectors, a single incident electron can generate a large number of signal electrons. To emulate this scenario, modulation measurements were conducted under various incident laser power conditions corresponding to different levels of signal injection per pulse. In this measurement, the number of photogenerated electrons per pulse (e/pulse) owing to short-pulse laser irradiation was varied with a beam splitter, and both the average PLS and the modulation contrast were evaluated. Figures 11 and 12 show the results of the leakage and modulation contrast as a function of photogenerated electrons per pulse. The conversion gain is assumed to be $10 \mu\text{V}/\text{e}$. The modulation characteristic remained correct even at approximately 35,000 electrons per pulse, and the PLS was negligibly small. The modulation characteristic measured at approximately 35,000 electrons per pulse is shown in Figure 13, demonstrating that the pixel operates correctly even under near-saturation conditions.

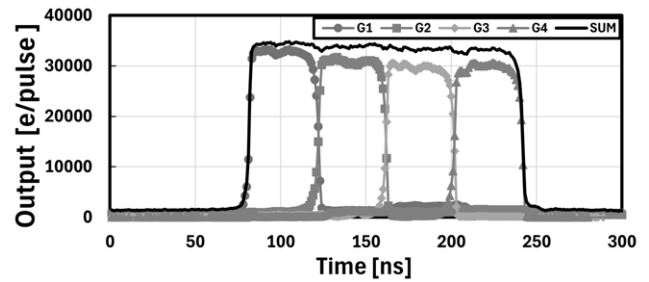


Figure 13. Modulation characteristics at a high number of photogenerated electrons (35,000 e/pulse).

5. CONCLUSIONS

We have developed and evaluated a four-tap SOI-based lock-in pixel structure that combines a shallow buried channel with intermediate gates to improve modulation contrast and suppress PLS. Experimental results demonstrated low PLS under both static and pulsed illumination. The proposed pixel achieved a modulation contrast of 92.5% with a PLS of only 1.2%, significantly outperforming the conventional design. Furthermore, the pixel maintained stable operation under high signal injection conditions—up to approximately 35,000 electrons per pulse—with minimal performance degradation. These results confirm that the proposed pixel is well suited for high-sensitivity, high-speed imaging applications, including ToF range imaging, X-ray sensing, and direct electron detection.

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