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Geometric Design and Compensation Rules Generation and Characterization for All-Inkjet-Printed Organic Thin Film Transistors

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Abstract. *Rules for geometric design and compensation aim to guarantee that layout representations match final printed patterns within an accepted tolerance for a desired process yield. The more conservative the rules, the better the yield. Therefore, for a given process and after an experimental extraction of the required process parameters, it is possible to derive minimum design rules that characterize the technological process to a point where, without necessarily having an in-depth knowledge of the process and materials involved; design engineers can address physical design in order to develop devices and systems. In this article, a methodology for the extraction and characterization of inkjet geometric design rules and the application of compensation techniques to permit the inkjet manufacturing of reliable and precise designs is proposed as a first step towards separating design from digital fabrication, in a similar way to what has already occurred in silicon microelectronics technology. © 2013 Society for Imaging Science and Technology.*
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INTRODUCTION

Inkjet printing is a challenging technique that will lead to a new paradigm in digital fabrication through the construction of electronic devices and circuits created 'drop by drop'. Designing devices and circuits requires a wide knowledge of the aspects of the process and a complex interaction between concepts, tools and processes originating in different science and engineering disciplines. Process and design engineers already addressed this challenge a number of years ago at the earliest stages of the development of silicon microelectronics technology.

In the late 1970s, the Mead–Conway design rules concept[1] revolutionized Integrated Circuit (IC) design. The idea was to abstract physics to a point at which design engineers could address physical design with sufficient certainty without a detailed knowledge of the fabrication technology.

Our work is based on the experience of the microelectronic silicon foundry model, and the concept of the Process Design Kit (PDK) as being the nexus between design and technology.[2] A PDK comprises a set of technology files related to specific device models which are used to accurately describe manufacturing process details to design engineers and are integrated in Electronic Design Automation (EDA) tools containing geometrical and electrical design rules, device technology parameters and simulation models. However, although the concept can be adopted, and tools and knowledge recycled, a new approach must be considered in order to take into account the particular challenges involved in inkjet printing.

Geometric design rules aim to guarantee that layout representations match final printed patterns within an accepted tolerance for a desired process. Thus, for a given process and after an experimental extraction using specific test patterns and a compensation methodology to increase the achievable resolution and pattern transfer fidelity, we will be able to find the minimum intra- and inter-layer design rules for our process.

INKJET PRINTING EFFECTS

In printed electronics, the intrinsic characteristics of functional materials lead to different constraints on device technology. Different research articles[3,4] have demonstrated the need for improving the pattern control of inkjet-printed lines and areas. By characterizing the conditions or parameters that lead to different printed morphologies, electronic devices can be improved in terms of their electrical performance.

As an example of printing behavior, a number of representative effects of inkjet-printed features are reviewed in Figure 1. The discrete drop nature of inkjet-printed shapes can create scalloping line behaviors, as depicted in Fig. 1(a). In addition, the balance between drop size, drop spacing and ink–substrate interaction can create a bulging effect,[5] as in Fig. 1(b).

Printing layer by layer directly affects the device performance because the preceding functional material deposited modifies the expected morphologies of the subsequent layers, as illustrated in Fig. 1(c).

Let us consider the printing of a complex device such as an Organic Thin Film Transistor (OTFT), as shown in Figure 2(a). OTFTs are excellent candidates for use in low-cost fabrication and large area production, because they allow for the construction of blocks such as logic gates and more complex circuits. OTFTs have been fabricated with various device geometries, but essentially consist of (1)

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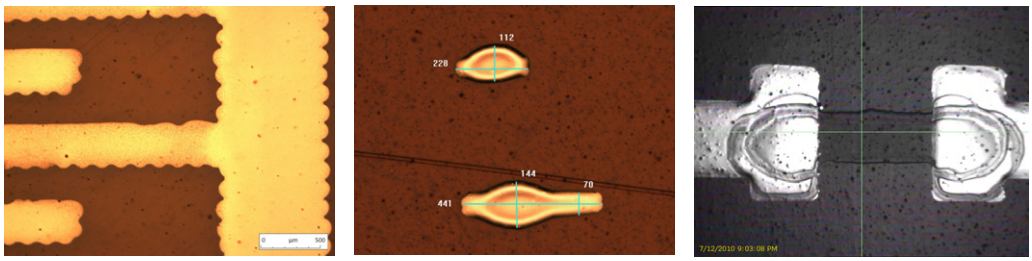


Figure 1. Different printing behaviors.

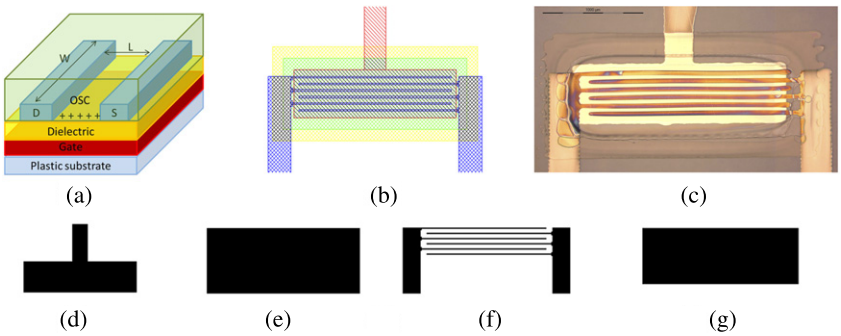


Figure 2. (a) OTFT structure; (b) OTFT layout design; (c) image of an all-inkjet-printed OTFT; (d) gate contact layer pattern; (e) insulator layer pattern; (f) source/drain layer pattern; and (g) semiconductor layer pattern.

narrow lines acting as drain–source electrodes (see Fig. 2f); and (2) areas which work as gate, insulator and organic semiconductor layers (see Figs. 2d, e and g). The printed morphology of these lines and areas is one of the key factors for improving the electrical characteristics of the OTFT. In fact, printing parameters can be fine-tuned in order to obtain optimal morphologies despite the printability of functional materials. To explain the relationship between the electrical characteristics of an OTFT and the device geometry, it is necessary to take into consideration all parameters that affect the transfer characteristic in the saturation regime, as shown below in Eq. (1). This simplified equation does not capture the behavior in terms of changes in gate leakage, parasitic series resistances and capacitances. These parameters need to be considered in more complex device models.

$$I_{DS} = \mu \cdot C_i \cdot \frac{W}{L} \cdot \frac{(V_G - V_T)^2}{2}. \qquad (1)$$

Variations in the channel length (L) due to scalloping of the lines (Fig. 1a) or in channel width (W) as a result of the non-desired geometry produce a modification in the transfer curve characteristic and thus introduce variability amongst OTFT devices[6] and finally logic gates. Besides variation in lines and areas, the layer thickness also plays an important role, for example both in the gate capacitance (C_i) and the gate leakage current.

In this article, we propose the technology optimization and characterization methodology for the extraction of design rules related to OTFTs, but this can also be applied to other devices (e.g. passive devices, antennas, sensors etc.). This approach aims to achieve a good match between the designed and inkjet-printed geometric relations, as respectively shown in Figs. 2(b) and (c). An interesting alternative is also proposed for reducing layer thickness by means of tuning the drop lattice.

METHODOLOGY OF TECHNOLOGY CHARACTERIZATION

For the generation of design rules, we need a concise description of process characteristics. This is achieved through the technological characterization of the geometries and morphologies of printed patterns. The quantitative relation between designed patterns and printed dimensions is the key factor in this, as discrete inkjet printing resolution and inkjet spot-based patterning restricts pattern generation.

We have developed a methodology to optimize the morphology of the printed lines and areas. Different parameters and characterization structures need to be considered in order to establish the optimal printing feature, prevent line instabilities and to obtain the design rules relating to the physical resolution limits of the manufacturing process.

In the field of printed technology, it is important to control the fidelity of the patterning feature in order to exactly reproduce the circuit layout. By defining the optimal patterning, we can define the design rules, such as the minimum width, spacing, notch and so on, in order to establish the minimum feature size that can be manufactured by the technology.

In order to avoid irregular pattern morphologies caused by deposition and curing processes, printed drop characterization and jetting optimization are both required. Once the single drop deposition has been optimized, the next

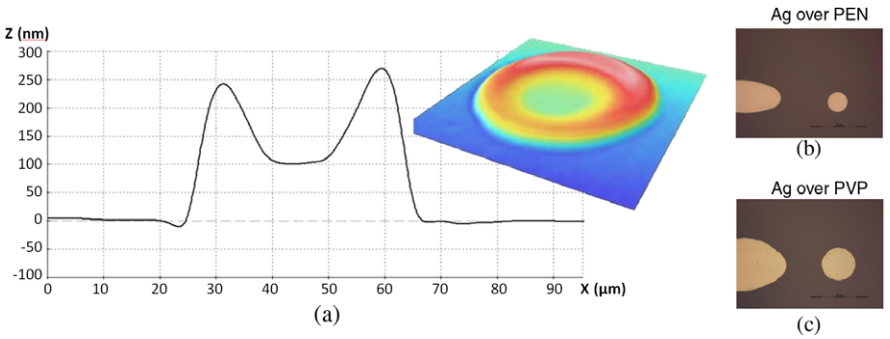


Figure 3. (a) 3D and sectional image of a sintered drop with coffee ring shape; (b) silver line and dot over PEN substrate; (c) silver line and dot over PVP insulator layer. N.B. images are at the same scale.

step is to control the behavior of the inkjet-printed lines and areas in order to determinate the final shape (the first methodology step). Although some printing parameters are controllable, the physical properties of ink cause a non-homogeneous distribution of deposited material. This characteristic of inkjet technology leads to the use of compensation techniques (the second methodology step) in order to ensure the ink coalescence allows for the proper transfer of the pattern. Having applied the aforementioned material characterization and compensation techniques, the printed pattern is totally optimized in terms of morphology and variability. Finally, the design rules (the third methodology step) for a particular ink can be established by means of pattern test structures. The overarching goal is to print lines that are as smooth, narrow and straight as possible. In the case of areas, the main issue that needs to be taken into account is achieving smooth edges. Different pattern test structures are required in order to obtain the minimum feature size such as width, spacing, notch and corners. The main goal of these structures is to take the technology to its limit whilst mitigating unwanted phenomena in the printed features.

MATERIAL CHARACTERIZATION

As inkjet printing technology involves a spot-based patterning system, the basic element is the deposited drop. Some examples reporting one-dimensional[3,4] and two-dimensional[7] models for printed line dimensions can be found in the literature. In this article, we will focus on the extraction of data for defined shapes by using an empirical method through the printing and characterization of test patterns. This method is costly, but it is useful for the generation of controlled pattern libraries for target applications.

An initial approach to printed pattern dimensions can therefore be conducted by using the following equation[8] where n is the number of deposited dots, DS the drop spacing, and D the spot diameter.

$$\text{Width} = (n-1)\cdot DS + D. \tag{2}$$

However, Eq. (2) can only be considered as offering an initial approach for estimating the dimensions of printed patterns prior to the physical characterization stage because it does not consider the overflow that may occur when ink density locally increases or where coalescence occurs. The nature of printed lines is complex and differences arise because of a number of factors in the process (e.g. ink–substrate interaction, drop spacing, jetting frequency etc.).

The coffee ring effect is a well-known phenomenon, and arises from fluid flowing from the center of a droplet toward the edge to compensate for evaporation losses,[9] as shown in Figure 3(a). Moreover, an example of the ink–substrate interaction is shown in Figs. 3(b) and (c), in which the silver line and drop morphology differ depending on the layers beneath it. To exemplify this, consider an OTFT bottom gate bottom contact structure: here the gate and drain–source electrodes will be differently patterned onto the substrate and the insulator layer.

It is reported in the literature that one can control the relative distribution of material across the printed line by controlling the substrate temperature and drop-on-demand delay.[5] Our work extends the research by means of tuning the drop lattice.[10]

Furthermore, some researchers[11–13] report on adjusting ejection parameters such as viscosity, ink concentration, surface tension, waveform of piezoelectric printhead and so on in order to obtain good bead expulsion without satellites or tails. We assume an optimized drop ejection since our work is focused on drop deposition instead of drop ejection.

The independent variables considered were:

- **Drop spacing**: Defined as the distance between two consecutively printed drops and scaled by the wetting diameter of the drop on the substrate.
- **Jetting frequency**: Inversely proportional to the delay period of the consecutive expelled beads. Clogs or misdirected drops limit the lower jetting frequency.
- **Drop lattice**: By modifying the pixel lattice in pattern design, one can geometrically adjust the amount of ink deposited per unit area.
- **Platen temperature**: Substrate temperature is related to the solvent evaporation rate, which subsequently affects ink spread and the coffee ring effect.

Various different combinations of parameters were used in order to optimize the deposition of material.

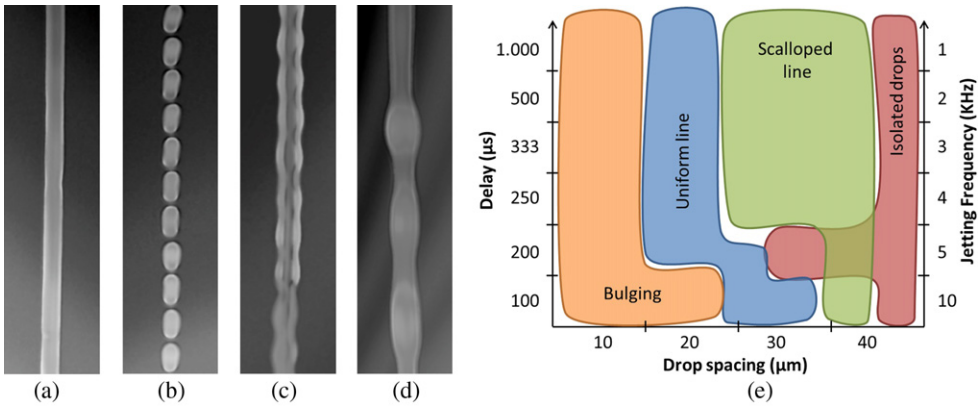


Figure 4. Examples of principal printed line behaviors: (a) uniform line; (b) isolated drops; (c) scalloped; (d) bulging; and (e) typical printed line behavior at intermediate temperature with DS increasing from left to right.

Experimental Material Deposition Optimization: The First Step in the Methodology

We conducted our experiments on a research inkjet Dimatix DMP2831 printer using piezoelectric drop-on-demand printheads with a 2 μm orifice ejecting 10 pL drops. Our stages have x, y, and rotational degrees of freedom with 15 μm repeatability. Operating in drop-on-demand and raster mode, our printer can work with jetting frequencies ranging from 1 to 10 kHz.

A conductive ink was selected for the material characterization and optimization of the critical impact of the drain and source electrodes to the OTFT performance, and its printing complexity in contrast to the organic semiconductor and insulator films. The conductive ink used was a 20 wt% silver nanoparticle content (Sunchemical Suntronic EMD5603); and poly(-4-vinylphenol) (PVP) with poly(melamine-co-formaldehyde) methylated (crosslinker) was used as an insulator. The characterization structures were printed on a flexible DIN-A4 size PEN substrate (DuPont Teijin Teonex ® Q65FA). Using our setup, the average diameter of the sintered silver ink drop measured was found to be 52 μm on top of the PEN substrate, and 34 μm on top of the insulator layer, as shown in Figs. 3(b) and (c). Because the drain and source are printed onto an insulator, the layer beneath the electrodes used for their characterization is the c-PVP.

An initial experiment was performed to optimize the behavior of the sintered printed lines. The independent variables used in this experiment are drop space and jetting frequency. The substrate is heated at intermediate temperature (40°C) and drop space varies between 5 and 40 μm center to center. Higher drop spaces were discarded for our silver nanoparticle ink, as it made no sense to use drop spaces bigger than the drop diameter.

A number of principal behaviors emerge when examining printed silver patterns across a variety of drop spaces and delay periods. These behaviors were first labeled by Soltman et al. as isolated drops, a scalloped line, a uniform line, a bulging line, and stacked coins. Though the final behavior is not observed in our printed patterns, Figures 4(a) to (d) show the other four basic morphologies.

At low DS, an overflowing irregular bead forms and isolated drops land at large DS. In some cases, isolated drops merge producing partially scalloped lines creating a combined behavior. Finally, the minimum drop-on-demand delay is approximately 1 ms (1 kHz) on our printer. Delays from 100 μs to 1 ms are appended. Upper delays become problematic because the ink has sufficient time to form a film skin at the nozzle. Once printed, the resulting patterns are measured and quantified with a mechanical stylus profilometer and by means of confocal and interferometric microscopy techniques (Sensofar PLu neox).

Fig. 4(e) schematically shows where each of these behaviors arises on a specific drop space and delay at an intermediate temperature. A smooth, narrow and uniform line is achieved for a limited range of drop spaces as a function of deposited spot diameter and jetting frequency. For the cases of drop spaces equal to drop diameter, the line edges are ridged following the boundary of the drop, giving a scalloped profile. If the drop space is even higher, isolated drops appears since there is no overlapping between drops regardless of the delay. In the case of a large amount of overlapping i.e. less than half of the drop diameter, bulges along the lines arise due to the excess of ink volume per unit of printed area. At a given DS, the line behaviors are not strongly affected by a delay larger than 250 μs. For lower delays, a uniform line is obtained by varying the drop space from 20 to 30 μm.

Using parameter values to obtain uniform lines (a drop space of 20 μm and a delay of 200 μs), a second experiment was performed focusing on an alternative group of parameters in order to optimize the homogeneity and cross-section. The independent variables used in this experiment were the substrate temperature, drop lattice, and printing orientation. As a degree of freedom, patterns were printed both in the printing direction (PD) and counter printing direction (CPD).

By modifying the drop lattice, we are changing the percentage of droplets of the line and providing a useful pattern characterization structure for the improvement of film homogeneity.

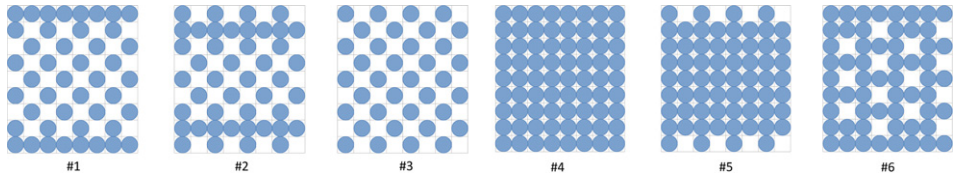


Figure 5. Different drop lattices evaluated. Images represent a portion of a horizontal line.

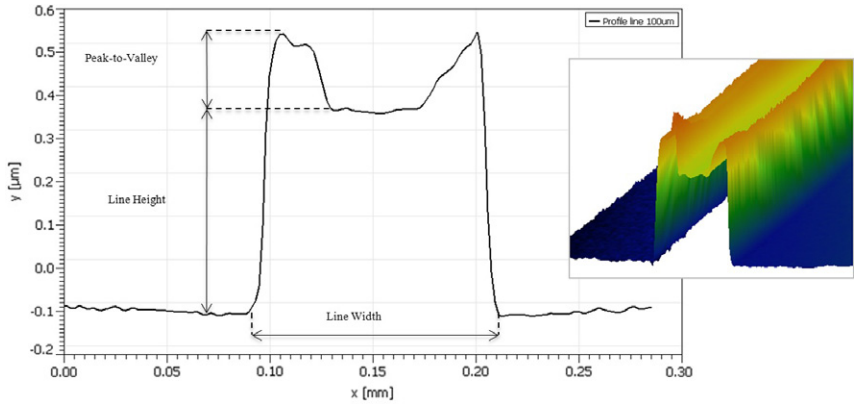


Figure 6. A 3D and sectional image of a sintered drop and bead parameters defined.

The pattern characterization structure was divided into a set of lines with different pixel lattices, as detailed in Figure 5. Pattern structures were printed using a range of substrate temperatures from 20 to 60°C and also using different printing directions.

The device characterization methodology defines some qualitative analyses labeled as: (1) line width; (2) line height; (3) peak-to-valley coffee ring versus height ratio; and (4) line uniformity, as shown in Figure 6. Even though line uniformity was assessed by means of varying drop space and delay, different drop lattices can produce non-homogeneous layers in terms of profile, due to the variations in the pixel density and therefore in the amount of ink deposited per unit area.

The purpose of the printing experiments was to measure the named parameters for different drop lattices, substrate temperatures and printing directions taking cross-sections near the ends of each line and several at the center. Our strategy is based on comparing and seeking the optimal parameters for each cross-section that leads to a squared profile.

Figure 7 shows the dependency of the line width for each pattern on the temperature substrate and printing orientation. Taking into account arbitrary lines, the expected printed line width was 200 µm, as also predicted in Eq. (2).

As depicted in Figure 8, and with the same tendency as for line width, a further increase in height is obtained owing to the merging of the deposited beads. Consequently, the height is maximized for the 100% solid line pattern (4) in both printing orientations at 60°C.

Patterns (4) and (5) fit the desired width fairly well. Obviously an increase in line width is observed when the pattern becomes denser, resulting in more material deposited

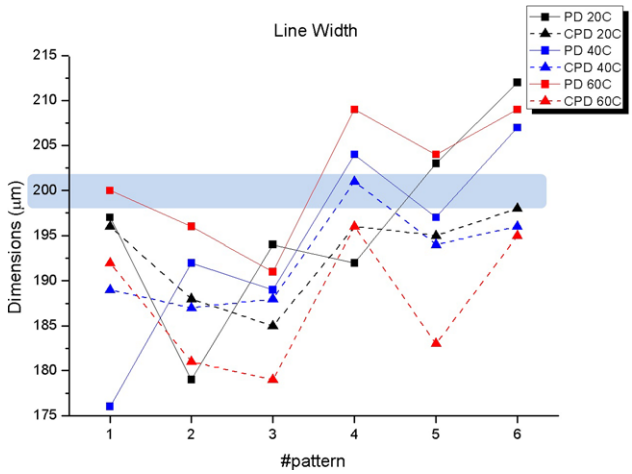


Figure 7. Measured line width.

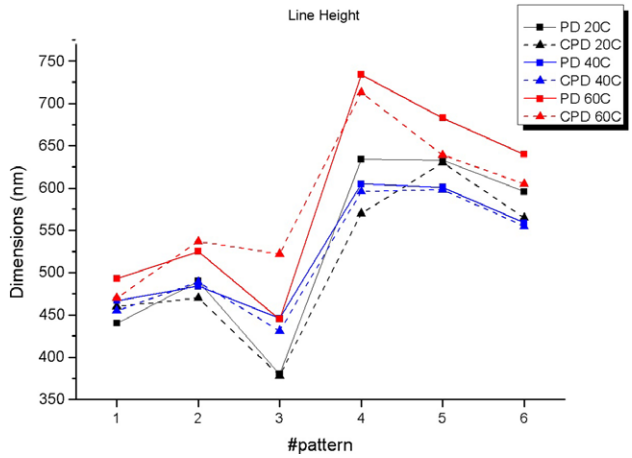


Figure 8. Measured line height.

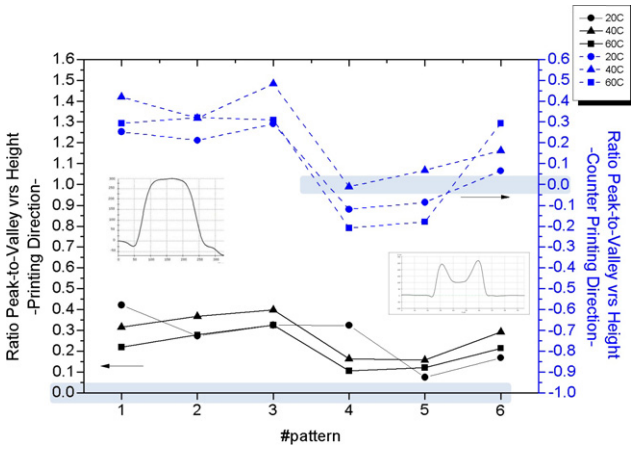


Figure 9. Measured peak-to-valley versus height ratio.

per unit area. However, the wider line appears for pattern (6) instead of for (4). In the same way, as the printing orientation influences the width, the printing direction lines present larger widths than the CPD lines due to different printing delays. Nevertheless, pattern (4) exhibits a closer result to the intended width in both printing orientations at 40°C.

Regarding the work by Soltman et al.[5] the coffee ring at the feature's edge occurs more strongly in a circular drop than in a straight line because of the greater ratio of edge length to center area in the drop. This effect leads to the characterization of both drops and lines. The morphology of the coffee ring on the patterns i.e. the peak-to-valley versus height ratio, is assessed considering substrate temperature and printing orientation as shown in Figure 9. Illustrated using blue boxes, a value of zero means close to a square profile without a coffee ring. Positive values indicate a convex profile and negative a concave line profile.

For higher and lower ratio values the influence of this effect compared with height is that it increases. Strikingly, as the substrate temperature increases, the coffee ring effect is not enhanced. Furthermore, the coffee ring arises in dense patterns such as (4) and (5) exclusively for CPD lines. There therefore exists a strong dependence on printing orientation. The printing direction patterns (4) and (5) at 40°C have close square profiles, as desired.

The line uniformity relating to the different drop lattices used was investigated by means of examining ridge width[14]—see Figure 10(a). The ridge width of scalloped pattern is defined as variation distance of individual rounded contact lines.[5]

Table I shows the ridge width depending on the pattern, printing orientation and substrate temperature. Data listed is an average of measurements. The value 0 indicates a straight line without a ridge (instances marked in gray).

The results show that the influence of the scalloped phenomenon is stronger for CPD lines than for PD lines. As the substrate temperature increases, instability is slightly enhanced for patterns (2) and (3), which have a 50% solid external line. For the patterns (1) and (6) formed at 40°C,

Table I. Ridge width (μm) measurement.

# pattern	20°C		40°C		60°C	
	CPD	PD	CPD	PD	CPD	PD
1	2.5	0.0	0.0	0.0	2.9	0.0
2	7.6	5.9	9.2	1.5	11.0	7.4
3	8.0	7.1	12.1	4.1	11.2	7.2
4	0.0	5.9	0.0	2.9	2.8	0.0
5	4.0	5.0	0.0	4.3	8.6	5.2
6	2.0	2.0	0.0	0.0	3.3	0.0

no ridge occurs. On initial reading of the results, at 40°C the ridge effect is not very pronounced.

Finally, considering: (1) line width, (2) line height, (3) peak-to-valley versus height ratio, and (4) line uniformity for different patterns and range of substrate temperatures, one can conclude that the best printing conditions are provided by pattern (4) at 40°C in PD orientation with a drop space of 20 μm and a jetting frequency of 5 kHz for the silver nanoparticle ink printed on PEN substrate.

EXTRACTION OF GEOMETRIC DESIGN RULES

Although geometric design rules can comprise a very large set of restrictions, they take into account two considerations: (1) the reproducible geometrical patterns by a specific process, and (2) the interaction between different layers.

In the field of Printed Electronics, it is important to control the feature fidelity of the patterning in order to exactly reproduce the circuit layout. By defining the optimal patterning, we can establish the design rules such as minimum width, spacing, notch etc. in order to achieve the minimum feature size which can be manufactured by the particular technology, as shown in Figure 11.

Compensation Techniques for the Improvement of Printed Structures: The Second Methodology Step

For inkjet-printed technology, the deposited pattern markedly deteriorates due to ink coalescence which leads to the need to use compensation techniques, as shown in Figure 12(a). Coalescence of separately deposited drops can occur on some substrates, and the drops can move or combine into larger drops creating an ink accumulation that can degrade the pattern fidelity.[15,16] The compensation techniques consist of modifying the shape pattern e.g. altering pixel density to redistribute the local density of ink in order to mitigate a lack of or accumulation of ink in some points of the structure in order to properly transfer the desired pattern. As a consequence of compensation techniques, the device mismatches are much less affected by the variability of the process, increasing yield and thus allowing for a more aggressive scaling down. An example of the concept is shown in Fig. 12(b).

The Pattern Shape Correction (PSC) is a compensation technique[2] based on Resolution Enhancement Techniques (RETs), particularly the Optical Proximity Correction (OPC)

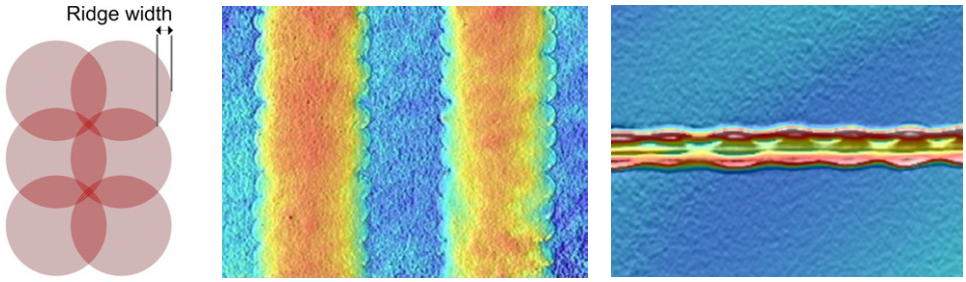


Figure 10. The ridge width effect of scalloped lines (200 μm width).

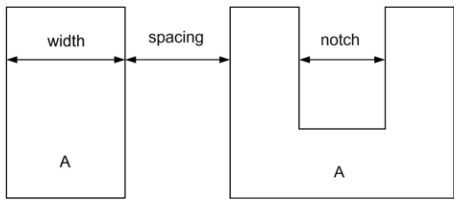


Figure 11. The definition of basic geometric design rules.

for correcting distortions of the photolithography process in silicon technology.

Outstanding improvement in the width notch was obtained by applying compensation techniques based on incorporating either additive or subtractive PSC serif-type features in order to produce the desired shape, as shown in Figure 13. Although the compensation technique can be applied to all dots in the patterns, efforts are being focused on the junction of perpendicular lines as being the main critical point. By eliminating pixels at the inner and upper left corners (as shown in Fig. 13c), a further resolution and rule for optimizing the minimum notch is achieved as illustrated in Fig. 13(d). Figure 14 shows additional examples of subtractive PSC serif-type features evaluated to improve minimum notch rule matching. The compensation feature shown in Fig. 13(c) was found to be the best for our printer/ink/substrate set.

Design Rules Characterization Structure: The Third Methodology Step

By carefully characterizing and understanding the conditions that lead to different printed line morphologies by means of pattern test structures, we will be able to establish the design rules for a particular ink. In this article, we present a set of pattern test structures useful for obtaining the physical limits of the manufacturing process resolution.

As previously discussed, the ink–substrate interaction affects the final line/area morphology. For this reason, and continuing with OTFT application, silver characterization structures need to be printed both in PEN substrate (since the gate is the first layer printed) and over the insulator layer (source and drain are bottom contacts). The left hand structures in Figure 15 have the characterization structures directly printed onto the substrate; and the right hand structures of Fig. 15 are on top of the previously deposited insulator layer. As can be observed in Figs. 3(b) and (c), the morphology of lines strongly varies depending on the preceding layer.

By means of the different pattern test structures included in the design of Fig. 15, by using optical and electrical instrumentation one can extract and characterize the minimum design rules for a given material and technology. The characterization structures included are discussed in the sections that follow.

The Minimum Width Rule

The structure consists of a set of lines for which line width progressively increases, while the spacing between remains constant (as shown in Figure 16a). The width of the first line set is 40 μm and increases up to 600 μm. Spacing between the lines needs to be sufficient to avoid merging.

By using this pattern, one can obtain the minimum rule width values such that the line is sufficiently straight, smooth and without stacked coins, scalloped or bulging behaviors, as in Fig. 16(b). This rule gives us, for example, the minimum width at which the drain and source electrodes must be printed to ensure a good morphology onto the insulator.

The Minimum Spacing Rule

The structure consists of a set of lines for which the space width between progressively increases, whilst line width remains constant.

This experiment needs to be repeated with additional line sets with different line widths, since minimum spacing also depends on the overflow caused by the line width.

By means of this pattern, one can obtain the minimum spacing rule such that every possible line width is sufficiently separated to avoid merging with neighboring lines. Figure 17(c) shows a displacement error that might lead to short circuit as shown in Fig. 17(d). This rule gives us, for example, the minimum spacing at which the drain and source electrodes of an OTFT must be printed onto the insulator to obtain the optimum channel length (L) for a given finger width.

The Minimum Notch Rule

The concept of the minimum notch rule concerns the structure of the U-shaped open loop. The structure consists of a set of U-shaped open loops for which line width and notch spacing progressively increase (Figure 18a). If the notch spacing is insufficient, ink coalescence will occur on

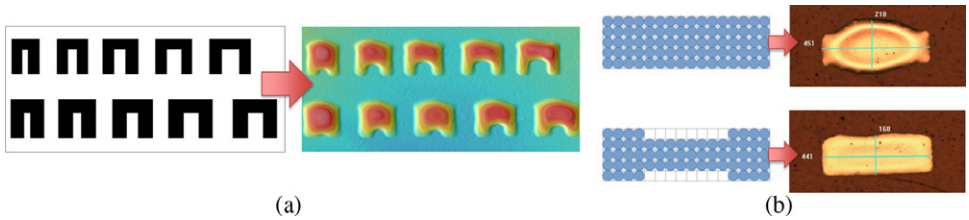


Figure 12. (a) A deteriorated printed pattern; and (b) the application of a compensation technique.

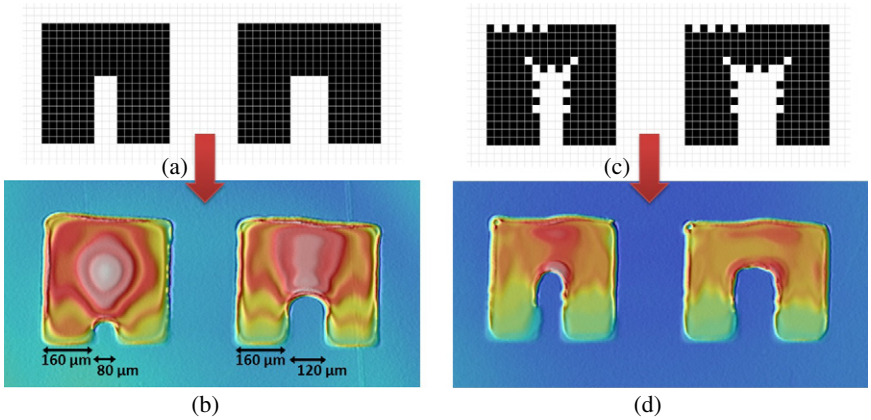


Figure 13. (a) Non-compensated notch pattern; (b) 3D image of the deposited non-compensated pattern; (c) PSC compensated notch pattern; and (d) 3D image for PSC compensated notch rule.

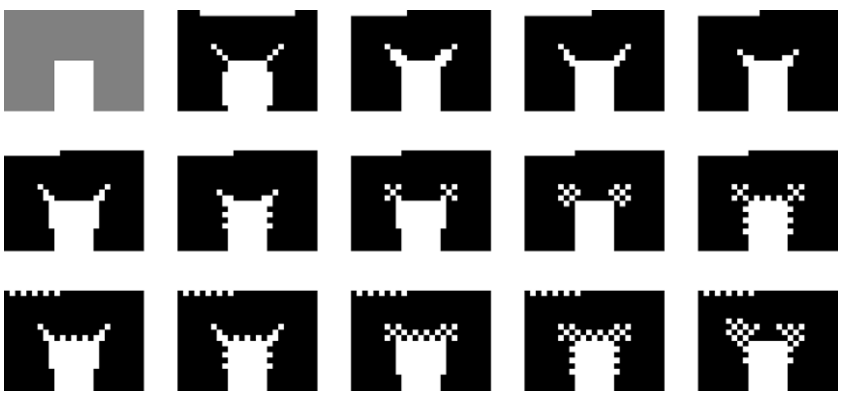


Figure 14. Different compensation strategies evaluated by taking out pixels locally.

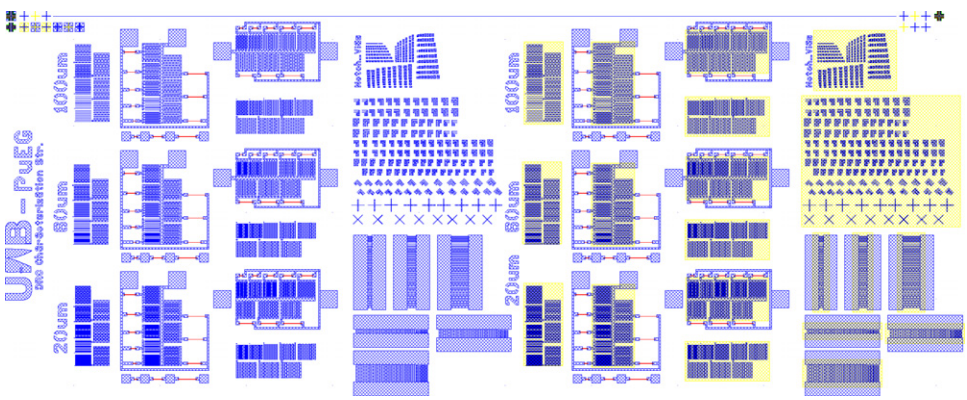
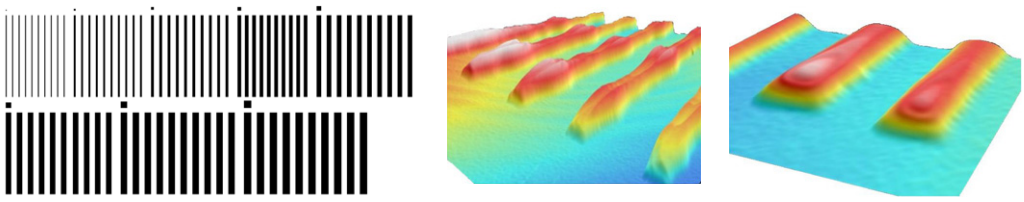
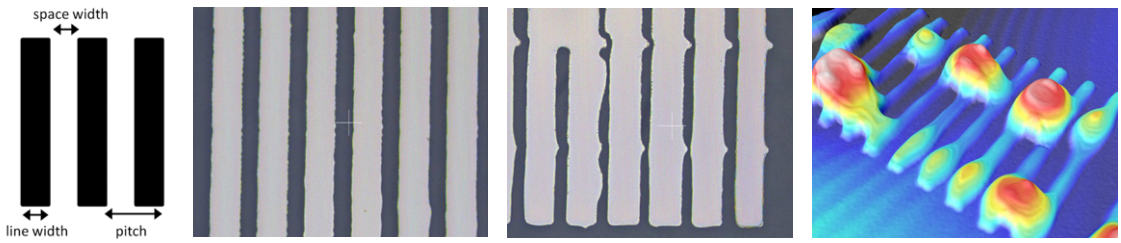


Figure 15. Layout of the test structure for characterizing the conductive ink on substrate and on insulator.



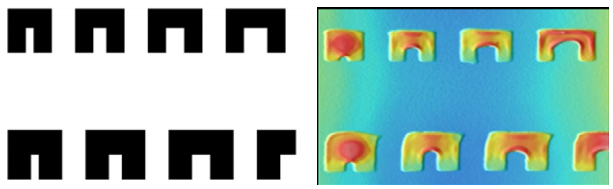
(a) (b) (c)

Figure 16. (a) Characterization pattern for minimum width rule extraction; (b) non-homogeneous line behavior; and (c) homogeneous line behavior.



(a) (b) (c) (d)

Figure 17. (a) Diagram of a line and space pattern; (b) correct spacing; (c) printer misalignment; and (d) electrical shorts, minimum spacing violated.



(a) (b)

Figure 18. (a) Test pattern; and (b) 3D image for minimum notch rule extraction.

top of the U-shaped open loop (Fig. 18b), modifying the width of the upper track and consequently the length and section of the U-track.

The goal of this rule is to extract the minimum notch spacing to avoid merging at the inner corners of bended lines. This is a typical rule used in e.g. snake resistors to reduce the area used by the resistive track.

The Corner Structures Rule

Integrated circuits require the patterning of corners. Convex corners occur, for example, at the junction of lines. Furthermore, an abrupt change in the direction of a line has resolution limits owing to corner rounding, among other undesired effects.[14] The purpose of this pattern is to assess the convex corners by means of the common corner structure, as shown in Figure 19(a), increasing the spacing between them whilst the line widths remain constant. Experimental results of this test structure will indicate how the actual contour varies at the printed edge depending on orientation, for example in Figs. 19(c) and (d).

By using this test structure, one can establish the optimal line width and spacing such that the ink is confined to a right angle line junction without merging (examples of such cases are shown in Figs. 19(c) and (d). This rule will be used to ensure that conductive tracks running in parallel will not be short-circuited when a change in orientation occurs.

The Junctions Rule

Microelectronic circuits also require the patterning of junctions. Junctions occur when a line is connected to another perpendicular line or a larger pattern (e.g. a connection pad). Furthermore, an abrupt change in the morphology can create strangled lines with profiles that are different than expected. Figure 20(a) shows the characterization structure and compensation technique used to improve the junction of source and drain fingers to their pads. The test structure consists of a set of T-shaped lines for which line width progressively increases, as shown in Fig. 20. The amount of ink entrained for the T-shaped structure depends on the ratio of the line width—the higher the ratio, the more the ink is entrained.

Automation of the Extraction of Design Rules

The characterization of pattern structures to extract Design Rules is tedious work due to the large quantity of structures that need to be characterized. Optical, confocal, interferometry or mechanical profilometry are powerful tools but are slow to use.

Alternatively, we can use structures that can be characterized by electrical measurements instead of by using optical metrology techniques. Figure 21 shows an interdigitated array of electrodes (with a constant spacing between them and for which finger width progressively increases) that will allow for the characterization of the minimum spacing rule for a given line width. If we repeat the structures whilst varying the line spacing, we will obtain the minimum spacing rule for every line width permitted by our particular technology.

As structure characterization is established by an interdigitated array of electrodes where finger width increases, if

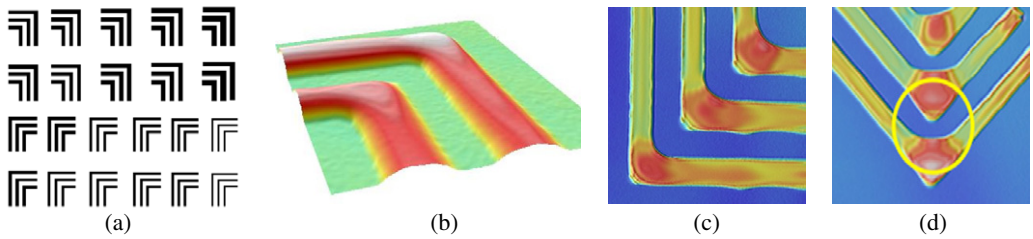


Figure 19. (a) Test pattern; (b) 3D image of corner patterns; (c) corner pattern; and (d) corner pattern rotated 45°.

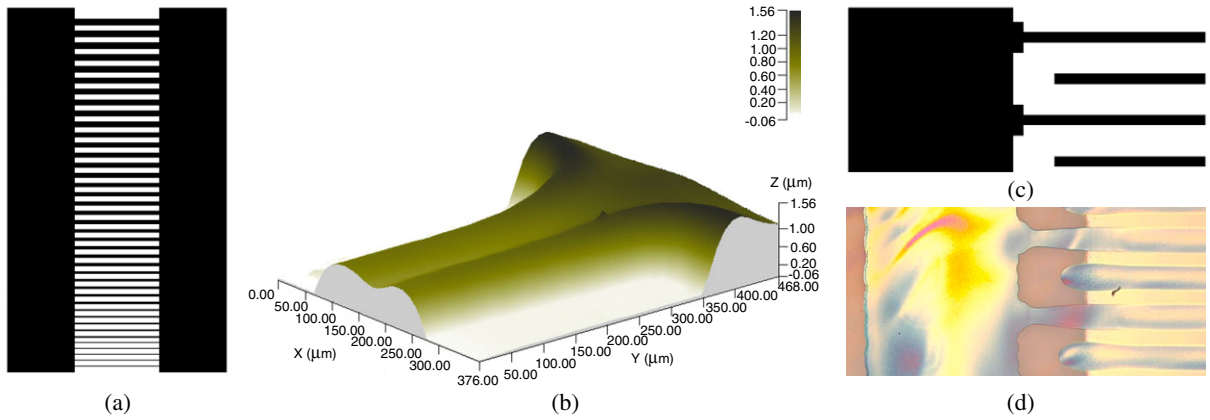


Figure 20. (a) Test pattern for junction characterization; (b) 3D image of junction; (c) layout of 40 µm width source and drain electrodes using additive PSC serif-type feature to improve junction; (d) image of printed layout with strangled lines although the compensation is applied.

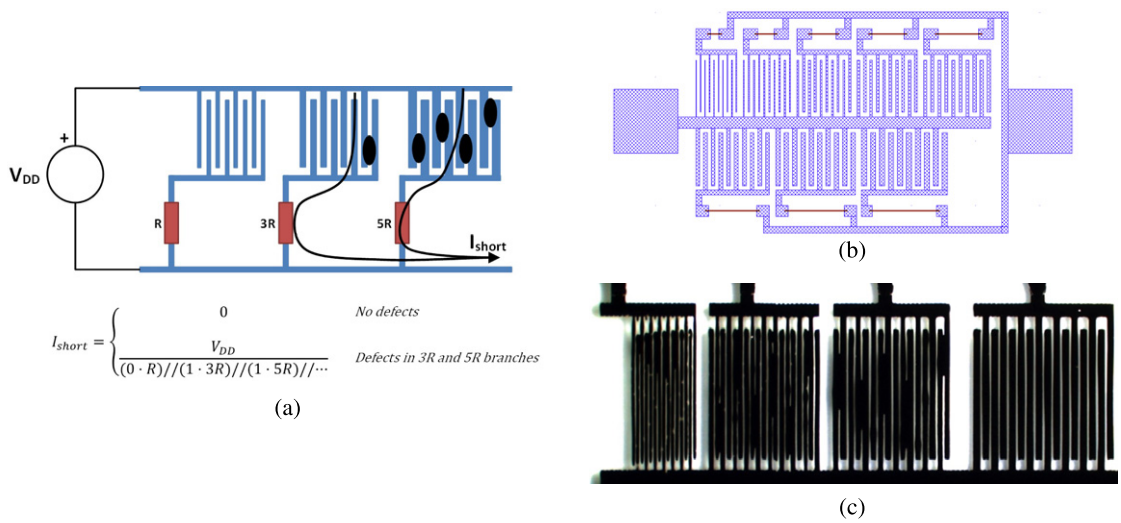


Figure 21. (a) Electrical circuit of characterization pattern; (b) layout of characterization pattern; (c) printed characterization structure over PVP with shorts at smaller spacings.

the fingers are not sufficiently separated to avoid merging with neighboring lines, a short-circuit current will flow. In order to identify the set of fingers (related to finger width) which are insufficiently separated, a circuit using a scaled resistor was used to detect the short-circuit position through measurement of the current. With only a two-point current measurement, a large quantity of finger sets can be analyzed though the decomposition of the individual resistors related to each group of interdigitated finger arrays.

In the characterization structure shown in Fig. 15, we have characterized groups of interdigitated arrays of electrodes (each one containing at least 10 fingers), with widths ranging from 40 to 200 µm and line spacings of 20, 60 and 100 µm, directly printed on PEN and on top of an insulator layer. Different structures were included to characterize lines printed in both the printing and counter printing directions. The electrical characterization of these structures gave us a preliminary minimum spacing rule,

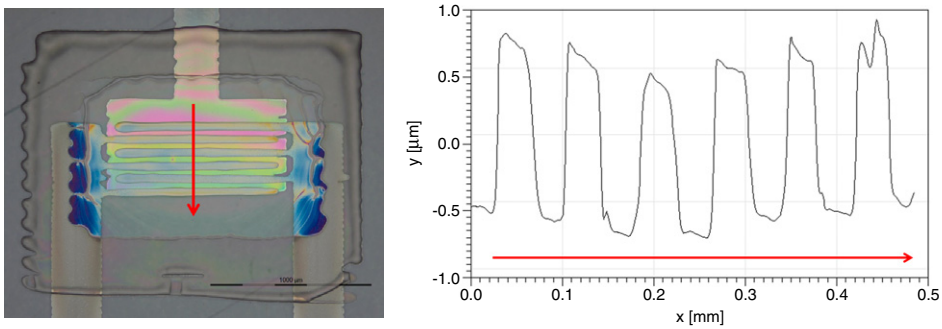


Figure 22. Left: all-inkjet-printed transistor; Right: profile of drain and source interdigitated electrodes. Red arrow shows the direction of measurement.

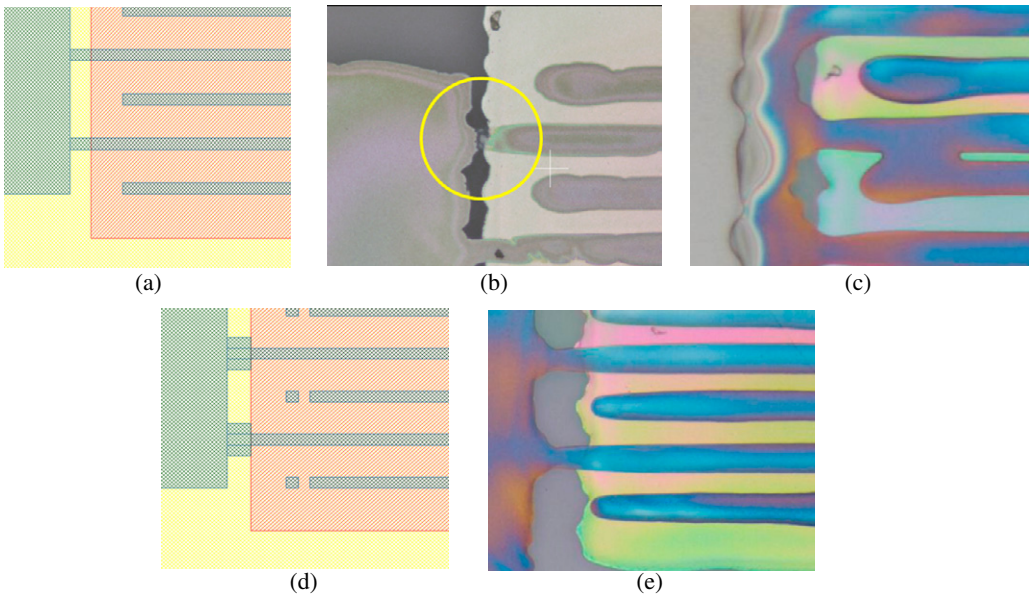


Figure 23. (a) Layout of source and drain electrodes without compensations; (b) and (c) different effects occurring with non-compensated electrodes and junctions; (d) compensated layout; and (e) compensated electrodes.

Table II. Minimum spacing rule.

Finger spacing	20 µm		60 µm		100 µm	
Minimum line width allowed	PD	CPD	PD	CPD	PD	CPD
Ag over substrate	no	no	140 µm	180 µm	all	all
Ag over insulator	100 µm	80 µm	40 µm	40 µm	all	all

as summarized in Table II. Measurements were visually corroborated by means of optical microscopy and other techniques.

RESULTS OF METHODOLOGY APPLICATION ON OTFT DEVICES

Figure 22 shows the applied methodology for the deposition of the drain and source electrodes on an all-inkjet-printed OTFT. Following on from the results outlined earlier, the electrodes and channel widths have been optimized as shown in Fig. 22 Right. The profile shows that the electrodes are regular, without a pronounced coffee ring effect and with sufficient separation in order to obtain a high yield.

Figures 23(b) and (c) shows different effects that occurred with non-compensated electrodes and junctions such as short circuits between drain and source electrodes, strangled junctions in some cases producing open circuits, and a bulging effect at the end of the electrodes.

In order to avoid these undesired effects, we applied the compensation techniques methodology by respectively extracting and adding drops to electrodes and junctions, thereby improving the morphology of drain and source electrodes and increasing the yield of the fabricated devices.

SUMMARY AND CONCLUSIONS

We have discussed the extraction and characterization of geometric design rules and the application of compensation techniques for the inkjet manufacturing of reliable and precise designs based on the knowledge inherited from the well-developed silicon microelectronics technology.

Our work is focused on the enhancement of the OTFT structure from a morphological point of view in order to improve device performance and process reproducibility,

and to increase yield, thus allowing for a more aggressive scaling down. As discussed above, line morphology is a key factor. Our contribution to the field is to propose a clear methodology for individually characterizing the materials printed onto different substrates/layers in order to obtain optimal morphologies, for example, for source and drain electrodes. In addition to the inkjet printing parameters that are widely used, such as temperature, jetting frequency or DS, we have employed the modification of the drop lattice as a novel parameter. Before the establishment of the design rules, a compensation techniques methodology has been applied. Moreover, a set of compensation structures has been provided in order to obtain minimum dimensions and improve shapes, such as junctions and corners that markedly deteriorated due to ink coalescence. Finally, we have introduced an automated solution for the extraction of design rules by using electrical measurements.

ACKNOWLEDGMENTS

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