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Dielectric Patterning Using Aerosol Jet Printing

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Abstract. *A method for spatially selective etching of dielectric layers using an aerosol jet printer is described. The method, referred to as direct etching, was first implemented using inkjet printing. This article reports on the adaption of the method to operate on an 'Optomec' aerosol jet printer in order to increase patterning resolution and processing throughput, as required for commercial photovoltaic applications. It is demonstrated that the etching process can be tailored to different applications by varying the processing parameters, such as the gas flow rates, platen movement speed and number of printing passes. The results presented in this article show that grooves as narrow as* 20 μm *can be etched in dielectric layers that are commonly used for passivation of commercially produced silicon solar cells. Accurate alignment enabled by the 'Optomec' aerosol jet printer allowed etched patterns to be formed in pre-patterned surfaces, a property that may find application in a number of selective-emitter solar cell designs which currently use aligned screen printing for metallization. In addition, a method of etching point openings for metal contacts for enhanced rear surface passivation is presented and discussed.* © *2012 Society for Imaging Science and Technology.*
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INTRODUCTION

Dielectric materials are crucial to many solar cell designs, where they are often used as insulating and passivation layers. The ability to pattern dielectrics accurately, at high resolution and with a high processing throughput can greatly benefit the development of new commercially viable solar cell designs that are more efficient than their predecessors. This is particularly important for newer generations of solar cell designs requiring well passivated rear surfaces and localized metal contacts. The photolithographic processes used widely in microelectronics for dielectric patterning are unsuitable for photovoltaic manufacturing due to cost and complexity, with screen printing and laser-based patterning being preferred techniques.[1] The former, however, provides poor resolution, while the latter often creates damage to the underlying silicon[1] which can limit performance. Ideally, as an industrial process, such dielectric patterning methods would: (i) have a high processing throughput; (ii) be low cost in terms of equipment, consumables, maintenance and waste disposal; (iii) allow for significant automation and be easily integrated into a manufacturing line; (iv) provide adequate patterning resolution; (v) avoid causing any damage to the underlying semiconductor material; and (v) be reliable and robust. Direct etching with an aerosol jet printer (AJP), also referred to as aerosol jet etching (AJE), may offer an alternative patterning method that can balance the trade-offs between the robustness and fast processing rates of industrial printing methods, such as screen printing, and the high resolution of photolithographic and laser-based methods.

More specific to solar cell applications, the accurate patterning and feature realignment made possible with AJE allows for the implementation of selectively doped metal contacts, which can significantly improve overall device performance by enabling a large fraction of the illuminated surface to be lightly doped, thus improving current generation. The formation of etched holes for rear contacting is another process where accurate and discrete patterning techniques like AJE can be utilized to improve the design and performance of solar cell devices. This article reports on optimization of the AJE process for potential solar cell applications.

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DIRECT ETCHING

Process description

Direct etching allows for spatially selective etching of dielectrics.[2] A hydrofluoric acid (HF) mixture is generated on the substrate by combining an acidic component with a fluoride component. In theory, the hydrogen and fluoride ions can combine in solution to form HF. Direct etching involves the following steps (see Figure 1):

1. An acidic, water-soluble polymer (i.e., polyacrylic acid (PAA)) is spin-coated onto the surface of the dielectric.
2. A fluoride solution is deposited onto the polymer with an AJP in a specified pattern. Hydrofluoric acid then forms on localized areas of the wafer (i.e., areas where the solution mixes with the PAA) and is able to etch the underlying dielectric.
3. Samples are then rinsed in de-ionized water to remove etch products and residual PAA.

Direct etching has the potential to be low cost and less damaging to the environment than other patterning methods which involve immersion etching in HF, largely due to the minute volumes of chemicals required for the process. It also has the added advantage of eliminating the need to apply mechanical force to the substrate. Initial trials of direct etching with an inkjet printer demonstrated etched line widths as narrow as 40 μm and laboratory cell efficiencies (on commercial-grade silicon wafers) of up to 17%.[3]

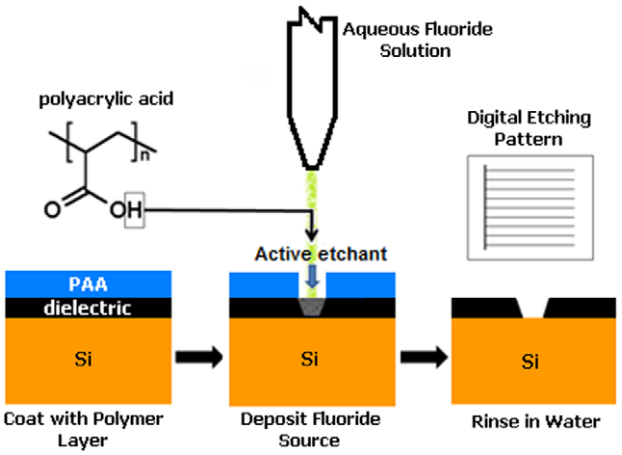

Figure 1. A schematic of the steps involved in direct etching.[2]

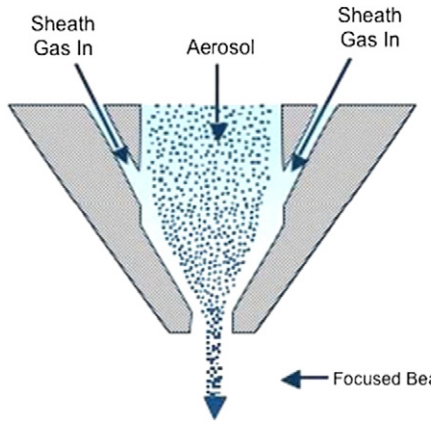

Figure 2. A schematic of atomized material exiting the deposition head opening. The sheath gas surrounds the material and prevents it from contacting the inner surfaces of the tip (sourced from Optomec Inc.).

Aerosol jet printing

Early experiments suggested that the AJP may enable narrower etched line widths than achieved to date by the inkjet implementation of direct etching.[4] The AJP works by, firstly, atomizing the desired print material to produce a fine mist. A nitrogen carrier gas then transports this mist to the print head, where a second annular stream of nitrogen gas is introduced to focus the mist into a collimated beam for precise deposition (see Figure 2). The AJP is capable of: (i) printing feature sizes as narrow as 10 μm; (ii) printing materials with viscosities ranging from 1–1000 cP; (iii) depositing material on non-planar surfaces; and (iv) processing at a maximum speed of 300 mm/s.[5]

In addition to narrower etched lines, it is possible that the AJP may enable higher processing throughputs than achieved by inkjet printing. However, realistically, processing throughputs would need to be significantly increased to enable the patterning of full-size commercial solar cells within a few seconds.

A further advantage is that the AJP can operate in a large range of ambient temperature and humidity conditions. Optomec specify an operating temperature range of 10–40°C and a relative humidity range of 30–90%.[5] This capability suggests that the printer could be a robust manufacturing tool. The ambient temperature range for AJE is discussed later in this article.

EXPERIMENTAL

Silicon samples were coated with various dielectric layers, which included thermally grown silicon dioxide (SiO_2), silicon nitride (SiN_x), silicon oxynitride ($SiON_x$) and aluminum oxide (Al_2O_3) deposited using plasma-enhanced chemical vapor deposition (PECVD). Each substrate was square with one rounded edge, with approximately 4 cm long sides. With the exception of the samples described in the "PAA thickness" experiments, all samples were then spin-coated with 20% w/v PAA (diluted from a 25% stock solution obtained from Polysciences, Inc.) to produce a dried polymer layer ~1.8 μm thick. A 10% w/v ammonium fluoride (NH_4F) solution in de-ionized water (prepared from a 40% w/v stock solution obtained from J. T. Baker) was then deposited onto the sample using the AJP.

An ultrasonic atomizer was used for all AJE experiments described in this article. The ultrasonic atomizer chiller temperature and voltage were kept at 25°C and 45 V, respectively. There was a thick white mist visible in the ultrasonic atomizer vial for all depositions conducted with the AJP. After rinsing, an optical microscope was used to examine the clarity of the etched lines and measure feature widths.

RESULTS AND DISCUSSION

Printing speed

The speed at which the stage moves during deposition plays a large part in determining the amount of aerosol deposited on the substrate, with faster printing speeds resulting in less material deposition per unit area. Experiments were designed to determine the interdependences between the printing speed and number of layers printed, in order to observe the effect on the resulting etched line widths and clarity. When printing patterns are repeated the generated solution can etch deeper and the line width increases with the number of repetitions (i.e., printed layers).[2]

Figures 3 and 4 illustrate how the resulting etched line widths varied with printing speed and number of printed layers through SiO_2 and SiN_x layers, respectively. Figure 5 shows optical microscope images of example lines etched in a 75 nm thick PECVD SiN_x layer deposited on a textured silicon wafer. The samples for Figs. 3 and 5 were processed using: (i) a 100 μm tip; (ii) an atomizer flow rate (AFR) of 15 sccm; (iii) a sheath gas flow rate (SFR) of 10 sccm; and (iv) a platen temperature of 50°C. The data generated for Fig. 4 used an AFR of 12 sccm and an SFR of 15 sccm; all other parameters were kept equivalent to those used for the experiments that yielded the results depicted in Figs. 3 and 5.

In general, line widths increase with slower printing speeds and for increasing numbers of layers. Consequently,

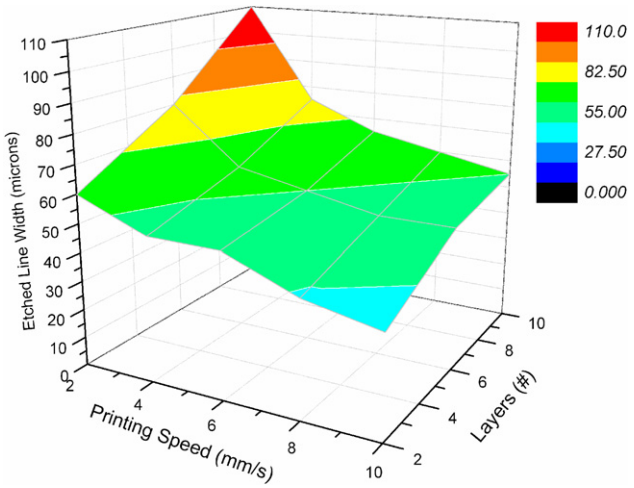

Figure 3. The etched line width (*z*-axis) varies as the printing speed (*x*-axis) and number of printing passes (*y*-axis) are varied. The sample was a textured silicon wafer with a 120 nm thick thermally grown SiO_2 layer.

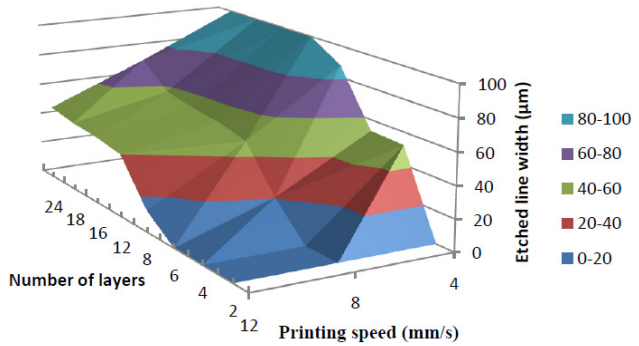

Figure 4. The etched line width (*z*-axis) varies as the number of printing passes (*x*-axis) and printing speed (*y*-axis) are varied. This set of results was for a textured silicon wafer coated with a *75* nm thick PECVD SiN_x layer that was spike-fired at a peak temperature of *850*°C after deposition.

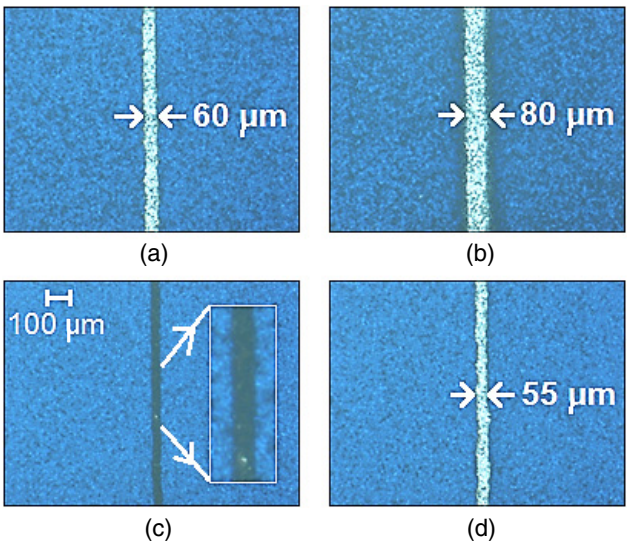

Figure 5. Optical microscope images illustrating how the line width and etching vary with printing speed and number of layers printed. The processing parameters were: (a) 2 layers at 2 mm/s; (b) 10 layers at 2 mm/s; (c) 2 layers at 10 mm/s; and (d) 10 layers at 10 mm/s. All other experimental parameters were kept constant. Incomplete etching resulted with 2 layers at a speed of 10 mm/s. This sample was a textured silicon wafer with a *75* nm thick PECVD SiN_x layer, which was spike-fired at a peak temperature of *850*°C after deposition.

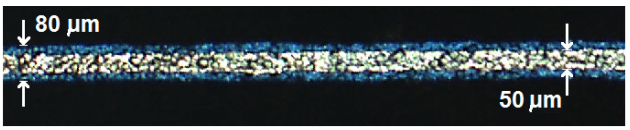

Figure 6. The thin, bright line in the middle (~ *50* µm wide) was etched through a *75* nm SiN_x layer and was realigned to a previously patterned ~ *80* µm wide planarized groove. The groove was printed at a speed of 4 mm/s with three layers and the thinner etched line was printed at a speed of 16 mm/s with four layers. All other processing parameters were kept constant.

the printing conditions can be selected to suit individual applications which have different etching resolution requirements (e.g., where different etched line widths are required). One application where this functionality is useful is where the etched lines are required to be aligned to previously etched or patterned regions. By varying the processing speed and layers, a thinner etched feature may be realigned to be positioned within a wider feature, as shown in Figure 6.

An example that is more specific to solar cell applications is the fabrication of selective-emitter structures. If the wider planarized groove is heavily doped prior to etching the thin middle line then subsequent metallization of these exposed silicon regions will result in a heavily doped metal–silicon interface, which leaves the majority of the remaining front surface lightly doped and passivated by the dielectric.

Platen temperature

The temperature of the platen largely determines the temperature of the etching solution generated on the substrate and hence the rate of the etching reaction. Figure 7 illustrates how the platen temperature can be controlled in order to minimize etched line widths (all other experimental parameters were kept constant). Figure 8 shows optical microscope images of etched lines from the same set of experiments.

Platen temperatures in the range of 50–60°C have shown consistent results and clean etching. This value is slightly higher than the optimal value of 45°C quoted for direct etching experiments performed on an inkjet printer.[2] Since increasing the platen temperature leads to faster evaporation of the aqueous NH_4F solution, the effect of increasing the temperature is similar to that of reducing the AFR, or in other words the amount of liquid deposited onto the sample. This effect will be discussed in more detail in the subsection "Gas flow rates".

There are, however, side-effects of significantly increasing the platen temperature, as the deposited mist tends to dry more prior to contacting the substrate. For platen temperatures higher than 60°C there was an increasing tendency for deposition tips to clog whilst printing.

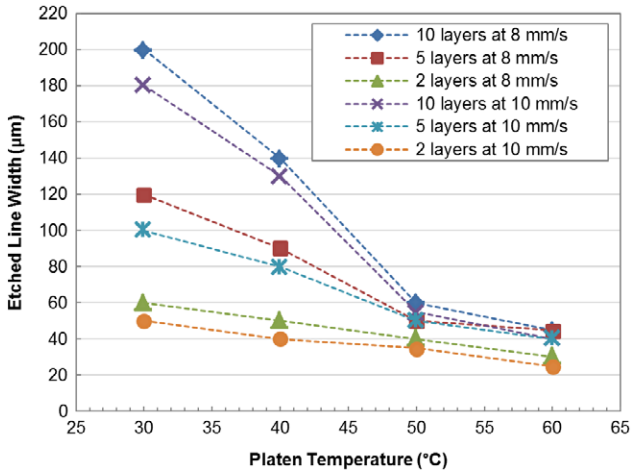

Figure 7. Etched line width plotted as a function of platen temperature for a 120 nm thick SiO_2 layer thermally grown on a textured silicon wafer. For all experiments the tip size, AFR and SFR were maintained at *100* µm, 15 sccm and 10 sccm, respectively.

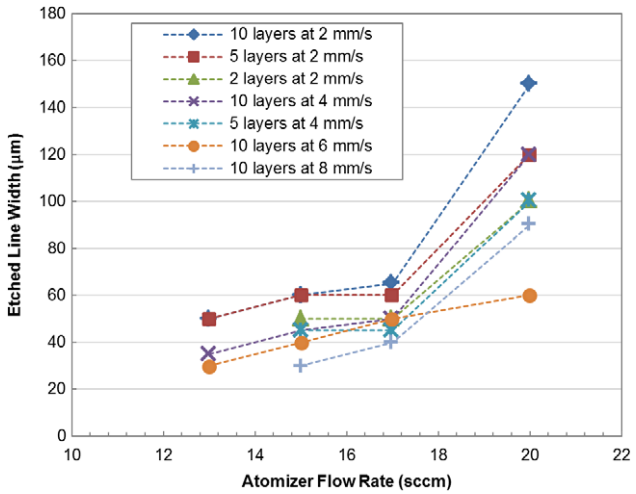

Figure 9. Etched line width plotted as a function of AFR for *75* nm thick, *850*°C spike-fired SiN_x layers deposited onto a textured silicon wafer. Some values are not shown for AFRs of less than 13 sccm because incomplete etching resulted.

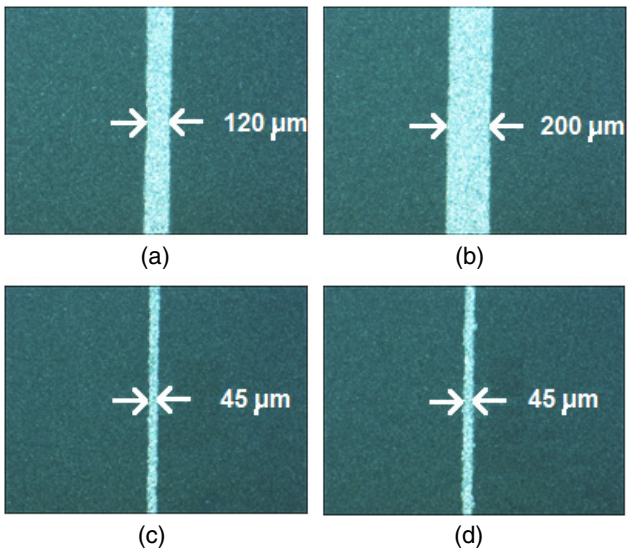

Figure 8. Optical microscope images showing how the etched line width varied as a function of platen temperature for a 120 nm thick SiO_2 layer thermally grown on a textured silicon wafer. The processing parameters were: (a) 5 layers at *30*°C; (b) 10 layers at *30*°C; (c) 5 layers at *60*°C; and (d) 10 layers at *60*°C. The printing speed was 8mm/s and all other experimental parameters were kept equivalent.

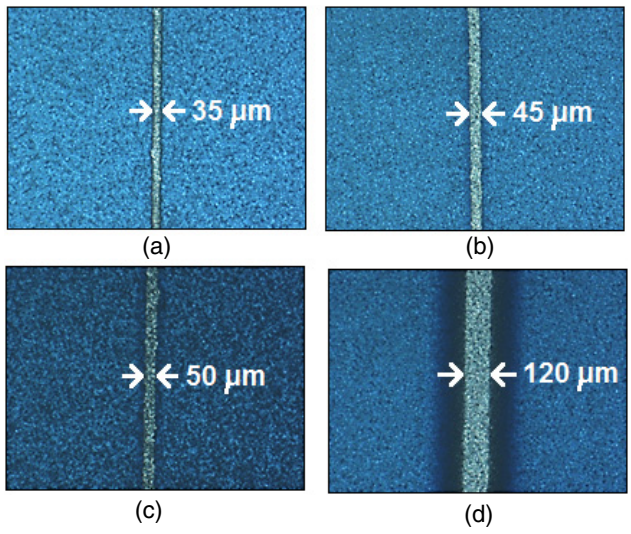

Figure 10. Optical microscope images showing lines which were etched using different AFR values for a *75* nm thick, *850*°C spike-fired SiN_x layer deposited onto a textured silicon wafer. All four samples were processed with the same experimental parameters, with the exception of the AFR which was: (a) 13 sccm; (b) 15 sccm; (c) *17* sccm; and (d) 20 sccm.

Gas flow rates

The AFR partially determines the resulting volume of material deposited onto the substrate. By varying the AFR, the line widths and clarity of etching can be controlled. However, if the AFR is too low then an insufficient amount of aqueous NH_4F solution will be deposited on the surface and features may not be completely etched through the dielectric, as shown in Fig. 5(c). Figure 9 summarizes the effect of varying the AFR on the width of lines etched in a 75 nm thick SiN_x layer deposited onto a textured silicon wafer. Optical microscope images of some of the etched lines are shown in Figure 10. A 100 µm tip was used and the platen temperature and SFR were maintained at 50°C and 10 sccm, respectively, for all experiments.

Etched line widths increase with larger AFRs most likely due to the spreading of the dissolved polymer region when more fluoride aerosol is deposited. For very low AFRs (i.e., below the threshold of etching through the dielectric) it was observed that the deposited material appeared to be solid as soon as it contacted the sample (as viewed on the process camera of the AJP). The dimensions of the solid deposit could be made very narrow; however, adequate etching did not occur under these conditions, most likely because there was insufficient water for the etching reaction to occur effectively.

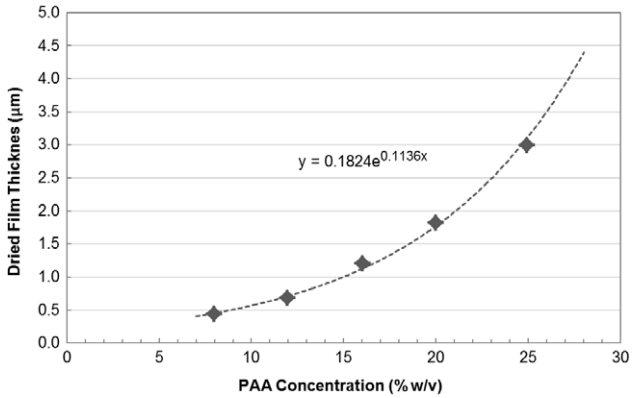

Figure 11. Dried PAA film thickness as a function of the weight percentage (% w/v) of the spin-coated PAA solution. The data points closely follow the fitted exponential function, although the fitted model makes less sense, physically, at PAA concentrations close to 0% w/v. The spin speed and time were kept at 7,000 rpm and 30 s, respectively, for all experiments.

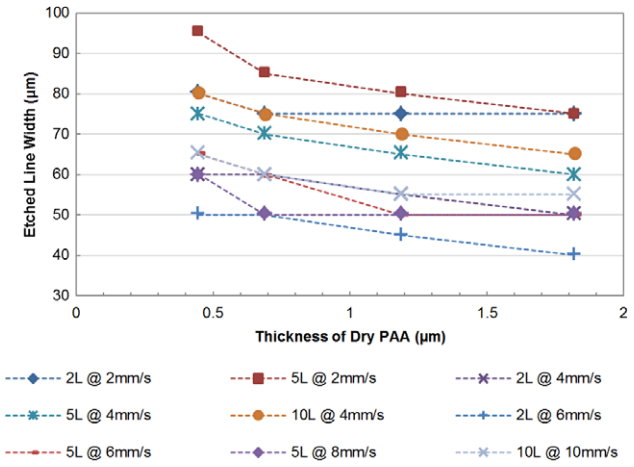

Figure 12. Etched line widths as a function of dried PAA layer thickness.

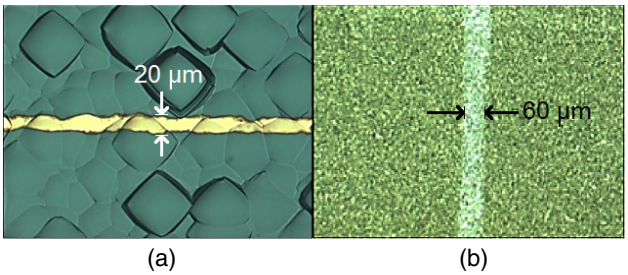

Figure 13. (a) A groove etched through a 75 nm thick SiN_x layer on a planar silicon surface with an average line width of ~ 20 µm. (b) A groove etched through a 75 nm thick PECVD aluminum oxide layer on a textured surface with an average line width of ~ 60 µm. Both samples were etched using a 150 µm tip, SFR of 25 sccm, AFR of 15 sccm and platen temperature of 50°C.

PAA thickness

The PAA layer performs two important tasks during direct etching. First, it acts as a source of hydrogen ions, necessary for producing the generated HF-etchant, and secondly it acts as an absorbent layer that contains the liquid etchant and restricts it from spreading laterally from the point of deposition. Experiments were designed to examine the effect that varying the thickness of the PAA layer had on etched line widths and clarity.

The thickness of dried PAA layers can be controlled by varying the concentration of the PAA solution that is spin-coated onto the sample surface. Figure 11 shows how the PAA layer thickness varied between 0.5 and 3 µm by simply changing the PAA concentration from 8 to 25% w/v.

Test patterns were then aerosol jet etched in a 120 nm thick SiO_2 layer thermally grown on textured p-type silicon wafers with PAA layers of different thickness. The printing speed was varied from 2 to 10 mm/s and the number of printed layers was varied from 2 to 10. The etched line widths and clarity were monitored under an optical microscope. Figure 12 shows that the width of the etched lines reduced as the PAA layer thickness increased for most AJE processing conditions trialled.

These results demonstrate that the AJE process is tolerant to variation in the dried PAA thickness. Complete etching of the underlying dielectric layer occurred for PAA layers from 0.5 to 2 µm thick, using identical AJP parameters. There was, however, a significant amount of variation in the etched line thickness for different PAA layer thicknesses. In general, thinner dried PAA layers tend to result in wider etched lines.

Thicker PAA layers tend to result in thinner etched lines as well; however, there is a limit to how thick the layer can be before it inhibits etching of the underlying dielectric. Thicker PAA layers require a larger volume of NH_4F solution to completely dissolve the water-soluble polymer and expose the underlying dielectric. For sets of AJE printing parameters with faster speeds and fewer layers, there may be insufficient liquid material available to allow for effective dielectric etching.

Alternative dielectrics

In addition to SiO_2 and SiN_x layers, recent trials have also demonstrated that $SiON_x$ and Al_2O_3 layers (both deposited using PECVD) can also be patterned with direct etching. The images in Figure 13 are examples of lines etched through these two materials. Lines as narrow as 20 µm have been etched through a 75 nm $SiON_x$ layer. Silicon oxynitride layers have demonstrated excellent passivation properties[6] and may well be a much more commonly used anti-reflection coating or rear dielectric layer in the near future. Aluminum oxides are also materials of particular interest in the PV community because of their ability to passivate p-type surfaces,[7] which has near-term application to rear surface passivation of next-generation, p-type commercial solar cells.

Ambient temperature

Experiments were designed to examine the performance of direct etching in varying ambient temperatures, the results of which are shown in Figure 14. Samples coated with 75 nm thick $SiON_x$ layers were prepared and etched in varying

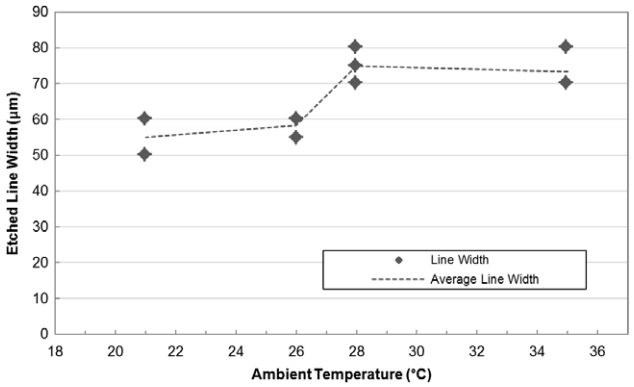

Figure 14. Etched line width for 75 nm thick SiN_x layers deposited on planar silicon wafers as a function of ambient temperature. All samples were etched using a 150 μm tip at a printing speed of 8 mm/s for 10 layers. The platen temperature, AFR and SFR were 50°C, 15 sccm and 25 sccm, respectively.

ambient temperatures, whilst keeping all other printing parameters equivalent. A digital thermometer placed inside the AJP enclosure was used to measure the ambient temperature of the process for each printing run.

There appears to be some variation in the width of the etched lines at different temperatures; however, these results demonstrate that AJE can be performed in a wide range of ambient temperatures, up to at least 35°C.

Aerosol jet etched point contacts

Rear surface designs for commercially produced silicon solar cells have remained largely the same since the screen-printed Spectrolab design was released in the 1970s.[8] The Spectrolab rear contact scheme generated a back surface field (BSF) over the entire rear surface, created by alloying the rear silicon with screen-printed aluminum (Al). The BSF is beneficial to overall cell operation because the built-in electric field repels minority carriers away from the rear surface of the cell and reduces their chance of recombination. However, there are significant recombination sites available at metal–semiconductor interfaces and the fact that the entire rear silicon surface is alloyed with aluminum means that the rear surface of the Spectrolab design acts as a very effective recombination region. Improvements in rear surface designs of solar cells provide the opportunity to increase average screen-printed cell efficiencies from 17–18% to around 20%.[1,9]

Previously fabricated high-efficiency solar cell devices, such as the passivated emitter and rear local-diffused (PERL) cell,[10] have demonstrated that significant gains in solar cell efficiency can be achieved by implementing rear point-contacting schemes of solar cell devices. Point-contact designs, compared to full-rear BSF cells, can substantially reduce the probability of minority carrier recombination at the rear surface of the device by reducing the total metal–semiconductor interface surface area. In general, the optimal configuration for point-contact designs requires small-area contacts that are spaced close together.[10,11]

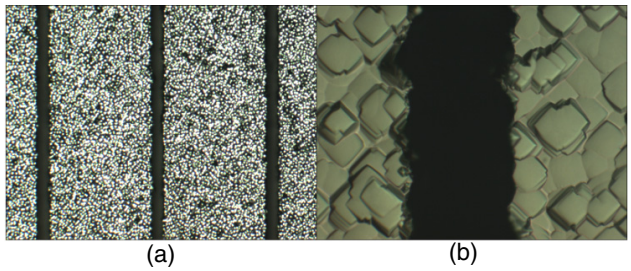

Figure 15. A silicon wafer mask with line openings scribed through it. Image (a) was viewed at a magnification of 50×; image (b) was viewed at a magnification of 500×. The line openings are, on average, 40 μm wide.

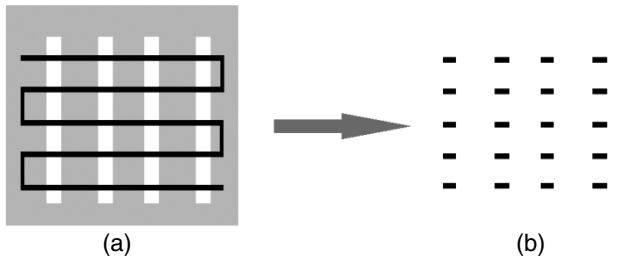

Figure 16. The use of a mask allows for a regular array of material deposited by an AJP. In (a), the continuous flow of material from the AJP (shown in black) is printed perpendicularly to the line openings of the silicon mask (shown in light gray). Part (b) illustrates the periodic, 'point-contact' pattern that is consequently printed onto the underlying sample. The relative dimensions of the openings and printed material are not to scale.

Photolithography has been demonstrated as a method with the ability to form very small contact sizes with well-controlled, narrow spacing;[12,13] however, as previously stated, it is considered too expensive and complex for commercial solar cell production. Aerosol jet deposition is a continuous-flow process and although there is a small mechanical arm to intermittently impede deposition, it is not designed for the high frequency on-and-off motion required for the etching of hole-openings. Therefore a major challenge for creating point openings in a dielectric layer with aerosol jet etching is in controlling the areas where the HF-etchant is generated.

One simple way of generating point contacts with aerosol jet etching is to use a mask to control where material is deposited. For initial trials, silicon wafer masks were made with line openings approximately 40 μm wide and spaced 500 μm apart. Microscope images of these masks are given in Figure 15. The masks were made by laser-scribing silicon wafers with a 1064 nm wavelength laser. The masks were then put through a sodium hydroxide (NaOH) etch to remove melt damage, smooth the edges in the scribed regions and allow for fully opened scribed lines.

In order to print a point-contact pattern, the NH_4F solution was printed perpendicular to the line openings in the mask (see Figure 16) so that the HF-etchant solution was only generated in areas that the mask did not cover. This resulted in an array of regularly spaced, rectangular-shaped deposits.

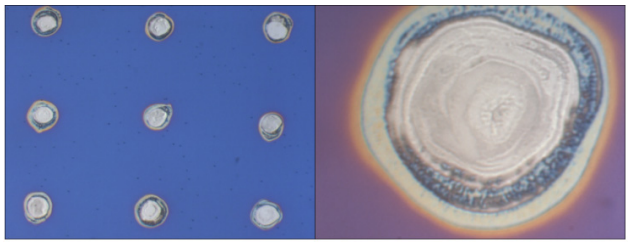

Figure 17. Holes formed with the use of a silicon mask in combination with AJE. Image (a) was viewed at a magnification of 50× and image (b) was viewed at a magnification of 500×.

Initial trials using this method resulted in holes with an average width of 60 μm, etched through SiO_2 layers 300 nm thick. Figure 17 displays microscope images of these etched holes. These samples were printed using a 150 μm tip and the following AJP parameters: (i) an AFR of 22 sccm; (ii) an SFR of 70 sccm; (iii) an ultrasonic atomizer voltage of 45 V; (iv) a platen temperature of 45°C; (v) a chiller temperature of 20°C; (vi) 20 printed layers; and (vii) a print speed of 10 mm/s. A PAA layer ~1.8 μm thick was deposited onto the samples, using 20% w/v PAA solution spin-coated at 7000 rpm for 30 s.

The resulting etched holes were circular, even if the NH_4F deposition was rectangular. Despite the demonstration of etched holes, it became evident that there were significant limitations to this method. First, the use of a mask does not allow for accurate alignment to sample features. Second, and more importantly, the dimensions of the etched holes are very greatly limited by the dimensions of the mask's line openings. Using the fabrication method described in this section, the narrowest line openings demonstrated for the silicon masks were of the order of 40 μm. For the proposed solar cell rear surface contacting application, smaller diameter openings would be desirable so that the contact regions can be positioned closer for the same metal–silicon interface area.[11]

CONCLUSION

New-generation solar cells, with passivated rear surfaces and localized metal contacts, need new dielectric patterning techniques that facilitate high patterning resolution, low production costs and the avoidance of damage to the underlying semiconductor material. The presented results demonstrate that grooves as narrow as 20 μm can be etched using AJE in 75 nm thick dielectric layers, while avoiding the damage to the underlying silicon substrate often caused by lasers. The method can be used to etch grooves in 120 nm thick layers of SiO_2 as well as 75 nm thick layers of SiN_x, $SiON_x$ and Al_2O_3 deposited by PECVD. The processing parameters, such as the gas flow rates, platen movement speed and number of printing passes, can be varied to fine-tune the method for particular etching requirements. Finally, the high positional accuracy of the AJP enables ready alignment of the etching to previously patterned regions, a property that may find application in a number of recently developed selective-emitter solar cell designs which currently use aligned screen printing for metallization.[14,15] Aerosol jet etching is currently being applied to innovative solar cell designs under development at UNSW and will likely continue to be a catalyst for further solar cell research.

Future work will look more closely at developing etching and patterning processes for high throughput processing in order to suit the requirements of commercial solar cell manufacturing. More specifically, an examination of AJE process stability over longer periods of operation will be required.

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