Journal of Imaging Science and Technology® 52(1): 010508–010508-7, 2008.

Three-Dimensional Architecture of Multiplexing Data Registration Integrated Circuit for Large-Array Ink Jet Printhead

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Abstract. *This article proposes a novel architecture of high selection speed three-dimensional data registration circuit for ink jet applications. With the configuration of three-dimensional data registration, the number of data accessing points as well as the scanning lines can be greatly reduced for large array ink jet printheads with nozzles numbering more than 1000. This integrated circuit architecture involves three-dimensional multiplexing with the provision of a gating transistor for each ink firing resistor, where ink firing resistors are triggered only by the selection of their associated gating transistors. Three signals: selection, address, and power supply, will be employed together to activate a nozzle for droplet ejection. The total number of data accessing points of the three-dimensional configuration will be the cubic root of the nozzle number with each jet controlled by five input lines, including multiplexing data latches and shift registers. The simulation and experiment results demonstrated a reduction of scanning time by up to 67% thanks to the reduction of lines for scanning when compared to a two-dimensional configuration. The total circuit area, 2500×2500 μm^2, will be 80% of the circuit area by three-dimensional configuration for 1000 nozzles. This device has been designed, fabricated by CMOS 0.35 μm process, and characterized. © 2008 Society for Imaging Science and Technology.*
[DOI: 10.2352/J.ImagingSci.Technol.(2008)52:1(010508)]

INTRODUCTION

In the past few decades, the design of advanced ink jet printheads has been working on the optimization of printing quality and speed while minimizing cost. As the nozzle number increased from tens to hundreds while keeping a constant number of data accessing points, two-dimensional (2D) arrayed switches[1–5] have become the most commonly employed architecture of driving IC (integrated circuit) in commercial ink jet printheads. The number of data accessing points will be $X(\text{Pads}) = 2 \times \sqrt{Y} + 1$ ($Y \sim$ nozzles), which is equal to 21 if the nozzle number is 100. Figure 1 shows the schematic diagram of a conventional 2D address selection circuit for a 25 nozzle integrated printhead.[6–9] However, if the nozzle number increases further from hundreds to thousands in a large-array-format ink jet printhead, not only will the data accessing points be easily increased to hundreds, but also the scanning time will significantly rise, which deteriorates the performance of ink jet printing. In order to break the aforementioned performance limitation, this study proposes a three-dimensional (3D) data registration scheme to reduce the number of data accessing points as well as the scanning lines while keeping a small circuit area for driving large-array ink jet printheads with nozzle numbers more than 1000. The total number of data accessing points will be $X = 3 \times \sqrt[3]{Y} + 1$, which is 31 for 1000 nozzles by the 3D novel design, and the scanning time is reduced to 30% (or scanning speed increases at least threefold), thanks to the greater

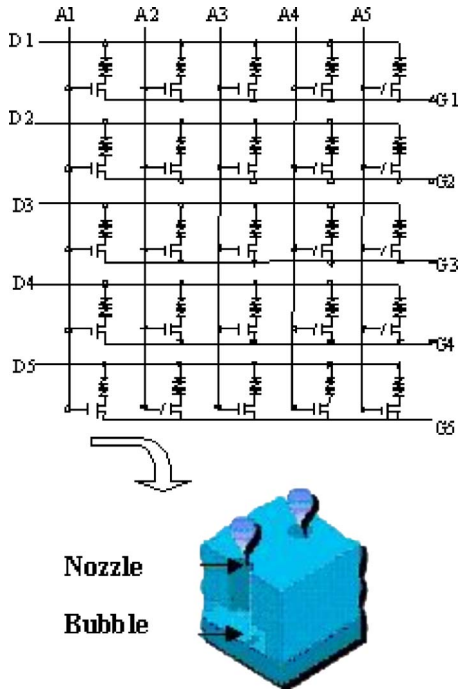

Figure 1. Two-dimensional multiplexing driving circuit for ink jet printheads.

Received Aug. 2, 2006; accepted for publication Nov. 20, 2007; published online Feb. 12, 2008.
1062-3701/2008/52(1)/010508/7/$20.00.

Table I. Performance comparison among 1D, 2D, and 3D driving schemes.

X:Pads, Y:Nozzles	$X \sim Y+1$	$X=2\times\sqrt[2]{Y}+1$	$X=3\times\sqrt[3]{Y}+1$ (X:Connection lines,Y:Nozzles)
Nozzles	1000	1024	1000
Heaters	1000	1024	1000
Resolution (dpi)	300	300 ~ 600	>600
Print swath(in)	1/6	1/3	>1/3
Interconnect pad	1001	65	31

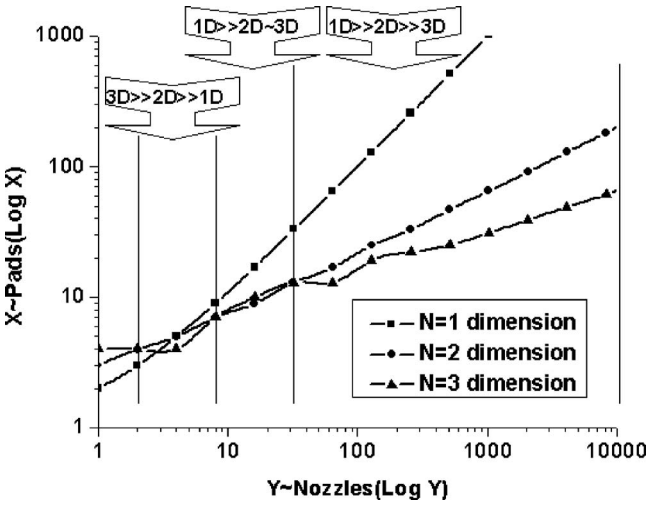

Figure 2. The numbers of required connection pads for 1D, 2D, and 3D control circuit.

reduction of lines for 3D scanning. The comparison among 1D, 2D, and 3D architectures is listed in Table I. As the number of nozzles increases, a driving circuit with higher dimension can effectively reduce the pad number. To illustrate the effectiveness of the circuit dimension to accommodate nozzles, three curves for calculating the pad numbers from 1D, 2D, and 3D control circuits are shown in Figure 2. The 1D case increases most rapidly while the 3D one increases slowest. There are two important intersections among the three curves, with the first one in a nozzle number of 10 and the second one in 30, which means the 1D circuit is suitable for controlling less than 10 nozzles, while 2D circuit is better for tens of nozzles. When the number of nozzles is increased significantly to larger than 30, which may be in a range of hundreds to even thousands, a 3D architecture is necessary to reduce the number of pads to tens.

DESIGN

A mixed-signal analog/digital/power application-specific integrated circuit (ASIC) that integrates all the functions required to drive and control the ink jet printhead is designed for the operation of large-format ink jet nozzles. The general strategy that we employ is to integrate all relatively small-signal electronic functions into one ASIC to minimize the total number of components. This strategy demonstrates

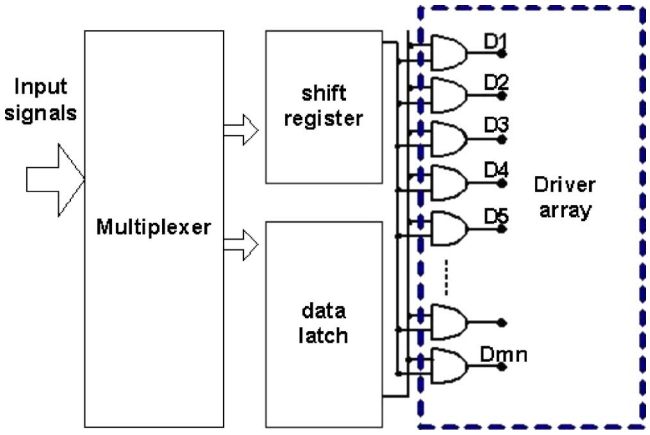

Figure 3. Function block of the control system.

that both the cost is lowered and the amount of the printed circuit board area is reduced. Based on this concept, a smart 3D multiplexed driver for thermal ink jet printheads with more than 1000 nozzles is proposed and the circuit architecture is shown in Figure 3. Three lines are employed to control the firing of one jet, including voltage, shift register, and data line. Each heater resistor requires a voltage line for the driving current flow and shares the same ground with the other resistors. The resistors are individually addressable to provide unconstrained signal permutations by a serial data stream fed from the controller. The shift register is employed to shift a token bit from one group to another through AND gates to power the switch of a jet group. The selection of a jet is thus a combination selection of the shift register for the group and the data for the specific jet. Such an arrangement allows encoding one data line from the controller to provide data to all of the jets, permitting high-speed printing by shortening the jet selection path[10,11] and low IC fabrication cost from the greater reduction of circuit component numbers.[12–15]

In controlling the firing of one heater resistor, the proposed 3D design (illustrated in Figure 4) reveals two parts of the control circuit: the pass-gate device (for signal path) and the power switch device (for power path). The pass-gate device is controlled by address (A) selection and selection (S), while the power line is controlled by power supply (P) selection. To activate one heater, all P, A, and S selections are required to be powered simultaneously. For example, to turn on heater 1, P1, A1, and S1 need to be set to "high" at the same time.

To understand the required threshold voltage V_{th} for turning on the *n*-type metal-oxide semiconductor (NMOS) driver and the driving current for heater resistor, NMOS circuit theory is employed for the calculation. The robustness of the driving current over the variation of the driving signal is estimated by bias sweeping condition. That is, as V_{th} remains constant, the IV characteristics of I_{ds} and V_{ds} are calculated with the variation of V_{gs} from 0 to 9 V.

In the driver transistor, to maintain a high robust V_{th} for consistent circuit turn-off property and low R_{on} for heater driving, the following conditions are considered:

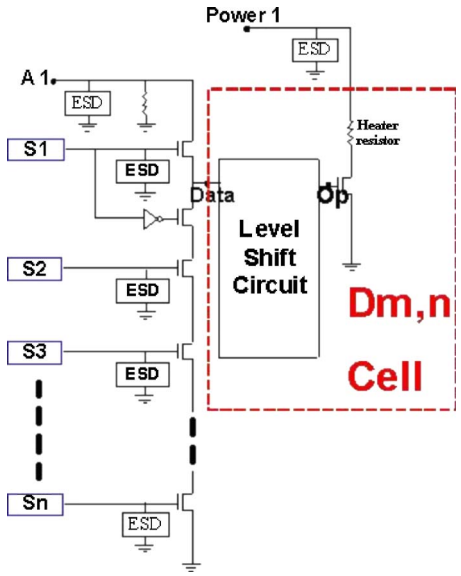

Figure 4. Driving circuit of three-dimensional architecture.

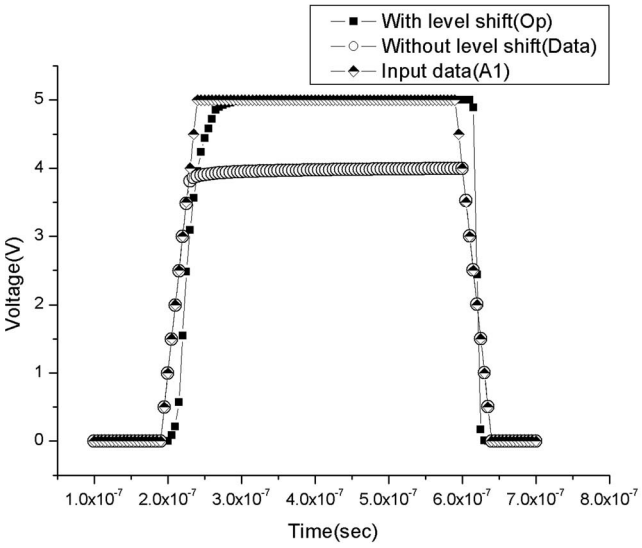

Figure 6. Transient simulation of the input and output signals of the level shift device.

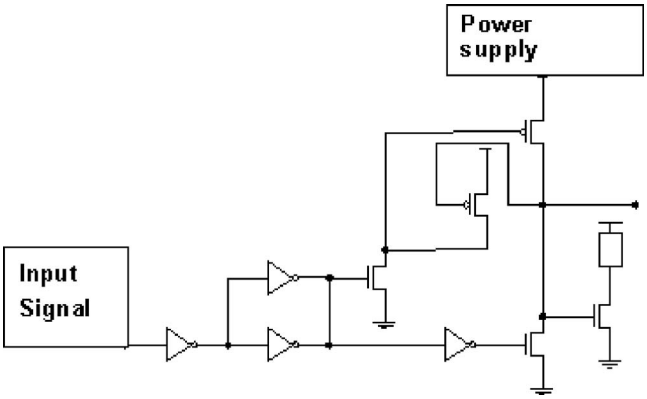

Figure 5. Level shift circuit.

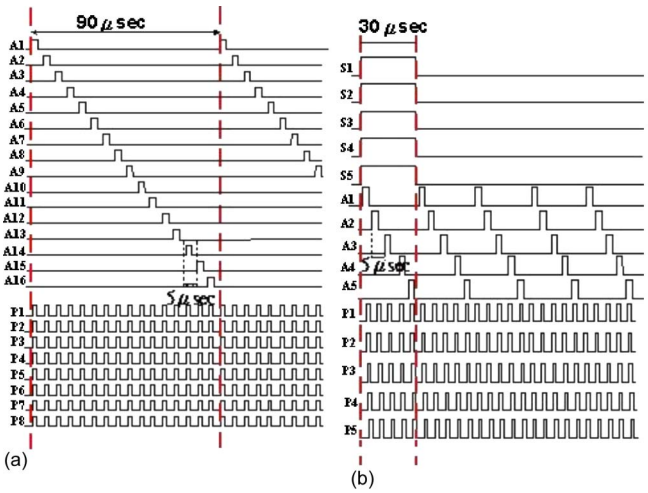

Figure 7. The sequence of driving signals from (A) 2D architecture and (B) 3D architecture.

In the subthreshold region of gate voltage V_G ($V_G < V_{th}$), the leakage current I_D will be exponentially related to $V_G - V_{th}$, as shown in the following equation,[16,17] representing the larger difference between V_G and V_{th}, giving a smaller leaking current I_D:

$$I_D \sim \exp\left\{\frac{q}{kT}(V_G - V_{th})\right\}.$$

At the same time, V_{th} also has a negative temperature coefficient around -3 mV/°C for a substrate doping with $NB = 3 \times 10^{15}$ cm^{-3}, N-type substrate background doping, so thermal guard ring design is required to reduce the sensitivity of V_{th} to the temperature variation.

To consider the previous two effects and keep the leakage current identification smaller than 0.5 μA at $V_D = 10$ V for preventing small bubble formation as well as the enough window for safe turn-off voltage swing, the estimated minimum V_{th} will be 1.4 V,[18] including 0.5 V for V_G swinging and 0.9 V from temperature variation (25°C–325°C), respectively. However, to lower the substrate doping level for increasing V_{th} will reduce the charge mobility to increase the output resistance Ron (usually smaller than 3 Ω), which isnot favored for heater driving. As a result, deep junction doping to reduce effect channel length is desired to maintain small Ron while keeping enough V_{th}.

On the other hand, to enhance the signal level for rapid driving, a level shift device is employed to hoist A and S signals, as shown in Fig. 4. Figure 5 shows the design of the level shift circuit consisting of p-type metal-oxide semiconductor (PMOS) and NMOS power devices for the compensation of the drift of heater resistors from fabrication variation to stabilize the thermal bubble formation. The transient response of the input and output signal before and after the employment of the level shift device is shown in Figure 6.[19,20] The signal demonstrates that not only the switch speed is raised by the level shift device, but also the voltage has been enhanced to 5 V, higher than those of the nonlevel-shift device.[21]

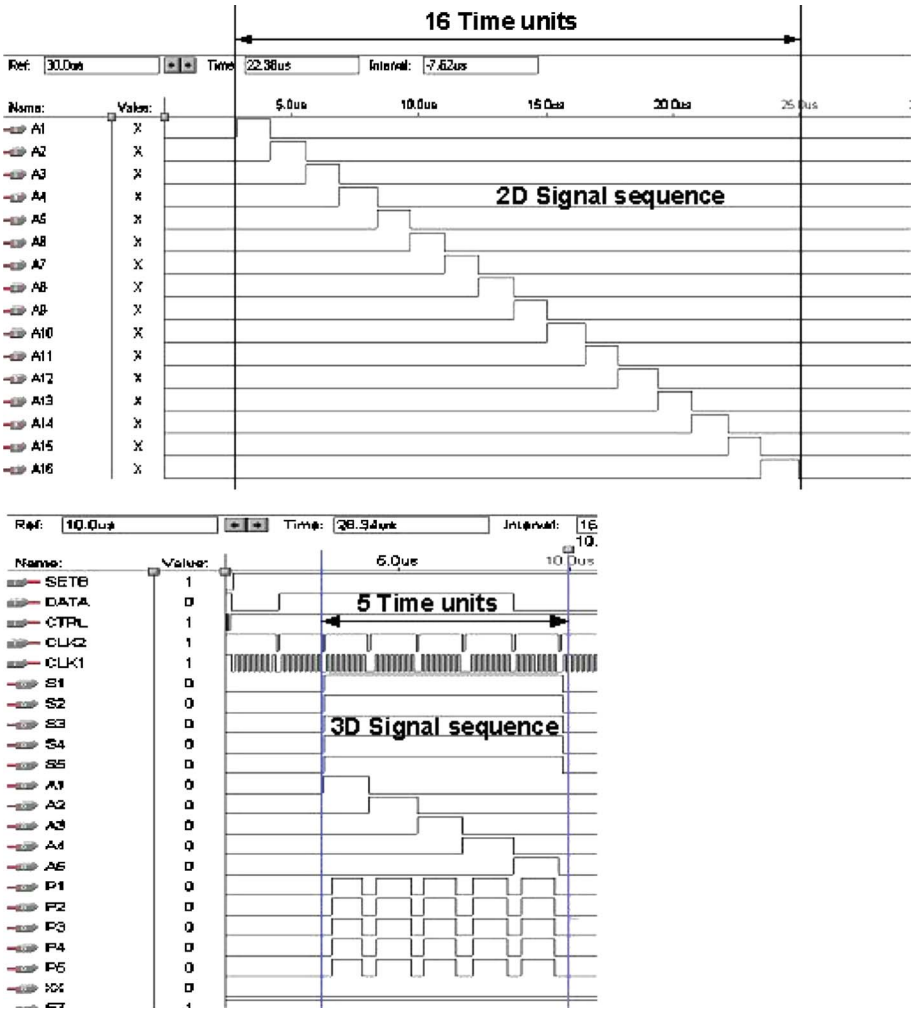

Figure 8. Simulation results of 2D and 3D circuits for signal scanning over 125 nozzles.

SIMULATION AND EXPERIMENT

The 3D multiplexer was fabricated from 0.35 μm 2P2M 5V/5V silicon (double poly double metal, V_{ds}/V_{gs}) by high voltage and mixed-mode process [Taiwan Semiconductor Manufacturing Company Ltd (TSMC), Taiwan, ROC] for fabrication of thermal ink jet printheads with more than 1000 nozzles and 31 controlling pads.

In the signal flow design, ink jet nozzles are usually scanned over one by one without jumping on unfiring nozzles. As a result, for the ink jet head with 125 nozzles, a 1D, 2D, or 3D circuit architecture will need 125, 16, and 5 unit times for scanning over all of the nozzles, respectively, as shown in Figure 7. Therefore, the scanning time of the 3D multiplexing circuit from the first address line to the 16th, as an example, takes only five units of clock time from the simulation result in Figure 8, much faster than that of the 2D configuration with 16 units of clock time. Thus, the maximum scanning time for the 3D circuit will be reduced to 30% of that in the 2D case.

To simultaneously write signals into the driving circuit, multiplexer data latches and shift registers are employed by

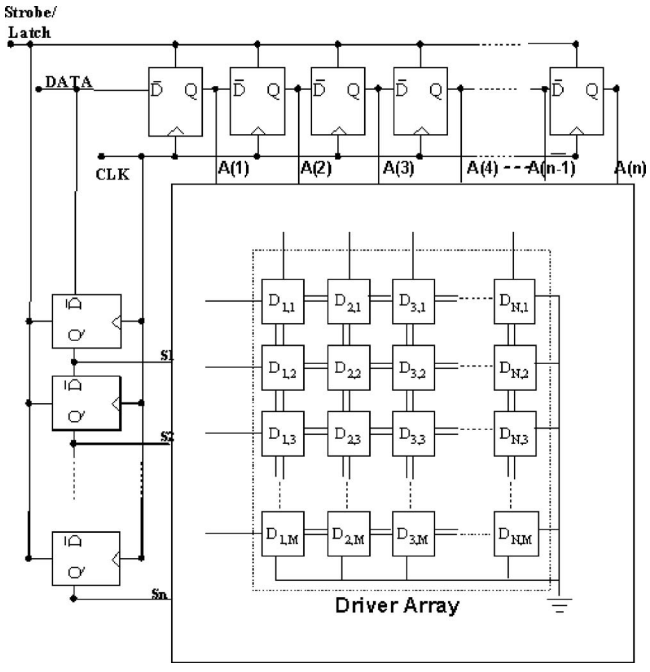

Figure 9. SPICE simulation results on the generation of A selection signal.

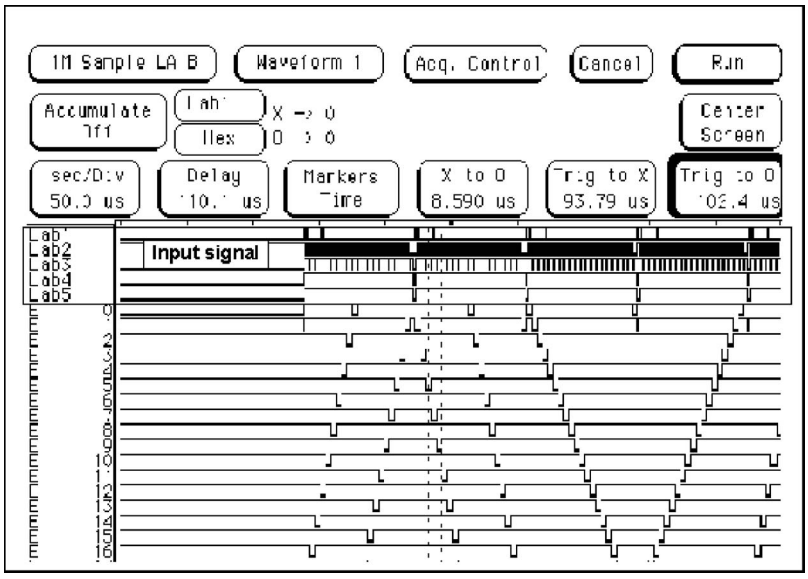

Figure 10. The design schematics of data latches and shift registers.

the application of commercially available CMOS ICs, as shown in Figure 9. Small numbers of shift registers, control logics, and driving circuits can be electrically connected and integrated with ink jet printheads using standard CMOS processes. The desired signal for S selections and A selections can be preregistered and latched in the circuit for one time writing.

RESULTS

In the logic analysis, the relationship between the ASIC input and output is shown in Figure 10. The input signals include DATA (signal for selected nozzle ejection), CLK1 (signal to scan DATA signal), CLK2 (signal to latch DATA signal), CTRL (signal to select enable type), as well as SETB (the time sequence to set up CTRL), and the output signals match the designed ASIC signals very well.

The Simulation Program with Integrated Circuit Emphasis (SPICE) simulation result on the relationship of input and output signal at 5 μs clock time is shown in Figure 11, demonstrating the successful application of CLK1 (8 bits) for scanning input DATA (first and fourth group) signal (S selection), and CLK2 to latch and address to a5, a6, a7, and a8 as well as a10 (A selection) for the generation of output signals.

Figure 12 shows a photograph of the fabricated IC prototype for driving 125 nozzles. Much care must be taken in the layout of the metal layers in order to avoid electromigration from device latch-up[22] by the design of the electrostatic guard ring, as shown in Figure 13. The chip area is 2.5×2.5 mm and was fabricated by a two-poly four-metal 0.35 μm twinwell CMOS technology (TSMC). Each transistor is surrounded by a full guard ring for preventing electrostatic shock.[23,24] The testing result of the IC shown in Figure 14 demonstrated the scanning of 125 nozzles takes 60.5 μs for 2D circuit architecture, while 20.5 μs for the 3D one, representing a time saving of 40 μs or a 67% time reduction. This result is very close to the simulation one of the IC shown in Figure 15. Figure 16 demonstrated the visualization of thermal formation.[25] The signals for sequential nozzle driving and the measured results from the fabricated chip are shown in Figure 17. The probe points N1N97 and N5N204 represent signals (S5, A5, and P5) on 3D module D55, and (A5, P5) on 2D module D55, respectively. The

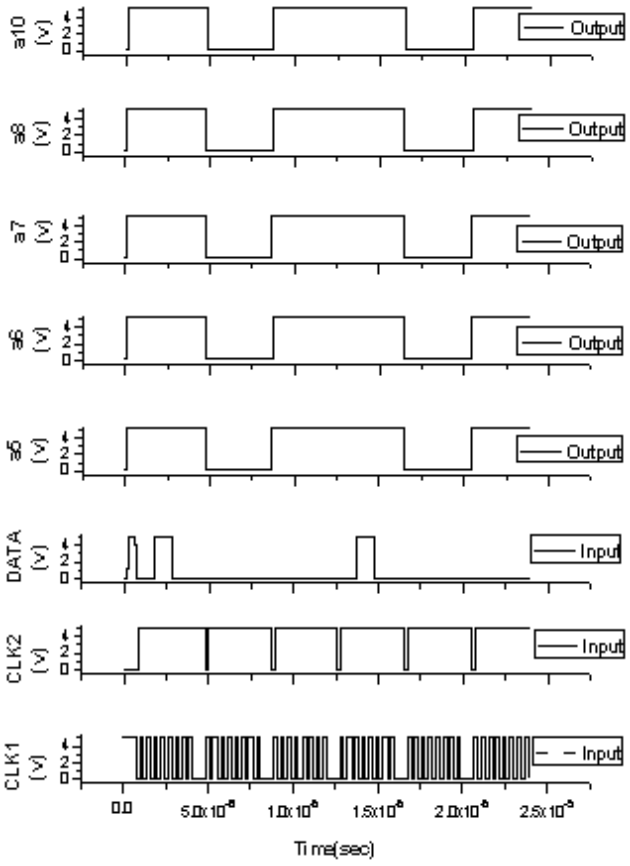

Figure 11. Logic analysis of the 3D multiplexer.

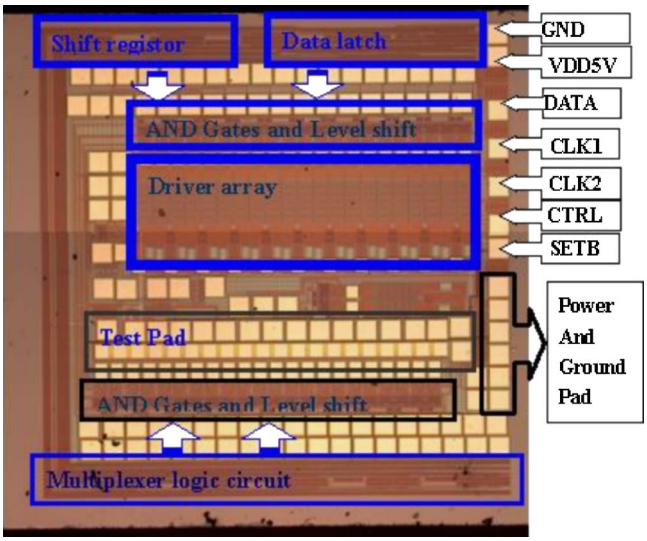

Figure 12. Chip photograph and the architecture.

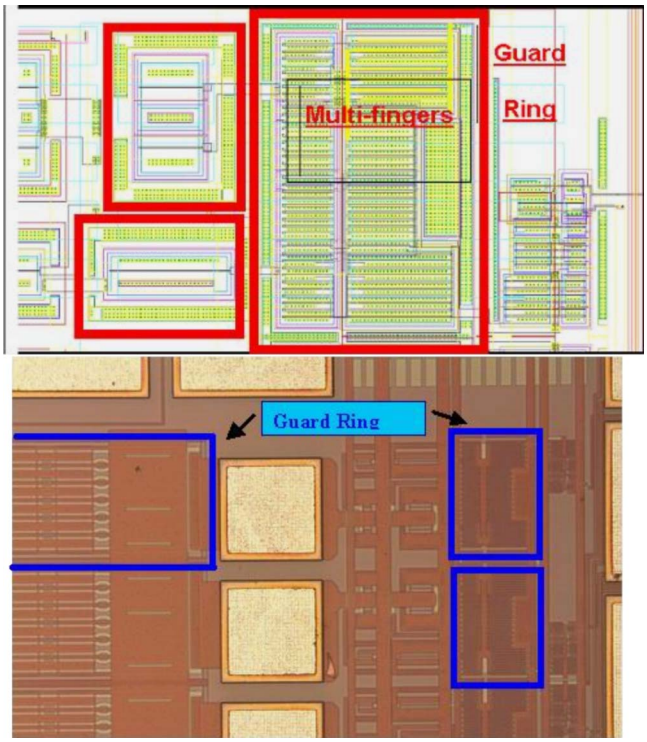

Figure 13. Guard ring surrounding devices of layout and real chip.

measured results verify that the scan speed by the 3D architecture is 34.4 μs faster than that by the 2D architecture with similar nozzle number. The settling time of 0.35 μs is also faster in the 3D case than that of 0.5 μs in the 2D architecture.

CONCLUSION

This article proposes a novel architecture of high selection speed 3D data registration for driving large-array ink jet printheads. The 3D driving architecture has successfully reduced the total number of control pads to 31 for 1000 nozzles as well as the scanning time up to 67% with a higher signal rising speed and smaller circuit area. All the

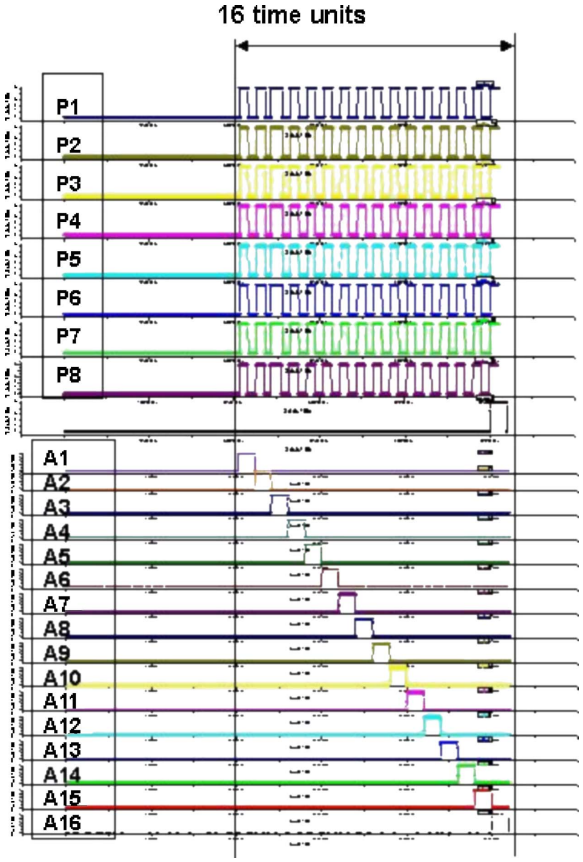

Figure 14. Testing result of the 2D architecture circuit.

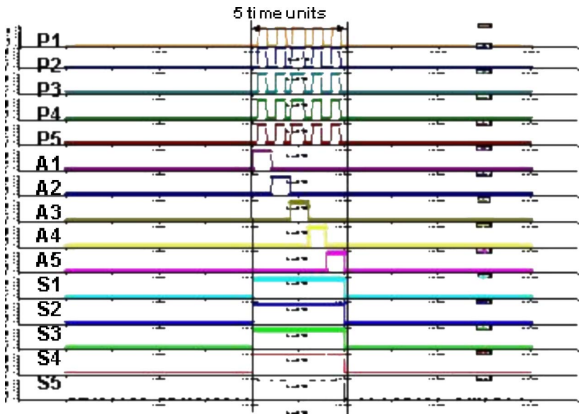

Figure 15. Testing result of the 3D architecture circuit.

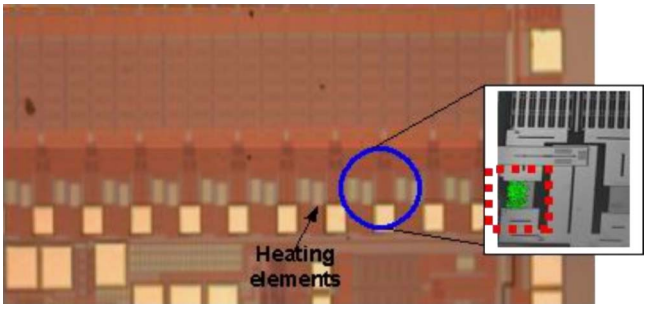

Figure 16. Visualization of thermal formation.

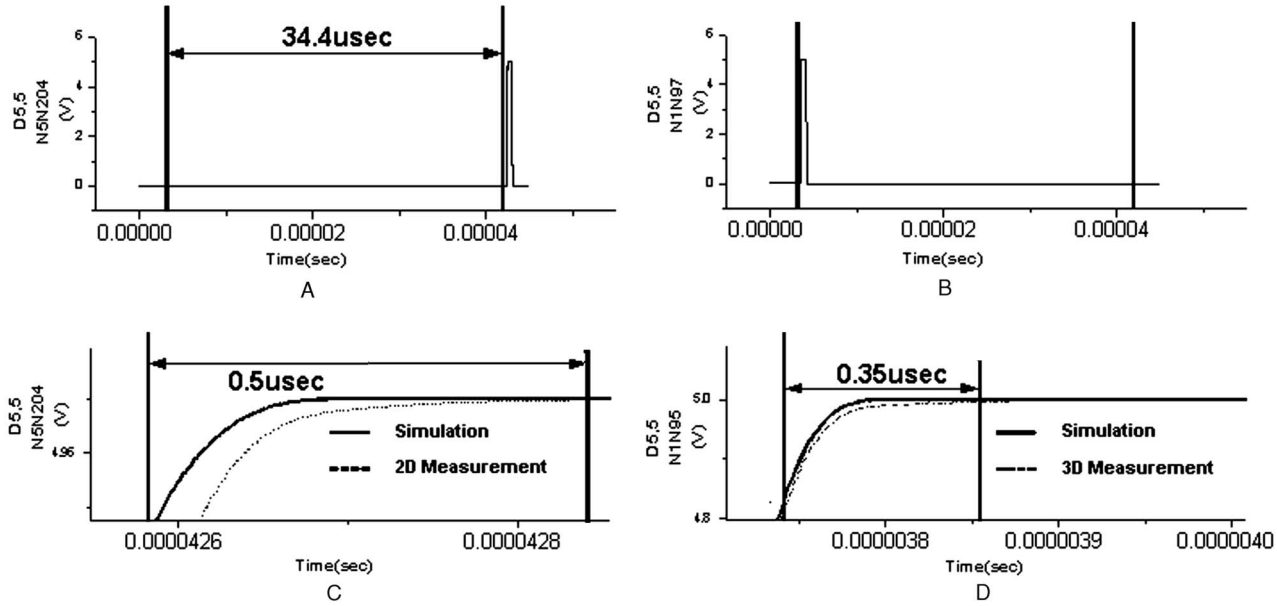

Figure 17. Experiment results for driving the nozzle D5,5 by 2D (A and C) and 3D (B and D) architect circuit. A and B compare the time lag, C and D compare the signal rising time.

subcircuits, including power control, digital I/O, analog-to-digital converter, and power drivers were integrated into a single device. This circuit has been designed, fabricated, and characterized. It demonstrated not only the functionality in the ink jet application but also the consistency between simulation and experiment results.

ACKNOWLEDGMENTS

The authors would like to thank the Chip Implementation Center (CIC), Taiwan, for organizing the chip fabrication. This research was supported by the National Science Council through Grant No. NSC 94-2212-E-007-067.

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