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A low noise CMOS image sensor with in-pixel OTA and intra-scene HDR feature

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Abstract

A low-noise CMOS image sensor (CIS) with intra-scene high-dynamic-range (HDR) feature is presented. The design employs in-pixel 5-transistor (5T) operational transconductance amplifier (OTA) in open-loop configuration to achieve high gain to amplify a weak signal under low illumination. A unity-gain configuration is adopted for high level illumination, and it can avoid saturation at the output, thereby enhancing the overall dynamic range. Noise suppression is further enhanced through analog correlated double sampling (CDS) in the column programmable gain amplifier (PGA) and digital CDS after analog-to-digital conversion, effectively suppressing kT/C noise, low-frequency noise and offset. A prototype was developed using 180 nm CIS process, and the characterization results show that the sensor has a low input-referred noise of 0.67 e^-_{rms} and dynamic range of 80 dB. The proposed approach provides a practical path toward low-noise, wide-dynamic-range CIS architectures and can be extended to future pixel-parallel readout schemes.

Introduction

Modern semiconductor processing technology have enabled CMOS image sensors (CISs) to benefit substantially from technology scaling, making ultra-low noise performance possible and even enabling photon-electron counting with deep sub-electron input-referred noise. Combined with 3D-stacking technologies, pixel-parallel ADCs for digital-pixel architectures have emerged, offering not only reduced readout-chain noise but also high resolution and high frame rate with global shutter operation [1, 2].

In conventional CIS technologies, however, increasing gain to reduce noise often compromises dynamic range, as the pixel output can saturate. Several approaches have been proposed to address this trade-off. Multi-exposure techniques can extend dynamic range, but they may introduce motion artifacts and flicker under LED illumination [3]. Other pixel-level approaches, such as multiple-gain operation, pixel binning, and in-pixel amplification, can also improve the noise–dynamic-range trade-off [4–8]. However, these techniques often rely on additional in-pixel devices, capacitance, or routing resources, which increase design complexity and may introduce area overhead or fill-factor degradation, especially in scaled pixels. Therefore, the key challenge is to improve both noise and dynamic-range performance while maintaining practical pixel implementation constraints.

This work presents a low-noise CIS prototype that achieves intra-scene HDR using OTA-based pixels and a low-noise readout chain. In low-illuminance conditions, the in-pixel OTA operates in an open-loop high-gain mode to improve signal-to-noise ratio (SNR). Noise is further reduced by analog correlated double sampling (CDS) in the programmable-gain amplifier (PGA) and by digital CDS after A/D conversion [9], thereby suppressing downstream noise contributions. Intra-scene HDR is realized by combining unity-gain and high-gain sampling within the same exposure cycle, avoiding the need for additional in-pixel capacitance. Measurements demonstrate an input-referred temporal noise of 0.67 e^-_{rms} in high-gain mode while achieving an intra-scene dynamic range (DR) of 80 dB. Although the prototype employs front-side illumination (FSI), further performance improvements are expected with advanced nodes and with global shutter implementations targeting high-speed, low-artifact imaging.

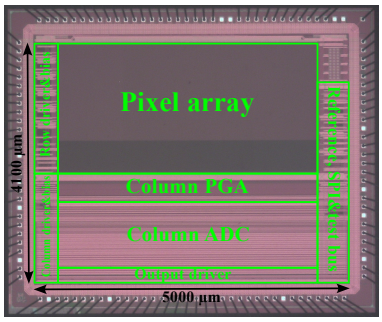

Figure 1. *Die photograph with blocks marked in green box.*

Implemented Architecture and Timing

A prototype chip was implemented in a 180-nm front-side-illuminated (FSI) CIS process for verification. A die micrograph is shown in Figure 1. The test chip integrates a pixel array (including multiple pixel variants for pixel-level characterization), a column programmable-gain amplifier (PGA), a single-slope single-ramp ADC (SS-ADC), and peripheral blocks including a row driver, bias generation, ramp generation, a serial peripheral interface (SPI), a test bus, and an output driver. An in-pixel 5T OTA is used as a front-end amplifier to boost the small sensing-node voltage, thereby suppressing the impact of downstream readout noise. The design was optimized to balance area, power, and bandwidth. To mitigate OTA offset and mismatch, an auto-zeroing MOS capacitor was implemented by utilizing the available space between the photodiode and the OTA. The OTA can be configured in unity-gain mode, enabling the HDR operation by sampling and holding reset and signal levels under two gain configurations within a single exposure.

Figure 2 illustrates the HDR operation of the OTA pixel. After shutter operation, the photodiode is reset and the pixel is prepared for the HDR readout sequence once the row is selected. When RST_{FD} and RST_{OTA} both are turned on, the OTA is reset and auto-zeroed: the common-mode voltage is stored and the offset is canceled in the unity-gain configuration. When RST_{FD} is turned off, the reset level in unity-gain mode is sampled by the

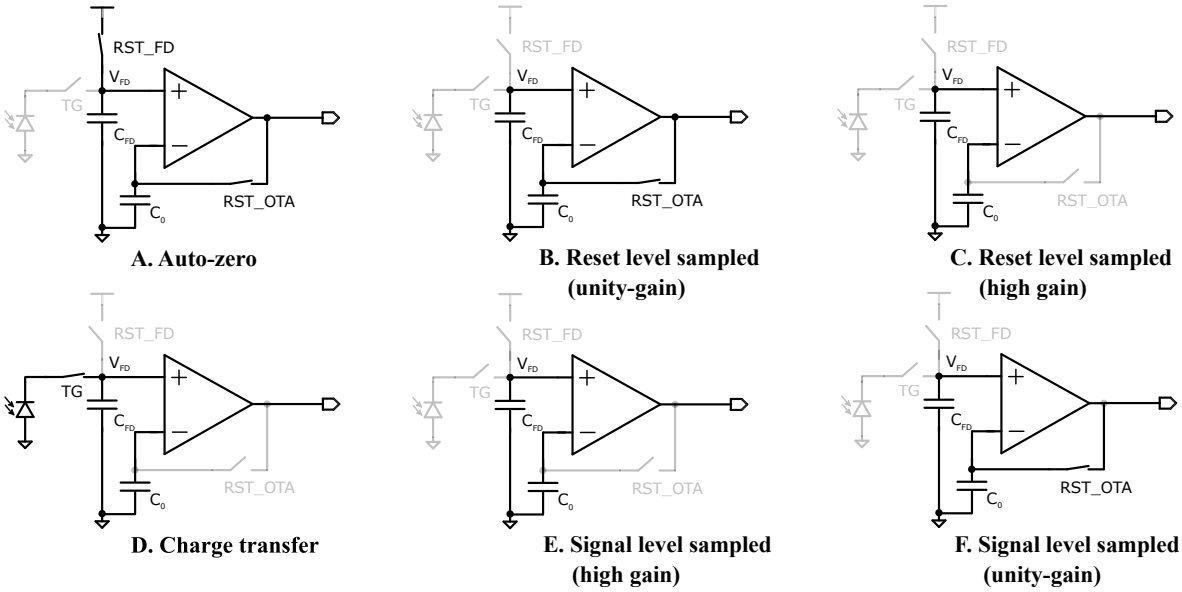

Figure 2. *Sequential operation (step A to F) of OTA pixel under HDR mode.*

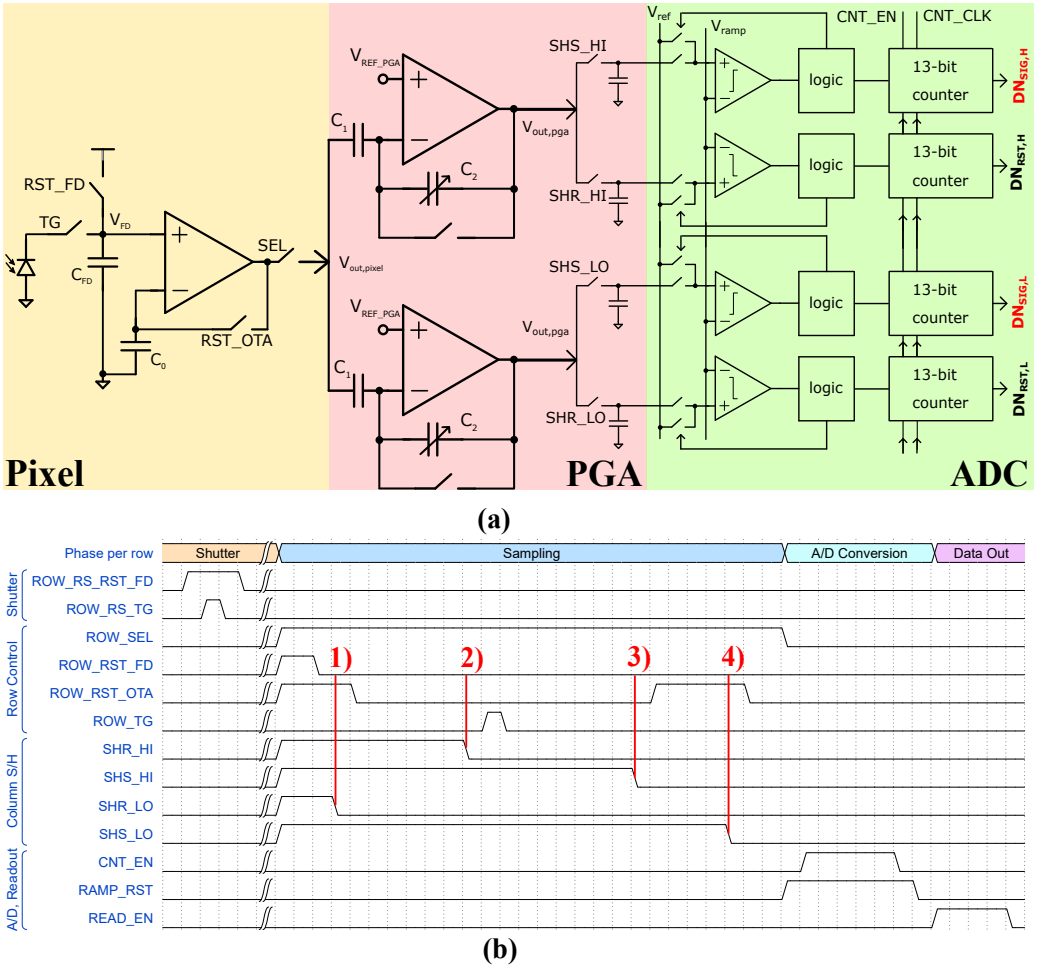

Figure 3. *Signal chain for test chip. (a) Block diagram and (b) timing diagram with 4 sampling points marked.*

column sample-and-hold (S/H) block. Similarly, the reset level under open-loop high gain can be sampled. The transfer gate TG is then turned on for the photon charge transfer, producing a voltage drop at FD node. This drop is amplified under high gain mode and subsequently sampled. After turning on RST_{OTA} again, the same transferred charge is read out through the unity-gain path and sampled. With these steps, the reset and signal samples in both gain modes are available for column-level A/D conversion, enabling intra-scene HDR.

The corresponding schematic and timing are shown in Figure 3, where CDS can be applied in both high-gain and unity-gain configurations to reduce offset mismatch and low-frequency noise. A two-stage CDS scheme is adopted: analog CDS is performed in the column PGA, followed by digital CDS after A/D conversion [6]. Together with the programmable-gain setting in the PGA, this approach provides both extended dynamic range and effective noise suppression. For A/D conversion, a modified single-slope single-ramp ADC [7] is employed. Each column includes two identical readout chains for reset and signal levels, respectively. For each chain, the comparator performs two comparisons—one against the reference level and the other against the corresponding reset or signal level—so that the resulting code is formed from the timing difference. This two-step operation provides first-order self-cancellation of comparator delay mismatch during digital CDS. In addition, row noise arising from ramp or reference variations is largely suppressed, since it appears as a common disturbance across columns.

Characterization Results

Figure 4 shows the input-referred temporal noise versus the nominal column PGA gain for the OTA pixel under two operating modes: an open-loop high-gain mode for low-noise operation and a closed-loop unity-gain mode for high dynamic range. Different in-pixel OTA gains lead to different noise partitioning along the signal chain; in particular, higher front-end gain suppresses the contribution of downstream stages when referred to the input. In unity-gain mode, the input-referred noise decreases rapidly as the PGA gain increases, indicating that the readout-chain noise is progressively attenuated. In open-loop high-gain mode, the dominant noise contribution originates from the pixel front end, and increasing PGA gain provides limited additional benefit. The minimum noise of 0.67 e^-_{rms} is measured at a nominal PGA gain of 7. At higher PGA gains, the amplified pixel offset requires a larger digital CDS offset compensation, reducing the available output range and making the subtraction more challenging.

The SNR curves for different gain configurations are plotted in Figure 5. High pixel-side gain improves SNR at low signal levels, whereas low-gain configurations extend the dynamic range toward higher signal levels. By combining these two gain paths, intra-scene HDR can be achieved within a single exposure. However, careful design is required to mitigate the SNR dip when switching between gain configurations. A captured image under HDR mode is shown in Figure 6. The light source is intentionally placed near the border so that illumination enters from the bottom-left region, resulting in a strongly nonuniform scene. In the high-gain image, shadow details are preserved with increased contrast, while the bright region approaches saturation. In the low-gain image, the strongly illuminated region is not saturated, but shadow details are degraded. Therefore, image fusion of the

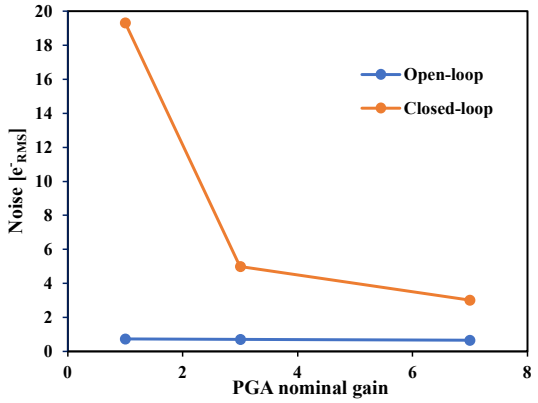

Figure 4. *Input-referred noise vs. PGA nominal gain.*

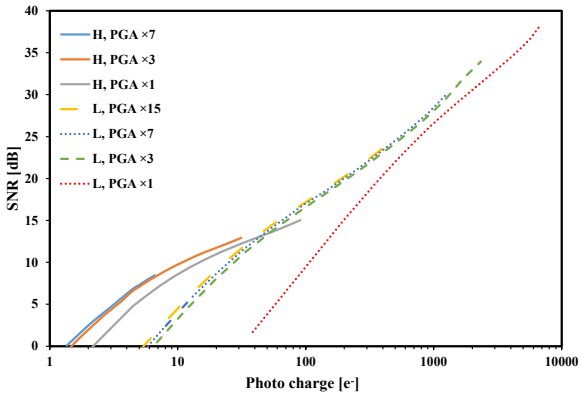

Figure 5. *SNR plot. "H" denotes the open-loop high-gain in-pixel OTA mode, while "L" denotes the closed-loop unity-gain mode. The number indicates the nominal PGA gain.*

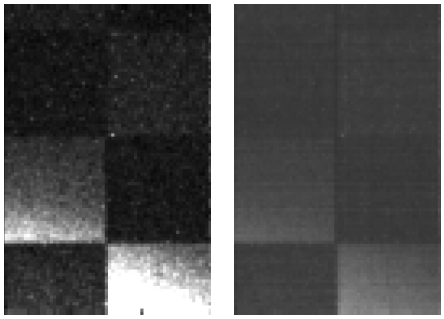

Figure 6. *HDR demo.*

two gain paths is required to produce a single HDR image.

Figure 7 and Figure 8 show the spatial-noise maps of the OTA pixel under unity-gain and open-loop high-gain modes, respectively. As expected, spatial non-uniformity is higher in open-loop operation, since device mismatch and gain variation are amplified. Although post-processing correction (e.g., flat-field/shading correction) can reduce the observed spatial noise, additional effort is still required in the image-processing pipeline. In future work, a closed-loop amplifier with feedback will be implemented to reduce gain variation, improve spatial uniformity,

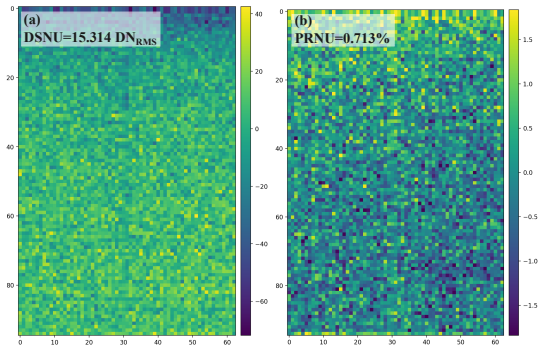

Figure 7. *Spatial noise (dark response non-uniformity and photon response non-uniformity) of OTA pixel when working under unity-gain mode.*

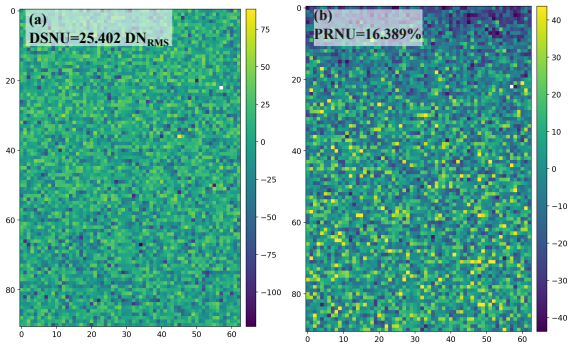

Figure 8. *Spatial noise (dark response non-uniformity and photon response non-uniformity) of OTA pixel when working under open-loop high gain mode.*

and increase bandwidth, enabling a higher frame rate through shorter settling time.

The measured output noise of the implemented column ADC and its breakdown are shown in Figure 9. In this measurement, the pixel array is isolated and a DAC-driven signal is applied to the column bus in order to characterize the column ADC independently. Row noise dominates the total temporal noise and remains within 7 LSB before the output approaches saturation. Both components increase gradually with input level, which is consistent with increased random-walk noise projected from the ramp volt [10]. The results are measured at a 25-MHz counter clock; no clear performance degradation is observed up to 100 MHz, enabling higher frame rate through reduced A/D conversion time.

Conclusion

This work presents a 180-nm rolling-shutter CMOS image sensor featuring an in-pixel OTA front end and a dual-gain readout scheme to achieve low noise and wide dynamic range. The main performance is summarized in Figure 10. Implemented with a 14-µm pixel pitch in a 256×96 array, the prototype achieves an input-referred temporal noise of 2.30 e^-_{rms} in unity-gain mode and 0.67 e^-_{rms} in high-gain mode. A dynamic range of 80 dB is obtained while consuming 33 mW, and the sensor operates at a frame rate above 21 fps under HDR mode. Spatial non-uniformity is characterized by DSNU of 15.3 DN_{rms} (unity gain) / 25.4 DN_{rms} (high gain) and PRNU of 0.71% / 16.4%, highlighting a trade-off between sub-electron noise and increased mismatch sensitivity in high-gain operation. Overall, the results demonstrate the

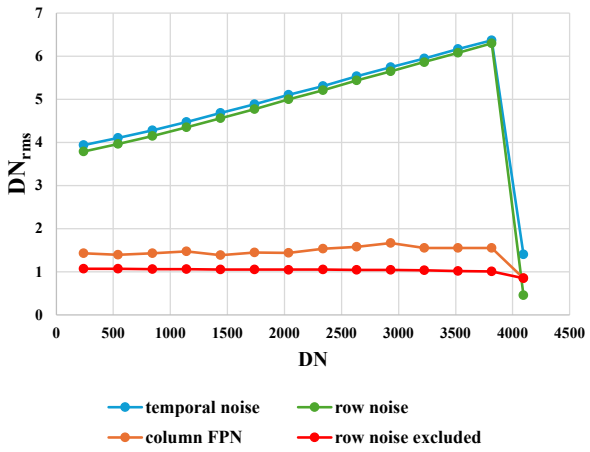

Figure 9. *The output noise of ADC versus signal and its breakdown.*

Parameter	Results
Process [nm]	180
Shutter type	RS
Pixel pitch [µm]	14
Array size	256×96
Noise [e^-_{rms}]	2.30(L) / 0.67(H)
DR [dB]	80
Power [mW]	33
Frame rate [fps]	>21
DSNU [DN_{rms}]	15.3(L) / 25.4(H)
PRNU [%]	0.71(L) / 16.4(H)

Figure 10. *Performance summary.*

effectiveness of the OTA-based pixel and dual-gain readout for low-light imaging with extended dynamic range, while indicating that future improvements should focus on reducing spatial non-uniformity in the high-gain path and improving the frame rate due to the limited output bandwidth.

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Author Biography

Pengfei Xu received his B.Eng (2019) from Huazhong University of Science and Technology, and his M.Sc. (2022) from University of Chinese Academy of Sciences. In 2023, he started the PhD research on low temporal noise CMOS image sensor at KU Leuven, Advanced Integrated Sensing (ADVISE) research group, located in Campus Geel.

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Guy Meynants received his Ph.D.(1998) in electronic engineering from KU Leuven. He is an expert on CMOS image sensors, invented 33 patents and patent applications, and co-authored 70 scientific publications. He has wide work experience: IMEC(1994), cofounder of FillFactory (2000), co-founder and CTO of CMOSIS(2007), and director at Photolitics(2019). He designed various CMOS image sensors for industrial, photography and space applications. Since 2021, Guy is professor at KU Leuven. He is a board member of the International Image Sensor Society.

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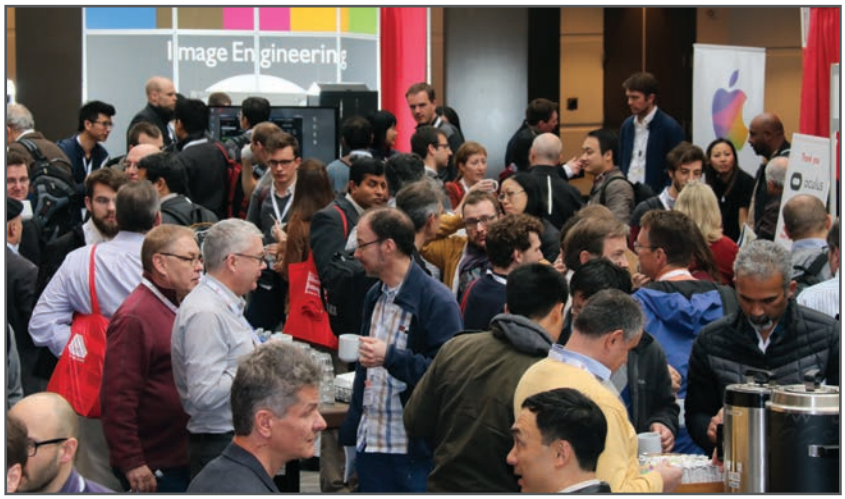

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