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Yield Enhancement in Production of CMOS Image Sensors: Defect Analysis and Solutions

Liviu Oniciuc, Abhinav Agarwal, Joseph Valenzuela, Daniel Chica, Loc Truong;
Forza Silicon (AMETEK Inc.); 2947 Bradley Street Suite 130, Pasadena, California, 91107, USA

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Abstract

Large-format CMOS image sensors used in cinematography are highly susceptible to systematic defect mechanisms that are difficult to detect using conventional wafer-probe testing. This work presents a wafer-level diagnostic methodology that leverages each die's captured image to generate defect and noise maps, which are then reassembled into full-wafer mosaics. This approach exposes spatially correlated defect patterns that electrical probing alone cannot reveal, including wafer-edge localized pixel failures and color-filter non-uniformities. By correlating defect signatures with pixel-level layout coordinates, we traced paired-pixel artifacts to excessive oxide formation at shared inter-pixel vias. Physical failure analysis confirmed the via-related mechanism which prompted the addition of a new cleaning step that significantly reduced wafer-border defects in engineering splits and early production. The same mosaic-based analysis identified concentric blue-channel non-uniformities linked to a specific color-filter processing step. The proposed method enhances visibility into systematic defects, accelerates root-cause identification, and provides a practical, high-resolution tool for improving yield in advanced CMOS image-sensor manufacturing.

Introduction

Large-format CMOS image sensors present unique production and yield-management challenges due to their extremely large pixel arrays and tight process tolerances. Small localized defects such as pixel, cluster, or column errors can significantly impact overall yield [1, 2], especially as resolution increases and sensors move toward large-format architectures [3, 4]. Effective identification, classification, and mitigation of these defect types are therefore essential for controlling cost and ensuring consistent sensor performance.

This defect analysis begins with a structured classification process encompassing communication interfaces, power domains, digital logic, analog subsystems, and the pixel array itself. Within the pixel array, the most common defect classes include row or column defects, pixel-cluster defects, and isolated pixel failures [5]. Examples of these defect types are illustrated in Figure 1 and Figure 2.

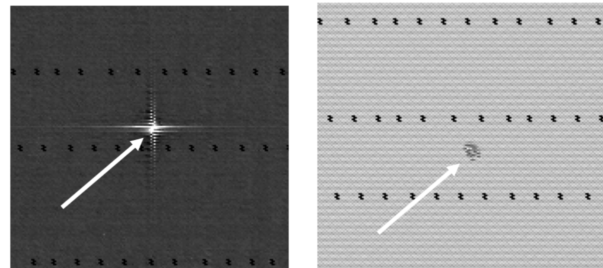

Figure 1. *Cluster defect in the dark (left) and with illumination (right).*

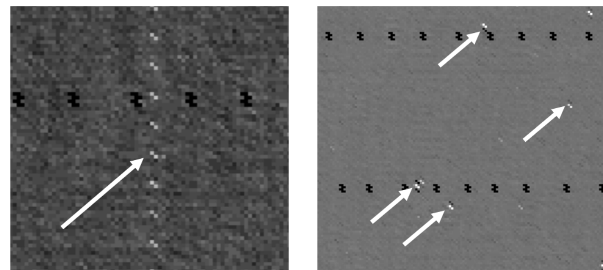

Figure 2. *Column defect (left) and pixel defect (right).*

Understanding whether each issue originates from process variation, contamination, or design-related sensitivities is a critical step in yield optimization. Many of these mechanisms including leakage, STI related stress defects, and via/interconnect issues require physical failure analysis to diagnose accurately [6, 7].

These classifications feed into the end-to-end production workflow (Figure 3), which includes wafer-level testing, optical inspection, material review board (MRB) evaluations, assembly into ceramic packages, final electrical testing, and manual optical inspection.

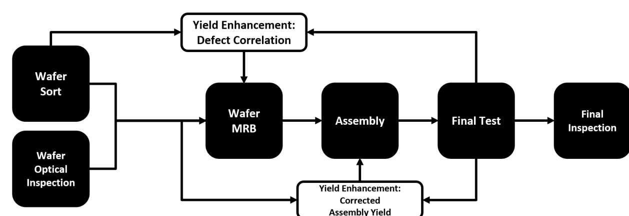

Figure 3. *General production workflow.*

Each stage contributes to improving yield by identifying root causes, classifying defect mechanisms, and feeding corrective actions back to both the fabrication process and the internal design team. The MRB process, in particular, plays a key role in differentiating true pixel-array defects from removable contaminants,

reducing false yield loss and enabling more accurate wafer disposition.

This structured approach to defect detection combined with comprehensive wafer-level and die-level inspections forms the foundation for the yield-enhancement methodology described in this work. It also motivates the development of advanced defect-correlation tools such as wafer mosaics and image-derived diagnostic maps, which further strengthen the ability to identify systematic failure mechanisms in large-format CMOS image sensors.

Objective

The objective of this work is to demonstrate how building the wafer-level mosaic can help to enhance CMOS image sensor yield by identifying and addressing systematic defect mechanisms that degrade device performance and reduce manufacturing efficiency.

Through integrated analysis of electrical probing, die-level image data, wafer-level mosaic reconstruction, cross-sectional microscopy, and collaboration with the wafer-fabrication vendor, the study aims to trace defect signatures to their physical root causes and evaluate process modifications that improve device reliability, and reduce defect density. This method leverages die-generated images and wafer-level mosaic reconstruction to recognize patterns that will help root cause the problem.

Method and Application

In addition to standard semiconductor test wafermaps, the analysis leveraged the fact that each die is capable of generating an individual image. Each image was processed independently to produce a dedicated diagnostic map (e.g., defect maps, noise maps). These maps were then re-aggregated into a full-wafer representation while preserving the physical orientation of each die within the wafer.

Figure 4 illustrates the aggregated defect map corresponding to a low-yield wafer. Application of this processing methodology reveals an increased spatial density of defective pixels, predominantly located at the wafer periphery.

By defining the wafer edge as the region of interest, a unique signature was identified which differed, in both density and shape, from defective pixels in the center of the wafer. Pairs of defective pixels, illustrated in Figure 10, were observed and were clearly discernible in both dark and illuminated images. This defect signature indicates that the defects originate from structures shared between the corresponding pixel pairs.

There was no sensitivity to the reset voltage and the timing experiments did not remove the issue after excluding the pixel charge transfer or reset completely. Looking at the output of the pixel line, the voltage swing looked suppressed for the bad pixels that pointed us to the source follower gate being very resistive. Based on the pixel design a via that was used to connect pixel pairs was determined to constitute the underlying root cause of the observed artifacts, noted in Figure 11. By correlating the precise pixel coordinates in the captured images with their corresponding positions in the design layout, the defects were physically localized within the physical samples.

In collaboration with our foundry partners at STMicroelectronics (Crolles, France), a comprehensive microscopy-based analysis was conducted on the identified via (Figure 11) which

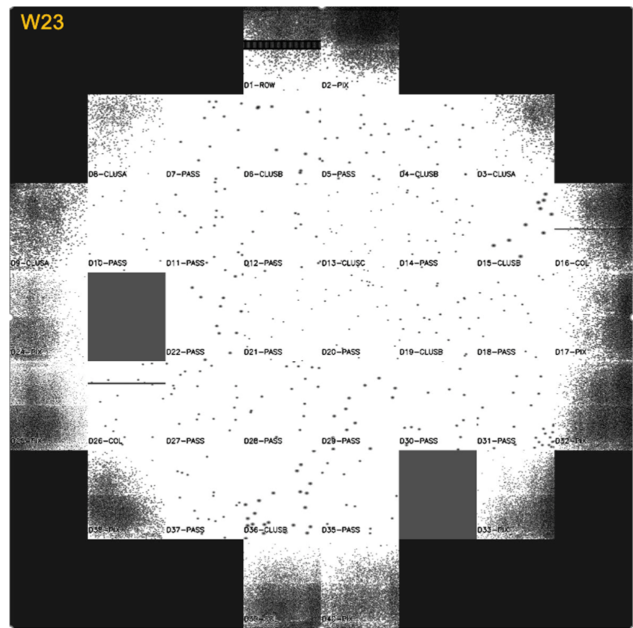

Figure 4. Wafer-Level Aggregated Image Defect Map

enabled a detailed identification and characterization of the underlying defect mechanism.

Transmission Electron Microscopy (TEM) analysis of the contact via shows TiSi interface (Figure 5). Energy Dispersive X-ray (EDX) Cross-sectional imaging at the localized failure site provided a direct comparison between a defective pixel and the corresponding structures in a nominal pixel (Figure 12).

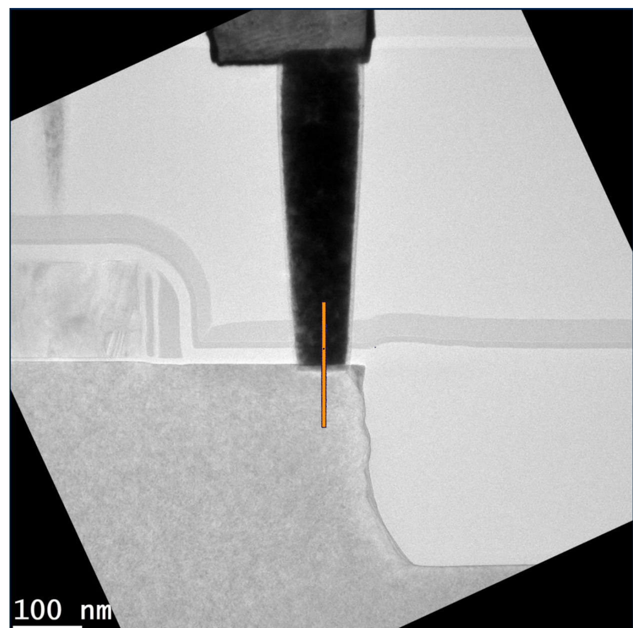

Figure 5. TEM Cross Section of TiN and Silicon interface noted in Orange

The defective pixels exhibited noticeably greater oxide formation at the shared via, resulting in an increased in-pixel resistance associated with these interconnects.

Result

A new cleaning step was added to the wafer manufacturing process to improve the in-pixel contact resistance with results shown in Figure 6.

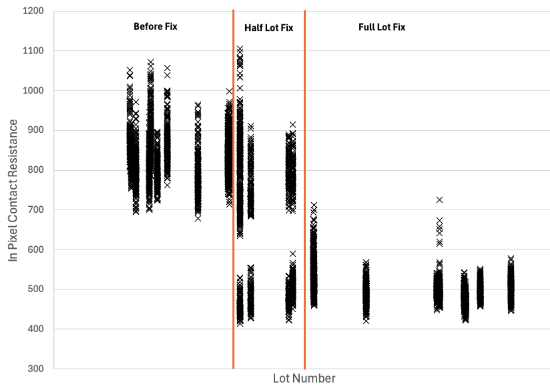

Figure 6. *In pixel contact resistance: [Lots] vs Resistance* $[\Omega/ct]$

The new process recipe was applied to half of the wafers in limited pre-production lots. The results demonstrated a clear correlation between the revised process and a reduction in wafer-border defects. Tracking the new process recipe within a lot, a clear yield improvement is observed in Figure 7. Additionally, mosaics of the reassembled wafer-defect maps for all wafers in the lot are provided, illustrating the direct correlation between the new recipe and the observed defect reduction (Figure 13).

Another example that showed the utility for the wafer-mosaic imaging approach is its ability to highlight defects originating from the color-filter process. By separating the images into individual color planes prior to constructing the wafer mosaic, a concentric defect pattern became evident and was confined to a single color plane. This localization effectively identified the corresponding process layer as the source of the fixed-pattern noise observed in the captured images. Shown are the results of this analysis including a full color-split (Figure 8) and a wafer processed depicting before and after (Figure 9) the corrective action (increased the layer viscosity) that was implemented for the blue color-filter coating.

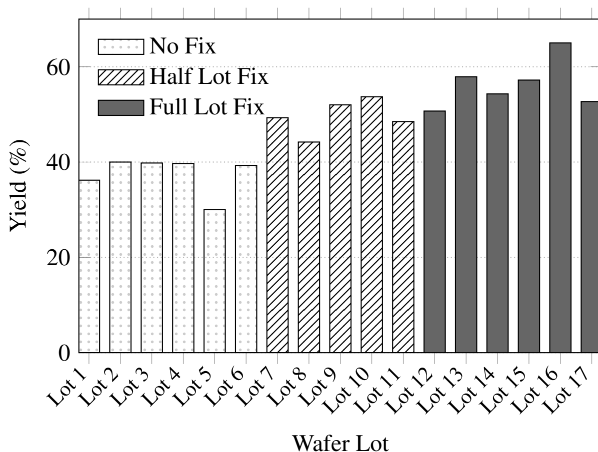

Figure 7. *Wafer lot yield comparing the in-pixel contact resistance fix*

Conclusion

Large-format CMOS image sensors present unique yield-limiting mechanisms, yet there is very limited publicly available work that addresses systematic defect identification at full-wafer scale. Constructing an aggregated wafer mosaic from individual captured images reveals subtle features and defect patterns that would otherwise remain undetected.

By integrating image derived defect mapping with design layout correlation and physical failure analysis, the method enables detection of process-induced mechanisms that conventional electrical test cannot resolve.

This expanded spatial perspective enables the identification of additional opportunities for process and design optimization, ultimately supporting the delivery of high-quality image sensors.

Acknowledgments

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Author Biography

Liviu Oniciuc, Director Integrated Product Services, Forza Silicon (AMETEK Inc.); Lecturer, Cal Poly Pomona

Abhinav Agarwal, Manager Design Engineering, Forza Silicon (AMETEK Inc.)

Joseph Valenzuela, Manager Integrated Product Services, Forza Silicon (AMETEK Inc.).

Daniel Chica, Product Engineer - System Design, Forza Silicon (AMETEK Inc.)

Loc Truong, DVP Business Manager, Forza Silicon (AMETEK Inc.)

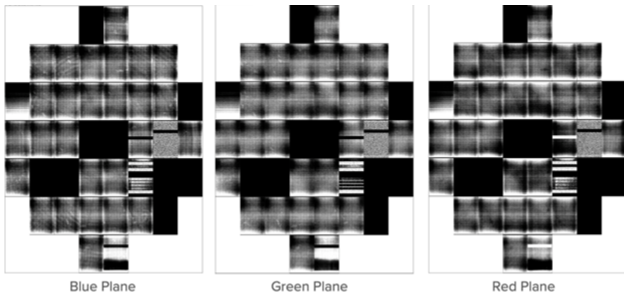

Figure 8. *Wafer image mosaic split per color plane*

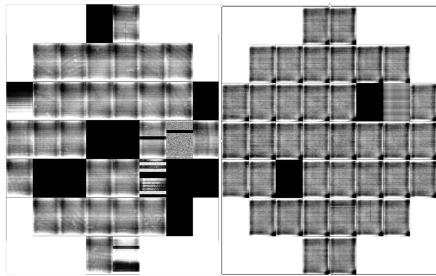

Figure 9. *Wafer image mosaic of blue CFA layer before (left) and after (right) the fix*

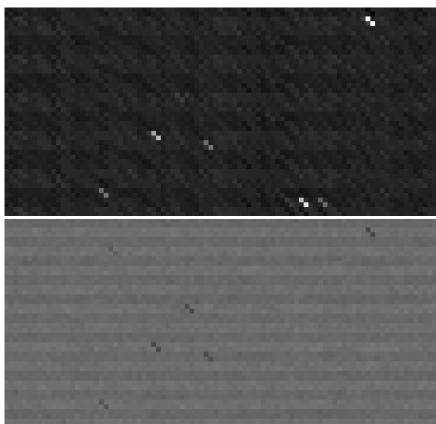

Figure 10. *Defective pixels with diagonal artifacts in the dark (top) and the illuminated (bottom) image*

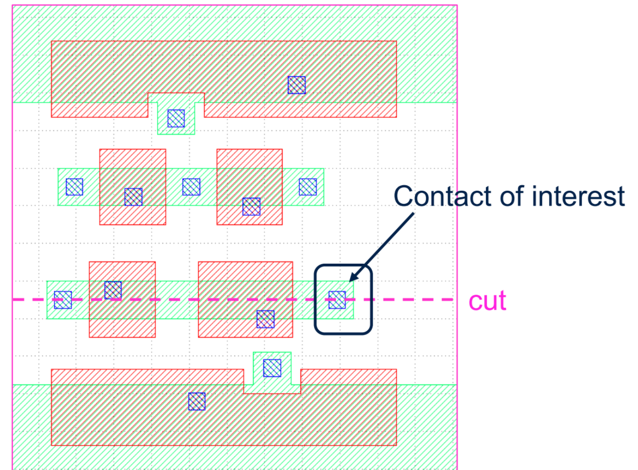

Figure 11. *Shared via localization*

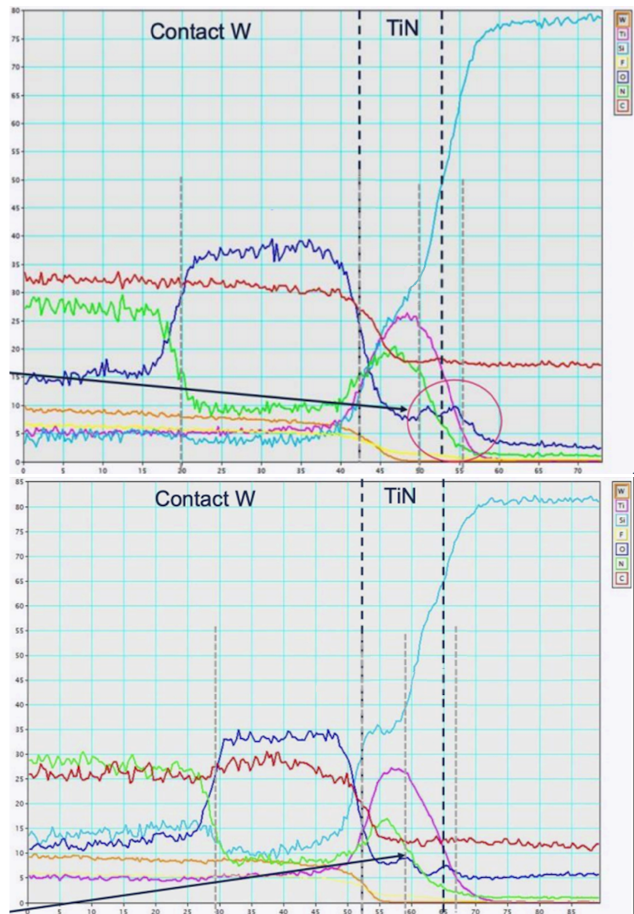

Figure 12. *EDX Cross Section of via shows TiSi interface oxidation (cyan). The x-axis is element [%], the y-axis is distance [nm]. Defective Pixel (top) vs. Nominal Pixel (bot).*

REF	1		3	4	6			10	12	13	15	17	18	19			23	24	
NEW		2			5	7	8	9	11		14	16			20	21	22		25

Waferlot Split: reference (REF) vs revised (NEW) recipe

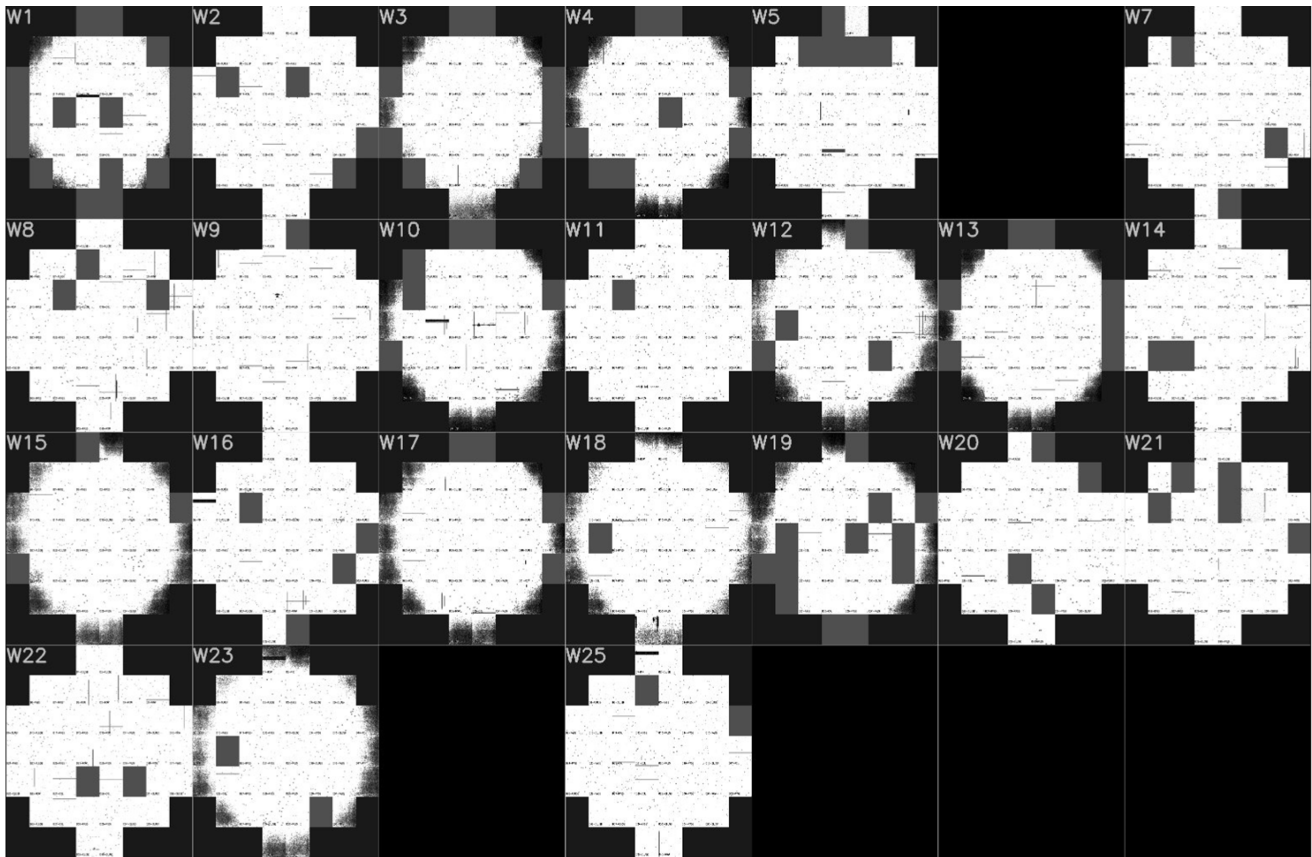

Figure 13. *Wafer defectmap mosaic for an entire wafer lot. Note the wafers with defects at periphery in waferlot split. Wafer 6 and wafer 24 were scrapped*

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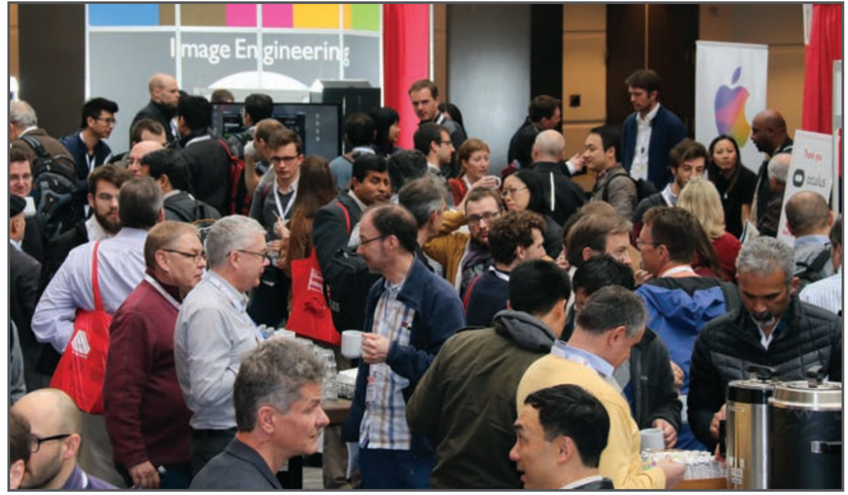

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