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A Global Shutter Proximity Capacitance CMOS Image Sensor for High-precision and High-speed Capacitance Imaging

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Abstract

This paper presents a newly developed global shutter proximity capacitance CMOS image sensor capable of high-speed and high-precision capacitance detection using noise cancellation technology. The chip was fabricated by a 0.18 µm CMOS process technology. It integrates high-density Si trench capacitors as in-pixel memories and features a $320^H \times 640^V$ pixel array with a pixel size of 12 $\mu m^H \times 6\ \mu m^V$. Experimental results demonstrate that the sensor successfully captures distortion-free capacitance images and simultaneously achieves a high frame rate of 90 fps and a high detection precision of 12 zF. Furthermore, a burst mode utilizing in-pixel memories enables continuous signal acquisition, achieving an unprecedented detection speed of 167 kfps. The developed sensor is expected to significantly improve inspection efficiency in diverse fields, including manufacturing and life sciences.

Introduction

Proximity capacitance image sensors are capable of non-destructively capturing the two-dimensional distribution of capacitance formed between an object and the sensor. This capability enables the visualization of minute surface irregularities of objects, the integrity of electrical connections in wiring, and the spatial distribution of dielectrics and conductors within insulating materials. Due to these distinct characteristics, various applications have been reported, including biometric authentication such as fingerprint recognition [1-4], observing temporal changes in fine particles like cells [5-8], and contact sensors for robots and medical devices [9].

In the fields of flat panel display (FPD) manufacturing and inspection, there are particularly high expectations for the application of these sensors in detecting the presence and precise location of defects in metal wiring [10]. Inspection cases for FPDs [11-12] have been reported, where capacitance image sensors are utilized to inspect thin-film transistor substrates, the fan-out wiring of peripheral circuits, and gate driver circuits. Furthermore, inspection cases for micro-LED displays [13] have demonstrated the ability to detect abnormal LEDs using these sensors. For such stringent applications, the system must possess both high capacitance detection precision to prevent inspection errors and high-speed detection capabilities. Consequently, the creation of high-precision and high-speed capacitance image sensors can contribute to accelerating the overall manufacturing process of displays by significantly improving inspection efficiency.

High detection accuracy below 100 zF has been achieved by noise-canceling techniques [14-16]. However, because of their long acquisition time, they are facing challenges in inspection efficiency and movie capturing.

This paper presents a newly developed proximity capacitance complementary metal-oxide-semiconductor (CMOS) image sensor that performs high-speed, high-precision capacitance detection in global shutter (GS) operation using noise cancellation. The sensor chip was fabricated by a 0.18 µm CMOS process technology. First, the basic circuit configuration and the high-precision capacitance detection principle are described. Next, the architecture and the operational timing of the developed high-speed GS sensor are explained in detail. Then, the measurement results of the fabricated chip are presented, demonstrating its basic characteristics as well as high-speed imaging capabilities. Finally, the conclusions are stated.

Circuit configuration and high-precision capacitance detection

Fig. 1 shows a schematic cross-sectional view of the sensor and the target object during capacitance detection. The proximity capacitance sensor detects the capacitance between top-layer metal of the sensor chip, used as the detection electrode, and the target object. For a conductor target, the object itself acts as the counter electrode and the input pulse is supplied directly, as shown in Fig. 1(a). The measurement capacitance (Cs) varies depending on the distance between the detection electrode and the target object. For a dielectric target, the flat conductor plate is used as the counter electrode and the input pulse is supplied to it as in Fig. 1(b). Cs varies depending on the dielectric constant and thickness of the measured object. For a target in liquid, the probe is used as the counter electrode as in Fig. 1(c). Cs varies depending on the presence or absence of the target object and the extent to which the target object covers the area directly above the detection electrode. Furthermore, it is possible to detect capacitance without external electrodes by supplying voltage from the guard ring within the sensor as in Fig. 1(d).

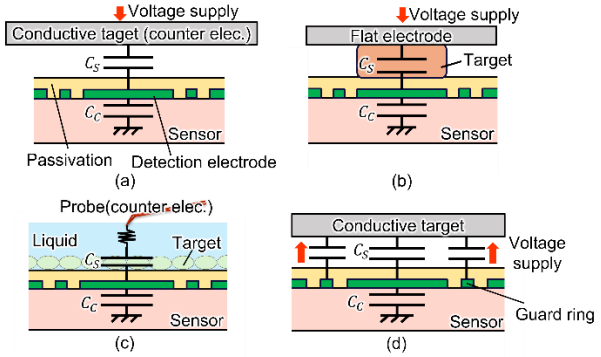
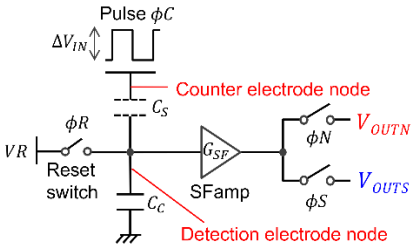


Fig.1 Schematic cross-sectional view of the proximity capacitance sensor and the target object during capacitance detection. (a) Conductor target. (b) Dielectric target. (c) Target in liquid. (d) Detection using an internal guard ring.

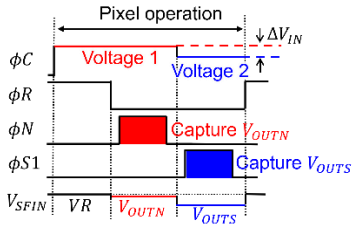
Fig. 2 shows the simplified sensor circuit schematic and operational timing diagram of the developed chip. The circuit contains a detection electrode capacitance (C_C). Two signals per frame are obtained: V_{OUTN}, which includes thermal noise and source follower (SF) threshold variations, and V_{OUTS}, which includes V_{OUTN} and a signal component determined by the ratio of C_S and C_C. The output, ΔV_{OUT} is obtained as follows,

$$\Delta V_{OUT} = V_{OUTN} - V_{OUTS} = \frac{C_S}{C_C + C_S} \times \Delta V_{IN} \times G_{SF} \qquad (1)$$

This correlated double sampling (CDS) operation cancels noise, such as SF threshold variations, and thermal noise, enabling high-precision capacitance detection.



(a) Simplified sensor circuit schematic



(b) Operational timing diagram

Fig. 2 Simplified sensor circuit schematic and operational timing diagram.

Developed high-speed global shutter proximity capacitance CMOS image sensor

Detecting small capacitances below aF requires a large ΔV_{IN} of several hundred volts in some cases. Consequently, a settling time of several microseconds is required to stabilize this external voltage pulse. Fig. 3 shows the operational timing diagrams for (a) a rolling shutter (RS) and (b) a GS. In a RS architecture (Fig. 3(a)), pixels are driven row by row, meaning this long settling time for the input pulse is required for every row. This accumulated settling time significantly slows down the overall frame rate. In contrast, a GS architecture (Fig. 3(b)) drives all pixels simultaneously. Thus, the external pulse is applied and allowed to settle only once per frame. Therefore, by implementing this GS operation, high-precision capacitance detection can be performed at a much higher speed. Achieving global shutter operation requires in-pixel memory, which increases the pixel size and consequently lowers the resolution.

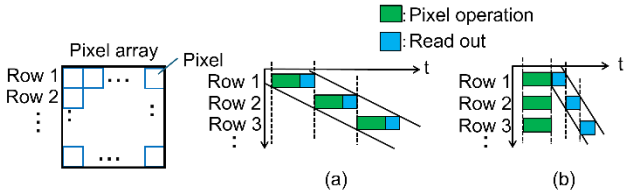


Fig. 3 Timing diagrams of the array type capacitance image sensors. (a) rolling shutter. (b) global shutter.

Fig. 4 shows the pixel circuit schematic of two pixels. To implement a GS, high-density Si trench capacitors [17-18] are integrated in each pixel, which serve as in-pixel memories for voltage signal storage [19-20]. The GS operation is achieved by driving all pixels simultaneously, temporarily storing the signals in the pixel memories, then reading out the stored signals row by row. By using the trench capacitors for the in-pixel memories, an increase in pixel size is minimized while thermal noise is suppressed, owing to the large capacitance provided. Furthermore, to achieve higher resolution, two pixels share three transistors (reset switch 2, source follower 2, and pixel select switch 2). In addition to its normal operation mode, the chip supports a burst mode [20-21] that acquires multiple frames with a single pixel operation. By turning switch B on, two pixels can be treated as one pixel, enabling burst imaging of up to five frames.

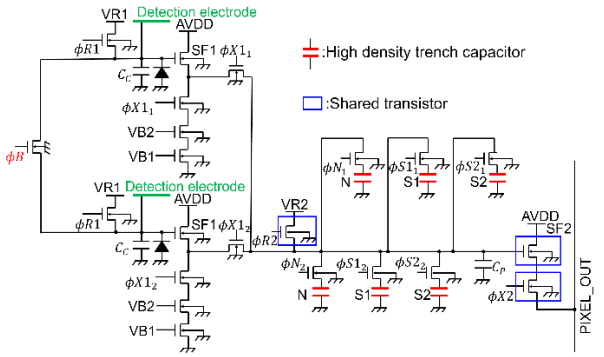


Fig. 4 The pixel circuit diagram of developed GS proximity capacitance sensor.

Fig. 5 shows the circuit block diagram of the chip. The read-out circuit consists of vertical and horizontal scan circuits, column parallel current sources, column parallel sample/hold (S/H) circuits, and output buffers. Furthermore, three S/H capacitors are implemented per column to enable the simultaneous readout of three signals.

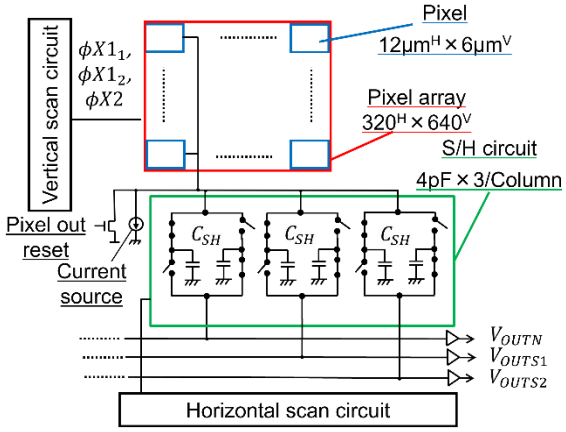


Fig.5 Circuit block diagram of the chip.

Fig. 6 shows the timing diagrams of (a) normal mode and (b) burst mode, respectively. In either mode, the chip drives the in-pixel operation pulses only once per frame, followed by sequential row-by-row readout. In normal mode, the signal is acquired by lowering the input pulse ΦC by ΔV_{IN} once per pixel operation. On the other hand, in burst mode, capacitance signals are continuously acquired with the same ΔV_{IN}. By utilizing six in-pixel memories, it is possible to acquire signals for up to five consecutive frames.

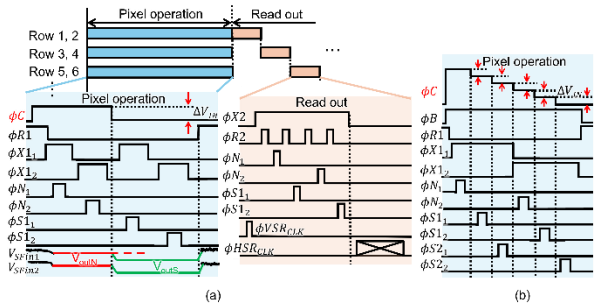


Fig. 6 The pulse timing diagrams of (a) normal mode and (b) burst mode.

Fig. 7 shows the micrograph of the chip, fabricated using a 0.18 µm, 1-polysilicon, 5-metal CMOS process technology. The chip has a die size of $4.8mm^{H} \times 4.8mm^{V}$, and $320^{H} \times 640^{V}$ pixels.

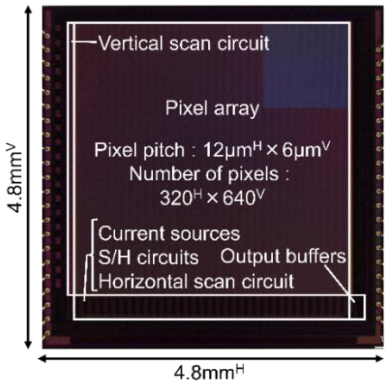


Fig. 7 The micrograph of the fabricated chip.

Chip measurement results

Fig. 8 shows the measurement system. It consists of a headboard with the fabricated sensor chip mounted face up, an analog front-end (AFE) board with voltage regulators and a 14 bit differential ADC, an FPGA board supplying operation pulse to the sensor chip, and a PC to receive digital signals.

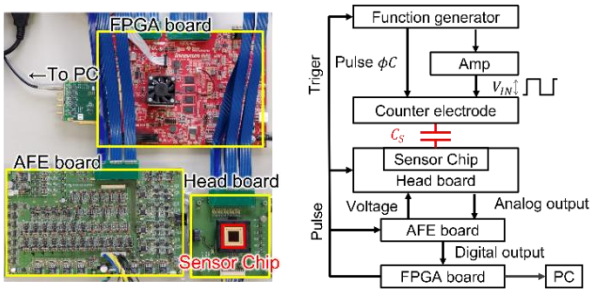


Fig. 8 The measurement system to measure the performance of the fabricated chip.

Fig. 9 plots the input-referred output voltage as a function of the input pulse voltage amplitude, ΔV_{IN}, for various target capacitances. Measurements were conducted under two conditions: in a conductive solution, and by varying the capacitance to a probe by gradually increasing the distance between the sensor surface and the probe tip. The results obtained with the conductive solution indicate the capacitance formed by the sensor's 1-µm-thick passivation layer, representing the maximum detectable capacitance of this chip. The colored dots represent the measured values, while the black straight lines indicate the theoretical characteristics for each capacitance value, calculated by the measured C_C of the chip. The blue dashed line indicates the random noise level of the sensor. The capacitance value where the signal equals the noise represents the minimum detectable capacitance for the input voltage. The output saturation observed in the results with the conductive solution is due to the signal exceeding the input range of the ADC. The results demonstrate good linearity of the output voltage with respect to the input voltage amplitude for capacitance values ranging from 1.5 fF down to 12 zF, indicating that accurate capacitance measurement has been achieved. Furthermore, a capacitance detection precision of 170 zF and 12 zF was obtained at a ΔV_{IN} of 20 V and 300 V, respectively.

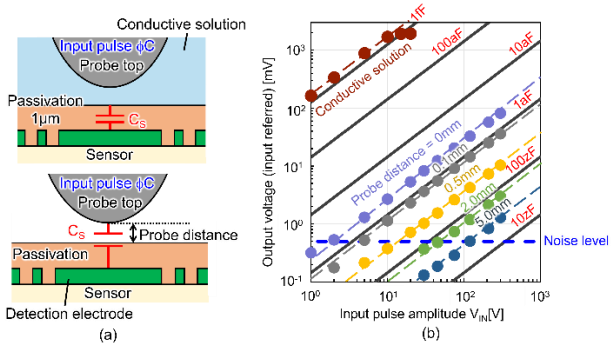


Fig. 9 The input-referred output voltage as a function of input voltage for various target capacitances of the fabricated chip.

Fig. 10(a) shows the schematic illustration of model for stainless steel. Capacitance imaging measures capacitance coupled with conductive particles as counter electrode. Fig. 10(b) shows a capacitance image of 50-150 µm diameter stainless steel particles captured by the fabricated chip. Fig. 10(c) shows six consecutive frames that were acquired while moving the particles with blowing air. These images are cropped to the $150^{H} \times 300^{V}$ pixel region indicated by the yellow square in Fig. 10(b). The imaging was performed at 90 fps. These images show that moving particles have been successfully captured without distortion due to its high-speed GS operation.

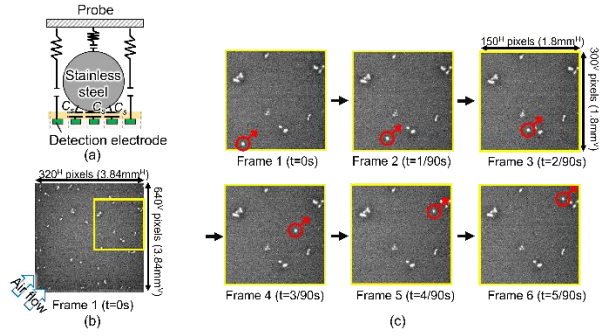


Fig. 10 (a) The capacitance imaging principle of stainless steel particle and (b) capacitance images of 50-150µm diameter stainless steel particles and (c) six consecutive frames while moving captured by the developed chip with 90 fps GS.

Fig. 11(a) shows a capacitance image of a conductive solution dropped onto the chip. This image is captured by turning switch B

on to treat two pixels as one, resulting in a 12 µm (H) × 12 µm (V) pixel grid arranged in a 320 (H) × 320 (V) pattern. Fig. 11(b) shows three consecutive frames captured in burst mode depicting the spread of the conductive solution. These images are cropped to the 160 (H) × 160 (V) pixel region indicated by the yellow square in Fig. 11(b).

In this burst mode operation, the signal component of the previous frame is used as the reference level for the subsequent frame. Therefore, the difference from the preceding frame is directly output for the second frame onwards. This operation provides the significant advantage of extracting only the changing components, which is highly effective for observing high-speed phenomena requiring kfps framerate or above. Consequently, in the second and third frames of Fig. 11(b), the areas where the conductive solution spread during the extremely short interval of approximately 6 µs are highlighted in white.

Furthermore, because each pixel integrates six in-pixel memories, the sensor architecture also supports a true three-frame burst mode with conventional CDS by acquiring the noise component between frames.

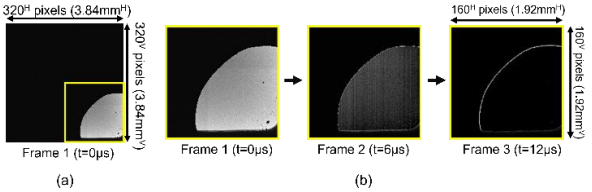


Fig. 11 Capacitance images of a conductive solution. (a) An image captured with 12 µm (H) × 12 µm (V) merged pixels. (b) Three consecutive frames captured in burst mode.

Table 1 summarizes the performance of the developed chip. The chip, capable of performing high-precision capacitance detection in GS operation by applying noise cancellation technology, achieved a high precision of 12 zF (ΔV_{IN}=300V) at 90 fps. Furthermore, it achieved high-speed capacitance detection at 167 kfps in burst mode.

Table 1 Performance summary of the developed chip.

# of Pixels	$320^H \times 640^V$ (Normal mode) $320^H \times 320^V$ (Burst mode)
Pixel Size	12 $\mu m^H \times 6\ \mu m^V$ (Normal mode) 12 $\mu m^H \times 12\ \mu m^V$ (Burst mode)
Sensor Type	Global shutter
Frame Rate	90 fps (Normal mode) 167k fps (Burst mode)
Saturation Signal	1.94 V (Input referred)
Random Noise (input referred)	501 μV_{rms}
Detection Precision	1.7×10^{-19} F (V_{IN}=20V) 1.2×10^{-20} F (V_{IN}=300V)

Fig. 12 shows the benchmarking of the developed proximity capacitance CMOS image sensors. The chip is the first to simultaneously achieve 90 fps and a high capacitance detection precision of 12 zF. In addition, it achieved an unprecedented high-speed capacitance detection of 167 kfps in burst mode.

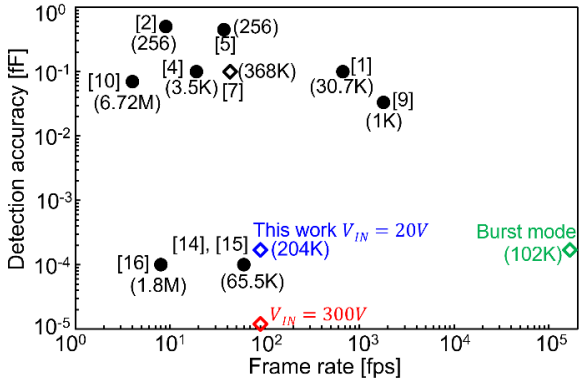


Fig. 12 Detection accuracy and frame rate for benchmarking with other sensors.

Conclusion

In this paper, a newly developed proximity capacitance CMOS image sensor featuring global shutter operation and noise cancellation technology was presented. The proposed chip was fabricated using a 0.18 µm CMOS process technology, and incorporates high-density Si trench capacitors as in-pixel memories. This architectural design effectively minimizes pixel size while enabling both normal and burst mode operations for high-speed capacitance detection.

The measurement results demonstrated the sensor's exceptional performance. It is the first sensor to simultaneously achieve a high frame rate of 90 fps and a high capacitance detection precision of 12 zF. Furthermore, by utilizing six in-pixel memories, the burst mode realized an unprecedented high-speed capacitance detection of 167 kfps. Experimental imaging successfully captured distortion-free capacitance images of moving stainless steel particles and the rapid microsecond-scale spread of conductive solutions, validating its high-speed and high-precision capabilities.

The developed chip is expected to be applied to high-precision and high-efficiency measurement instruments across a wide range of fields, including manufacturing and life sciences, and is anticipated to significantly contribute to the advancement of these fields.

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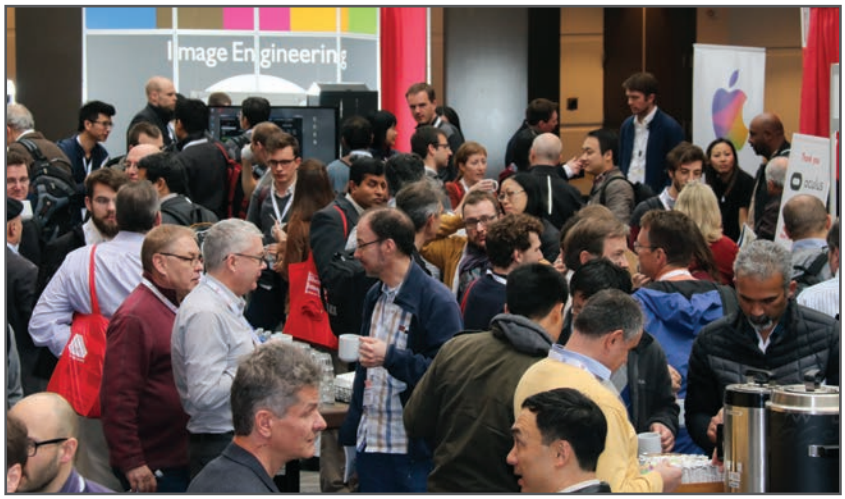

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