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# A 72-dB SNR 1K-fps Global Shutter CMOS Image Sensor with Dual Pixel Reset Voltage and Programmable Gain Amplifier

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## Abstract

*Absorption imaging using CMOS image sensors (CISs) enables non-invasive and non-destructive visualization and measurement of fluid concentration distributions. However, achieving high signal-to-noise ratio (SNR) under high illumination is challenging because large full well capacity (FWC) reduces conversion gain (CG) and increases input-referred noise. This work proposes a two-stage lateral overflow integration capacitor (LOFIC) CIS featuring dual pixel reset voltage (Dual VR) operation with an in-column programmable gain amplifier (PGA) and multi-sampling to suppress input-referred noise electron. The fabricated 140 × 140-pixel CIS achieved 130 dB dynamic range and 72.8 dB maximum SNR at 1000 fps. Imaging experiments demonstrated clear visualization of minute concentration variations, indicating suitability for high-speed absorption applications including in-chamber gas monitoring.*

## Introduction

With the rapid advancement of artificial intelligence (AI), data-driven optimization has become increasingly important across a wide range of fields, including manufacturing, agriculture, and healthcare, where data acquired from sensors are analyzed and fed back to process conditions and system operations. Within this trend towards smart systems, next-generation Internet of Things (IoT) sensing technologies are strongly demanded to visualize two-dimensional concentration distributions of fluids, such as gases and liquids, in dynamic environments using non-invasive and non-destructive approaches that do not disturb the target.

A representative application is monitoring gas concentration distributions inside semiconductor process chambers. In high-precision processes such as atomic layer deposition (ALD), gas distribution and reaction uniformity strongly affect process reproducibility and yield. Therefore, real-time visualization and measurement of concentration distributions is highly desirable.

For visualization of fluid concentration distributions, contact-based sensors such as catalytic combustion sensors [1] and electrochemical current-measurement sensors [2] are not well suited to two-dimensional or three-dimensional measurements through array integration. In contrast, optical absorption methods are compatible with array-based implementation and enable non-invasive visualization of concentration distributions. Representative approaches include tunable diode laser absorption spectroscopy (TDLAS) with tomographic reconstruction [3] and absorption imaging using CMOS image sensors (CISs), which has demonstrated gas concentration visualization inside semiconductor process chambers [4–6]. These methods are based on the Beer–Lambert law, which derives concentration from attenuation of transmitted light intensity.

Absorption-based imaging of fluid concentration distributions imposes several stringent requirements. First, to capture rapidly moving targets such as gases inside semiconductor process chambers without distortion, high-speed operation and global shutter (GS) functionality are indispensable. To distinguish concentrations of individual species in mixed gases or multicomponent liquids, illumination with light sources of different absorption wavelengths must be switched. In such cases, precise synchronization between exposure timing and illumination is required, making GS operation—where all pixels are exposed simultaneously—particularly effective for absorption imaging. Second, sensitivity over a wide wavelength range, including ultraviolet (UV), visible, and near-infrared (NIR) regions, is required to accommodate the diverse optical absorption characteristics of various materials. In particular, many molecules involved in semiconductor and chemical processes exhibit strong absorption in the UV region, which requires image sensors with a broadband spectral response. Third, under these conditions, extremely high signal-to-noise ratio (SNR) is required to accurately detect small absorption-induced signal variations.

As shown in (1), increasing the incident light intensity improves the SNR. In addition, a large full well capacity (FWC) enables a higher maximum achievable SNR by allowing a larger number of accumulated signal electrons before saturation.

$$\mathrm{SNR\,[dB]} = 20\log\left(\frac{N_{sig}}{\sqrt{\left(\sqrt{N_{sig}}\right)^2 + n_{sys}^2}}\right) \quad (1)$$

where $N_{sig}$ is the number of signal electrons and $n_{sys}$ is the input-referred system noise in electrons. Here, the square root of $N_{sig}$ represents the photon shot noise component.

Several techniques have been reported to increase the FWC of CISs. One approach employs multiple conversion gain schemes [7], which utilize multiple FD nodes. This approach is ultimately limited by the saturation charge of the photodiode (PD). Another approach expands the FWC by using non-silicon materials for the PD [8]. However, these methods inherently suffer from fundamental limitations, as the achievable FWC is constrained by the PD or FD. In contrast, the lateral overflow integration capacitor (LOFIC) architecture [9,10] stores the overflow charge from the photodiode (PD) in an in-pixel capacitor, enabling the storage capacitance to be designed independently of the PD and FD while providing a wide linear response range. By designing a large storage capacitance, LOFIC can significantly extend the FWC and achieve a high SNR, making it well suited for absorption imaging applications.

On the other hand, increasing the storage capacitance in LOFIC reduces the charge-to-voltage conversion gain (CG), which in turn increases the input-referred noise ($n_{sys}$) associated with voltage-domain noise from the readout circuitry. As a result, the improvement in SNR due to increased storage capacity eventually saturates, making it difficult to detect small absorption changes in high-illumination conditions. Therefore, in order to maximize the

SNR in absorption imaging, circuit techniques that reduce readout-circuit-induced noise are required in addition to expanding the FWC.

In this work, we improve the maximum achievable SNR under high-illumination conditions by suppressing the impact of voltage-domain noise originating from downstream readout circuits through a combination of a previously reported dual pixel reset voltage (Dual VR) scheme [11] and a programmable gain amplifier (PGA). This approach enables more accurate visualization of fluid concentration distributions using absorption imaging.

## Developed CIS

### *Objective*

The objective of this work is to achieve both an SNR exceeding 70-dB and a high frame rate of 1000-fps simultaneously, a performance combination that has not been previously reported for GS CISs. To achieve an SNR over 70 dB, a Dual VR [11] operation combined with PGA and a multi-sampling scheme [12] is introduced. These techniques suppress input-referred noise components, thereby improving the SNR. To achieve 1000 fps operation, a pipelined sample-and-hold (S/H) architecture is adopted.

### *Architecture of the developed CIS*

Figure 1 shows the pixel circuit of the CIS developed in this study. The pixel consists of a two-stage LOFIC structure [10], a voltage-domain memory bank for GS operation [4], and a UV-sensitive PD [13]. The capacitance values of LOFIC1 and LOFIC2 are 91.6 fF and 3.14 pF, respectively, and the high-sensitivity signal (S1), high-saturation signal (S2), and highest-saturation signal (S3) are obtained from FD, FD+LOFIC1, and FD+LOFIC1+LOFIC2, respectively. In addition, trench capacitor technology [14] is applied to the capacitors used for the LOFIC and the GS memory bank in order to reduce the pixel area. In this CIS, a Dual VR configuration is adopted, in which two reset voltages (VR1a and VR1b) can be supplied to the PD, and LOFIC by switching the control pulse φVR.

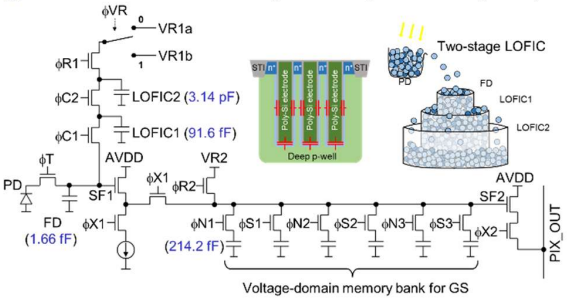


***Figure 1.*** *Pixel circuit diagram of the developed CIS.*

Figure 2 shows the block diagram of the developed chip. A PGA, shown in Figure 3, is placed only on the S3 signal path to amplify small signal differences under high-illumination conditions and to suppress the influence of downstream noise. The PGA used in this study adopts a configuration in which the closed-loop gain is determined by the ratio of the feedback capacitance $C_f$ to the coupling capacitance $C_c$. By implementing $C_f$ as a variable capacitor, the gain can be adjusted from 2× to 16×.

Furthermore, two sets of sample-and-hold (S/H) capacitors are implemented in a pipeline configuration for each of the S1–S3 signal paths. By pipelining the S/H capacitors, the operation of reading the signal of the n-th row to the HLINE and the operation of writing the signal of the n-th row to the HLINE and the operation of writing the signal of the (n+1)-th row from the VLINE to the S/H capacitors can be performed in parallel. This allows the driving frequency to be suppressed while ensuring sufficient settling time, thereby achieving high-frame-rate operation of up to 1000 fps.

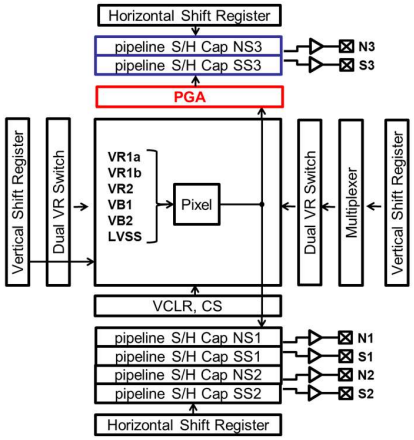


***Figure 2.*** *Chip block diagram of the developed CIS.*

### *Dual VR with PGA operation: Principle*

The principle of a Dual VR with PGA operation is shown in Figure 3. This operation is a technique that achieves both improved saturation characteristics under high-illumination conditions and high resolution w・尾 for small signal variations by employing two pixel reset voltages. Specifically, a high reset voltage is used during pixel reset to increase the saturation electron number, while a voltage near saturation is used for the reference signal, enabling small signal differences to be amplified by gain and converted by analog-to-digital conversion (ADC). As a result, high-resolution signal readout is achieved even in high-illumination regions. In addition, by setting the pixel reset voltage that does not need to be read out to a value sufficiently high to exceed the linear range of the source follower (SF), the saturation electron number of the pixel can be further increased, which is another feature of the Dual VR operation [11].

However, in previously reported Dual VR operations, signal amplification was performed off-chip immediately before AD conversion, making it impossible to reduce noise generated inside the chip. In contrast, this study adopts a configuration in which signal amplification is performed within the column circuits. With this configuration, noise generated after the column circuits can be reduced, and improvement in SNR is expected. Furthermore, since the WDR operation uses a two-stage LOFIC, three-pixel output signals and three pixel reset signals are required, resulting in a total of six in-pixel sampling operations. On the other hand, Dual VR with PGA operation is intended for use under high-illumination conditions, and therefore the readout targets are limited to two signals: the S3 signal and the reset signal N3.

Accordingly, this study introduces a multi-sampling operation [12], in which the S3 signal and the N3 signal are each sampled three times within the pixel. This reduces 1/f noise originating from SF1 as well as kTC noise generated during sampling of signals into the in-pixel analog memory. By combining the Dual VR with PGA operation and the multi-sampling operation, further improvement in SNR is expected.

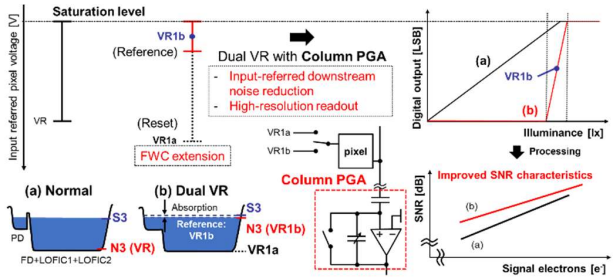


***Figure 3.*** *Principle of Dual VR with PGA operation.*

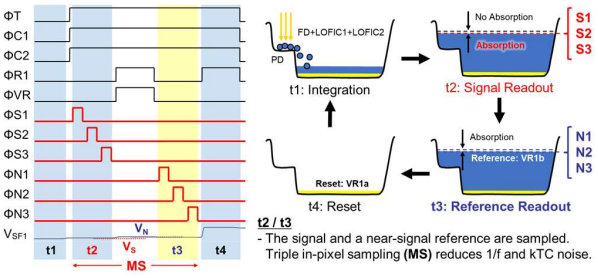


***Figure 4.*** *Timing diagram of the pixel driving for Dual VR with PGA operation.*

## *Dual VR with PGA operation: Timing diagram*

Figure 4 shows the timing diagram of the pixel driving period. At t1, the signal voltage accumulated in FD+LOFIC1+LOFIC2 through exposure after reset by VR1a in the previous frame is written to the GS S1-S3 memory. At t2, VR1b, which is set near the saturation voltage, is applied to FD+LOFIC1+LOFIC2, and at t3, this voltage is written to the GS N1-N3 memory as a reference signal. At t4, the pixel is reset by VR1a, and exposure for the next frame starts.

Figure 5 shows the timing diagram of the signal readout period in the Dual VR with PGA operation. At t1, the VLINE and the S/H capacitors are reset to remove residual charge. At t2, the amplifier is activated and an auto-zero (AZ) operation is performed to establish the reference state of the PGA, while forming a charge state in the coupling capacitor $C_c$ corresponding to the difference between the reference voltage $V_{refAMP}$ and the reference signal voltage ($V_{N3}$) written to the GS N1-N3 memory. At t3, the AZ operation is released, and the immediate PGA output is sampled and held as a reset signal (Reset/AZ sample) expressed by (2). This enables cancellation of the effect of charge injection $\Delta V_{CI}$ caused by the AZ switch in the subsequent processing.

$$V_{\mathrm{Reset}} = V_{\mathrm{refAMP}} + \Delta V_{\mathrm{CI}} \tag{2}$$

At t4, the S3 output voltage ($V_{S3}$) written to the GS S1-S3 memory is connected to the PGA input. Due to the virtual short of the operational amplifier, charge corresponding to the voltage difference $V_{N3} - V_{S3}$ is transferred from $C_c$ to $C_f$, and an output in which the voltage difference is amplified by the capacitance ratio $C_c/C_f$ is obtained. This output is sampled and held as the signal sample expressed by (3). By taking the difference from the reference sample, offset and switching-induced components are removed, and a small change in the pixel voltage relative to $V_{N3}$ is read out with high resolution.

$$V_{\mathrm{Sig}} = V_{\mathrm{refAMP}} + \Delta V_{\mathrm{CI}} + \frac{C_c}{C_f}(V_{\mathrm{N3}} - V_{\mathrm{S3}}) \tag{3}$$

Finally, by taking the difference between the reference sample $V_{Reset}$ and the signal sample $V_{Sig}$ in the readout stage, charge injection and offset components are canceled, enabling high-resolution readout of small changes in the pixel voltage. As a result, small fluid concentration changes can be detected in high-SNR regions, and when the gain is set to G, the influence of voltage-domain noise from downstream stages after the PGA can be reduced by a factor of 1/G.

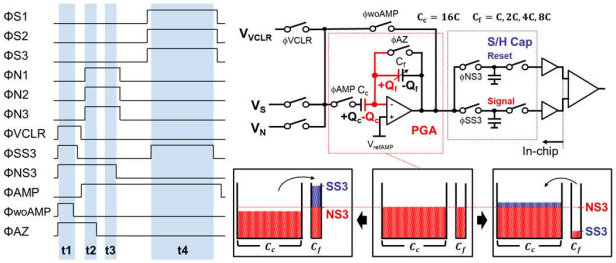


***Figure 5.*** *Timing diagram of the signal readout for Dual VR with PGA operation.*

## Chip measurement results

Figure 6 shows a photograph of the fabricated CIS chip. The chip was fabricated using a 0.18-µm CMOS process technology with 1-poly and 5-metal layers. The supply voltage is 3.3 V. The die size is 4.8 mm × 4.8 mm, and the pixel array occupied an area of 3,136 µm × 3,136 µm. The pixel pitch is 22.4 µm × 22.4 µm, comprising 140 × 140 pixels.

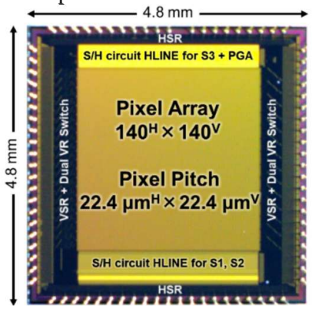


***Figure 6.*** *Micrograph of the developed CIS chip.*

Figure 7 shows the photoelectric conversion characteristics of the three output signals from the two-stage LOFIC pixel, as well as those obtained under Dual VR with PGA operation with a gain of 16× for the S3 signal. The horizontal axis represents relative light illuminance, and the vertical axis represents the input-referred signal voltage. A dynamic range of 128 dB was achieved under single-exposure GS operation, and 130 dB was achieved under Dual VR with PGA operation. All three signals exhibited good linearity.

Figure 8(a) shows the SNR characteristics under WDR operation and Dual VR with PGA operation with a gain of 16×. The horizontal axis represents relative light illuminance, and the vertical

axis represents SNR. Under WDR operation corresponding to 1000 fps, the maximum SNRs were 42.8 dB for S1, 59.3 dB for S2, and 67.3 dB for S3. The SNRs at the switching points between S1/S2 and S2/S3 were 28.5 dB and 39.5 dB, respectively. Furthermore, under Dual VR with PGA operation with 16× gain and multi-sampling at an equivalent frame rate of 1000 fps, an SNR of 72.8 dB was obtained. These results confirmed that high-speed operation could be maintained without SNR degradation. The characteristics under Dual VR with PGA operation were obtained by sweeping VR1b, and the corresponding valid range is indicated in Figure 8(a). Figure 8(b) shows the trade-off between amplifier input range and maximum SNR for different PGA gains. Increasing the PGA gain improves the maximum SNR by suppressing the influence of downstream noise, whereas the input-referred amplifier range becomes narrower. Therefore, the PGA gain should be optimized according to the target signal range and application.

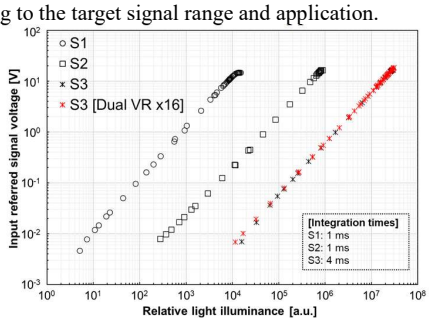


***Figure 7.*** *Photoelectric conversion characteristics under WDR and Dual VR with PGA operations.*

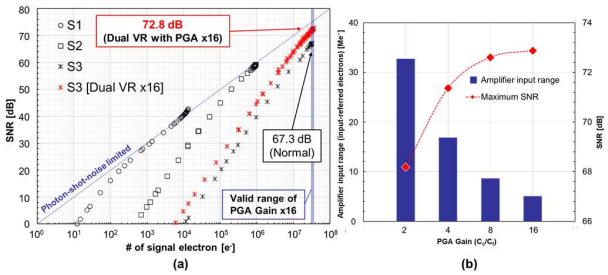


***Figure 8.*** *(a) SNR characteristics under WDR and Dual VR with PGA operations. (b) Trade-off between amplifier input range (blue bars, left axis) and maximum SNR (red dashed line, right axis) at different PGA gains.*

Figure 9 shows the measured spectral sensitivity characteristics. By employing Si PD technology with a high-concentration surface $p^+$ layer having a steep dopant concentration profile, high QE was achieved in the UV wavelength band in addition to the NIR region.

Figure 10 shows imaging examples under 500-fps WDR operation with three output signals. Figure 10(a) shows the imaging setup, including printed letters, two stuffed toys, and a rotating printed sheet. The left stuffed toy was placed inside a dark box to create a low-illumination region. High-intensity light was irradiated onto the printed letters near the upper-right side, and part of the light also illuminated the upper-left stuffed toy. Figure 10(b) shows five consecutive output frames. The S1 signal captured the stuffed toy inside the dark box under low-illumination conditions. In bright regions, S1 appears blacked out because of the operating principle of the two-stage LOFIC structure. The S2 signal captured the upper-left stuffed toy and the rotating printed sheet under high illumination.

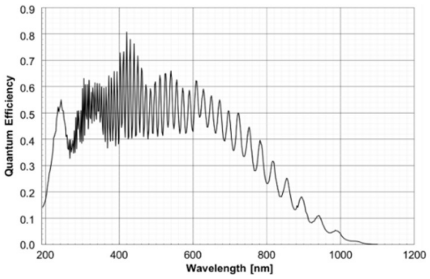


***Figure 9.*** *Spectral sensitivity characteristics.*

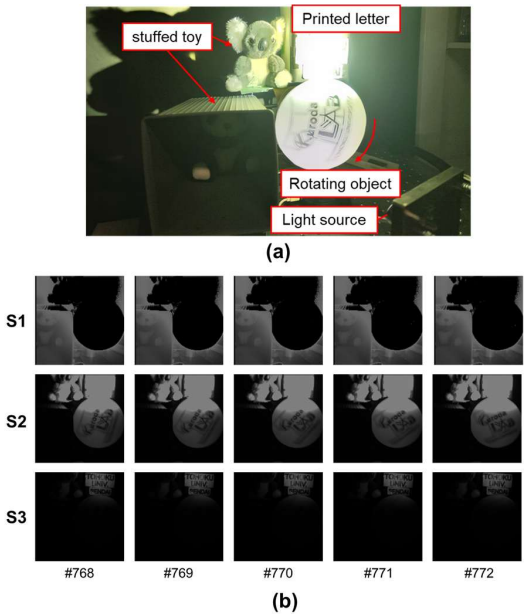


***Figure 10.*** *Imaging examples under WDR operation captured at 500 fps. (a) Photograph of the imaging setup. (b) Consecutive output images.*

Since the CIS operated in GS mode, no rolling-shutter distortion was observed in the rotating printed sheet. The S3 signal captured the printed letters near the light source under extremely high illumination. These results demonstrate the single-exposure WDR performance of the proposed CIS.

Figure 11 shows the experimental setup used for absorption imaging inside the chamber. A camera module equipped with a telecentric lens was used to observe the chamber interior under illumination from a UV light source. During the measurement, the chamber pressure was set to 10 Torr (1333 Pa), and the gas was switched from Ar at 20 sccm to $NO_2$ at 20 sccm. Figure 12 shows the corresponding absorption imaging results. The results obtained under two operation conditions are compared: (a) normal two-stage LOFIC operation without PGA and (b) Dual VR with PGA operation with a gain of 8. The images were acquired at 1000 fps. The displayed images correspond to magnified views of the highlighted region near the gas injection area. Compared with the normal operation without PGA, the proposed Dual VR with PGA operation provides clearer visualization of the structure near the gas injection region.

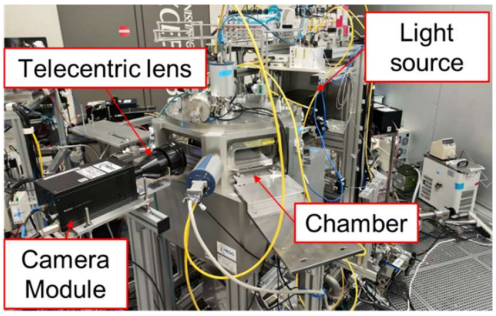


***Figure 11.*** *Experimental setup for absorption imaging inside the chamber.*

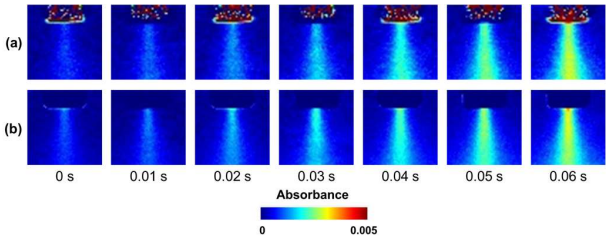


***Figure 12.*** *Absorption imaging results inside the chamber obtained under (a) Normal two-stage LOFIC operation without PGA and (b) Dual VR with PGA 8× gain operation.*

Table 1 summarizes the performance of the developed CIS. By introducing Dual VR with PGA operation, the input-referred noise from downstream circuits was reduced, enabling 72.8 dB SNR at 1000 fps. Figure 13 benchmarks this result against prior CISs, highlighting the proposed sensor's competitive high-speed, high-SNR performance for detecting minute absorption variations.

**Table 1: Performance summary of the developed CIS**

| | | |
|---|---|---|
| Process technology | | 0.18μm 1-poly-Si 5-Metal CMOS with pinned PD |
| Power supply voltage | | 3.3 V |
| Chip size | | $4.8mm^{H} \times 4.8mm^{V}$ |
| # of effective pixels | | $140^{H} \times 140^{V}$ |
| Pixel size | | $22.4\mu m^{H} \times 22.4\mu m^{V}$ |
| Fill factor | | 41% |
| Shutter operation | | Global Shutter |
| Maximum frame rate | | 1000 fps |
| CG | S1 | 96.8 μV/$e^{-}$ |
| | S2 | 1.75 μV/$e^{-}$ |
| | S3 | 51.0 nV/$e^{-}$ |
| FWC | S1 | 12.9 k$e^{-}$ |
| | S2 | 936 k$e^{-}$ |
| | S3 | 32.3 M$e^{-}$ |
| | S3 (@Dual VR with PGA) | 36.3 M$e^{-}$ |
| SNR | S1/S2 | 28.5 dB |
| | S2/S3 | 39.5 dB |
| | Maximum S3 (@Dual VR with PGA) | 72.8 dB (PGA 16× gain) |
| Dynamic range (@Dual VR with PGA) | | 128 dB<br>130 dB (PGA 16× gain) |

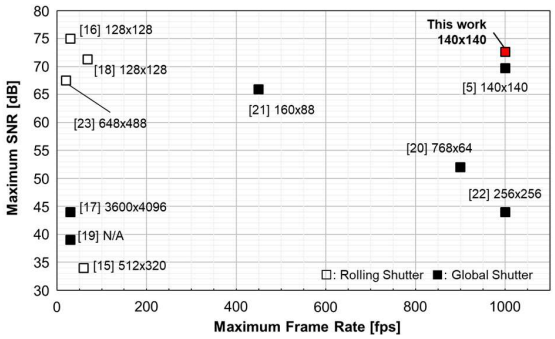


***Figure 13.*** *Comparison of maximum SNR vs maximum frame rate for previously reported CIS.*

## Conclusion

In this study, a CIS incorporating a Dual VR with PGA operation was developed for absorption-based visualization and measurement of fluid concentration distributions. By employing a two-stage LOFIC architecture, wide dynamic range was achieved, and by placing the PGA within the column circuits, the impact of voltage-domain noise originating from downstream readout circuitry was reduced. The fabricated CIS achieved a dynamic range of 130 dB under single-exposure GS operation. Under high-speed operation equivalent to 1000 fps, a maximum SNR of 72.8 dB was obtained by combining Dual VR with PGA operation with multi-sampling. Furthermore, imaging experiments of fluid concentration distributions demonstrated that minute concentration variations could be visualized with high precision using Dual VR with PGA operation. The proposed approach is considered effective for high-speed and high-precision absorption imaging applications, such as gas concentration monitoring inside semiconductor process chambers.

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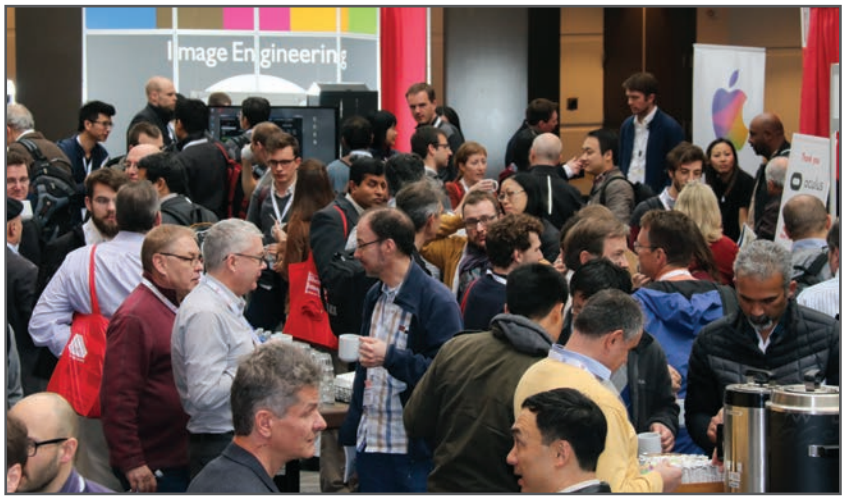



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