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An Asynchronous Time-Based Image Sensor with a Photovoltaic Receptor

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Abstract

Asynchronous Time-Based Image Sensors (ATIS) jointly perform event-driven temporal contrast detection and local exposure measurement, reducing throughput by reporting only relevant information with high temporal resolution. We introduce PVATIS, a new pixel front-end that replaces the conventional pair of reverse-biased photodiodes plus a logarithmic receptor with a single diode operated in photovoltaic mode. In open-circuit, this diode simultaneously serves as the photodetector and provides logarithmic compression in a self-biased configuration. The approach directly tackles pixel-level constraints, such as pixel pitch, noise, and energy, while trading off bandwidth due to increased integrated capacitance. PVATIS is therefore a strong candidate for high-resolution, HDR, low-noise, and energy-efficient operation, particularly suitable for 3D-stacked implementations and moderate-speed imaging.

Introduction

Dynamic Vision Sensors (DVS) [1] detect local temporal contrast asynchronously, emitting events only when brightness changes occur at the pixel level, which sharply reduces redundant data versus frame-based cameras and enables low-latency, low-power vision. This architecture makes them particularly suitable for fast, energy-efficient vision applications. Over the last decade, adoption has broadened from space [2] to infrared sensing [3] thanks to high temporal resolution and robustness, especially when combined with event-based processing pipelines, expanding their use in security, aerospace, and industrial applications [4, 5, 6]. Nonetheless, practical limitations persist: pixel-pitch pressure, noise/power trade-offs, and readout format constraints [7].

To make them more attractive, hybrid approaches that couple event sensing with exposure readout have emerged: the Asynchronous Time-Based Image Sensor (ATIS) [8] integrates time-based exposure measurement (minimizing data throughput by reporting only relevant information in a stream of events), while the Dynamic and Active Pixel Vision Sensor (DAVIS) [9] co-integrates DVS with APS, the latter favored industrially due to compatibility with synchronous APS readout streams [10].

Renewed interest in event-stream algorithms [7] further strengthens the case for ATIS-style architectures, yet classical ATIS pixels still rely on two reverse-biased photodiodes and a log receptor, which costs area and power and can limit scalability. These factors prevent organizations from fully exploiting its potential advantages.

Building on our previous work on the Photovoltaic DVS [11], we propose PVATIS, which simplifies ATIS by employing a shared photovoltaic diode for both stages. In an open-circuit configuration, the diode produces a voltage logarithmically dependent on the photocurrent, enabling both photodetection and logarithmic compression within a single self-biased device. This modification is fully compatible with temporal contrast detection, requiring only adaptations in subsequent circuitry to accommodate typical open-circuit voltages ($[0, 500]$ mV) [12]. While the PVATIS exposure measurement inherits principles from the original concept, it introduces novel design considerations and challenges, which are detailed in the following sections. The resulting Photovoltaic Asynchronous Time-Based Image Sensor (PVATIS) offers a promising pathway toward reducing pixel pitch, lowering noise, and improving energy efficiency.

Sensor's Implementation

In this section, a complete description of the sensor's implementation is presented, studying the PVATIS architecture and functionality of the three different supported modes: temporal contrast detection (PVDVS Mode), exposure measurement (PVTTS Mode), and a combination of both providing light intensity information of the region of interest (Dual Mode).

Diode operating in Photovoltaic regime

Fig. 1 illustrates the diode operation in the photovoltaic regime [12]; the family of curves at the right shows that quasi-static $I_D - V_D$ characteristics change with the illumination level. The diode current, $I_D = I_{GR} - I_{DIFF}$ combines a generation-recombination term I_{GR} (including photocurrent I_{PH} and the dark current I_{DARK}) and a diffusion component, $I_{DIFF} = I_S\left[\exp\left(V_D/\eta U_T\right) - 1\right]$, with I_S and η being the specific current and emission coefficient of the diode, respectively, and U_T, the thermal voltage. In this photovoltaic mode, the diode can operate as a solar cell harvesting luminous energy to power a load connected to the anode [13]. Under short-circuit, the maximum deliverable current for this application is the short-circuit current, I_{SC}. Alternatively, under open circuit, the dc current is null and the diode develops an illumination-dependent open-circuit voltage,

$$V_{oc} = \eta U_T \ln\left(1 + \frac{I_{GR}}{I_S}\right) \approx \eta U_T \ln\left(1 + \frac{I_{PH}}{I_S}\right) \tag{1}$$

which yields a logarithmic response versus photocurrent – see Fig. 1. Consequently, V_{oc} provides the same functional role as the ATIS logarithmic receptor [8], but saving 4 transistors. The diode's sensitivity to illumination variations is higher with low

illuminance since the slope of the V_{oc} curve is higher for low photocurrent values.

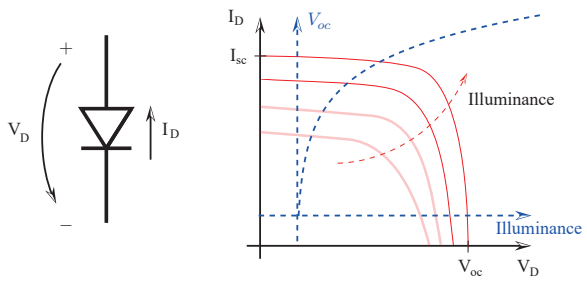

Figure 1. *I-V curves of a diode operating in photovoltaic regime and the dependence of the open-circuit voltage with illuminance.*

Conventional continuous-time logarithmic sensors typically require two separate devices for light-to-current conversion and current-to-voltage transformation, often introducing fixed-pattern noise that cannot be mitigated by correlated double sampling [14, 15]. By contrast, the photovoltaic mode performs both operations in a single device, reducing non-uniformity and static power consumption. Prior works demonstrate photovoltaic detectors achieving HDR imaging across visible and infrared spectra, as well as successful DVS implementations [16, 17, 11, 18]. Benefits include reduced area, lower noise, accurate dark reference, high sensitivity, and absence of image lag.

Pixel Architecture and Operating Modes

PVATIS employs one shared photovoltaic receptor that simultaneously feeds a photovoltaic DVS (PVDVS) path for temporal contrast and a photovoltaic TTS (PVTTS) path for exposure measurement (Fig. 2). This approach saves a total of 5 transistors ($4+1$ from removing the Change Detection stage's logarithmic receptor and the PWM's reset transistor, respectively) plus a photodiode.

The change detection front-end buffers V_{oc} (PMOS Source Follower), amplifies its variations (Change Amplifier), and encodes the polarity via a comparator. The exposure measurement front-end compares V_{oc} against a globally distributed ramp across the array, thereby encoding light intensity as a function of time. Hence, the proposed pixel architecture enables the sensor to operate in three different modes:

- **Temporal Contrast Detection Mode:** asynchronous events describing scene updates. This functionality is performed by default, independently of the exposure measurement circuit, and responds to the temporal contrast of V_{oc} unless externally stopped by activating a reset of the periphery.
- **Exposure Measurement Mode:** by activating the control signal TTS_ON, the PVTTS operates, and the entire array is read out independently of the PVDVS. This enables an exposure measurement of the whole scene at a desired time instant.
- **Dual Mode:** by disabling TTS_ON and enabling the PVTTS periphery, exposure measurements are locally triggered by confirmed contrast events in a region of interest.

  To limit background-activity noise, an exposure readout is started only if two neighboring pixels detect change concurrently ($2\times DVS\_RST$ is triggered); if activity continues ($2\times DVS\_REQ$ is turned on), the system aborts and defers the measurement until the final event settles.

For infrared applications, this translates into reporting motion/flow via PVDVS, plus average temperature within changing regions (Dual) or a scene-wide temperature snapshot (Exposure mode). Note that, the positive-slope ramp means dimmer pixels are reported earlier than brighter ones, which is advantageous under low light.

Top-Level Block Diagram and AER Readout

The top-level architecture is shown in Fig. 3. A 128×128 PVATIS-pixel array is connected to peripheral circuitry implementing the Address-Event Representation (AER) protocol [19]. Events are serialized through two-stage arbitration: within rows, then columns. Winning pixel addresses are encoded and asynchronously transmitted on a shared bus with a four-phase handshake (request, acknowledge, reset, idle).

In this case, two peripheries, one for each pixel stage, are required to perform the Dual Mode operation, as both change detection and exposure measurement are carried out simultaneously. Each periphery outputs a data package $\{x,y,t\}$, providing the address of the pixels that detect relevant information and the time instant of their readout. Note that depending on the information required, the dynamic power consumption can be regulated, as any periphery can be disabled using a global reset whenever only partial information is needed.

Experimental Results

In this section, some experimental results obtained from pixel- and matrix-level characterizations are presented. They demonstrate the proper operation of the sensor, validating the functionality of the three different modes PVATIS supports.

The experimental evaluation, illustrated in Fig. 4, was performed using a custom-designed PCB that integrates the fabricated sensor with an OpalKelly FPGA board for system control and data acquisition. To enable the Dual Mode, which simultaneously delivers temporal contrast detection and exposure measurement, an AERmini2 board was employed for the former functionality, while the FPGA handled the latter. A lens was positioned above the sensor to provide direct exposure to visual stimuli. The experiments took place in a dark room, ensuring controlled illumination conditions. For functional validation, however, the sensor was placed in front of a monitor displaying video sequences, allowing realistic and dynamic scenes to be projected onto the pixel array. This setup supported fast evaluation of the different operating modes and offered a straightforward means of assessing image reconstruction performance.

Functional Characterization Results

The functional characterization confirms the targeted operation. This evaluation specifically examines whether the three operating modes of PVATIS implemented in our chip behave as intended, ensuring that the event-based architectures accurately perform:

- temporal contrast detection,

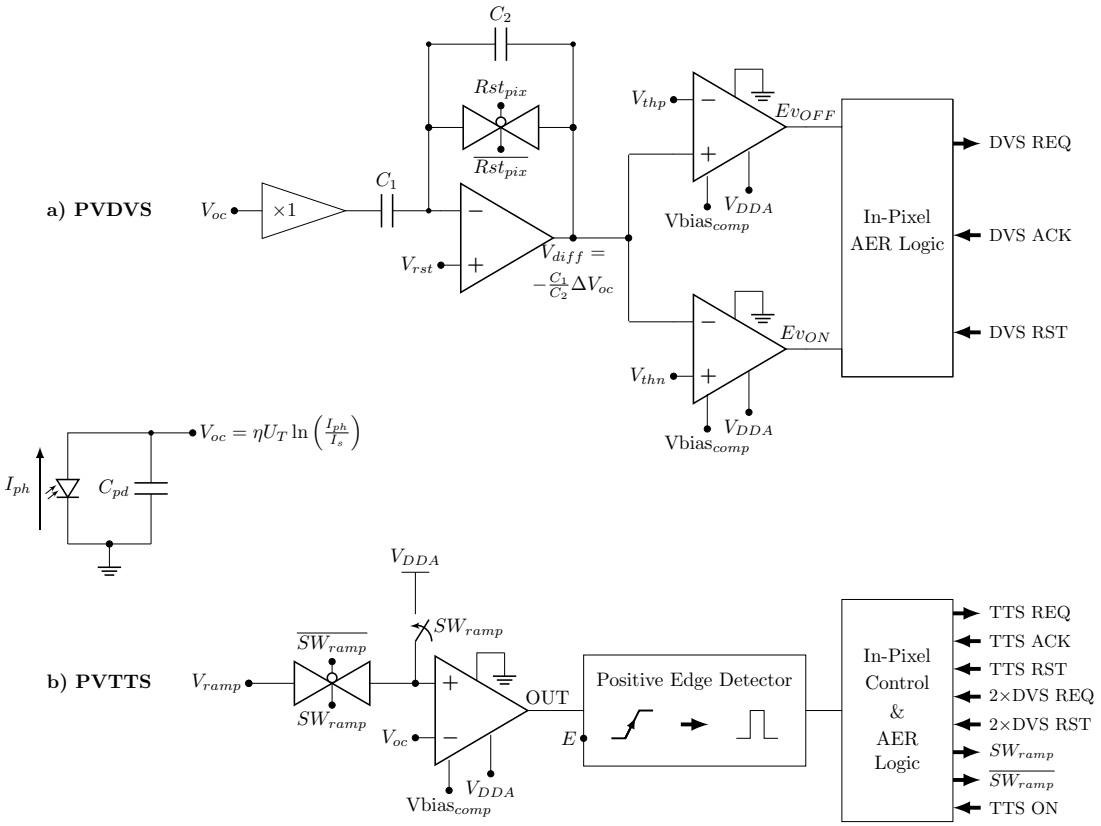

Figure 2. *Simplified PVATIS pixel: shared photovoltaic receptor driving a) PVDVS and b) PVTTS. Dual-mode operation uses dedicated peripheries that output $\{x, y, t\}$ – addresses and timestamps of relevant events. Dynamic power can be tuned by disabling unused peripheries.*

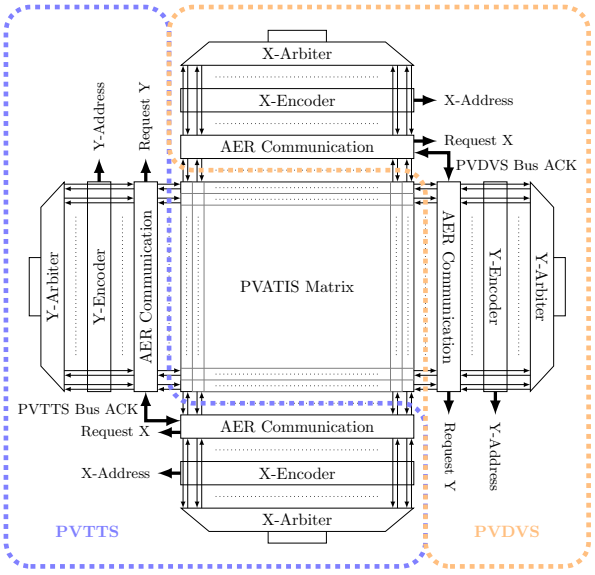

Figure 3. *Top-level block diagram of the PVATIS sensor. A 128×128 PVATIS-pixel array is connected to the peripheral blocks for AER communication protocol on the chip, with separate paths for PVDVS and PVTTS*

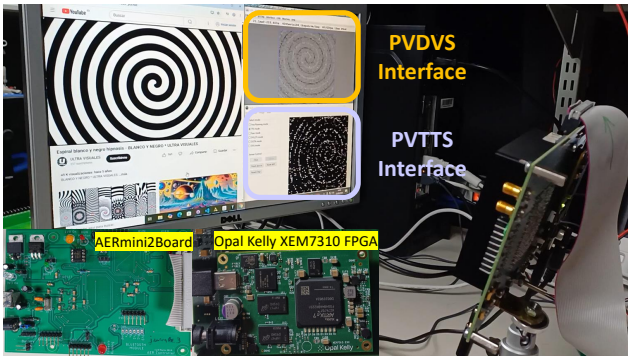

Figure 4. *Experimental Set-Up. Two different interfaces are used to represent temporal contrast detection and exposure measurement simultaneously. It demonstrates the correct operation of the Dual Mode.*

- exposure measurement of the entire scene and
- light intensity estimation within the region of interest.

Because the chip integrates full pixel matrices with photodiodes rather than relying on test inputs, it can be functionality validated directly through scene reconstruction using the sensor outputs. This strategy enables direct evaluation of the circuits' practical limitations and trade-offs under realistic scenarios. Besides that,

dedicated test structures provide more detailed measurements of circuit performance under controlled conditions, with results presented in the following section.

To illustrate functionality, several images captured by PVATIS are included. The PVTTS path achieves high dynamic range via logarithmic compression (Fig. 5) and naturally handles large intra-scene contrasts as pixels operate independently, as shown in Fig. 6.

Under general illumination changes – e.g., switching on room lights – PVDVS, PVTTS, and Dual Mode each behave as designed (Fig. 7), with Dual Mode delivering time-encoded intensity only where motion was detected. A key advantage of the positive-ramp scheme is performance in dim conditions: darker pixels trigger earlier, so informative data arrive sooner without requiring long integration. This feature provides a significant benefit and broadens the potential application space for this kind of sensors.

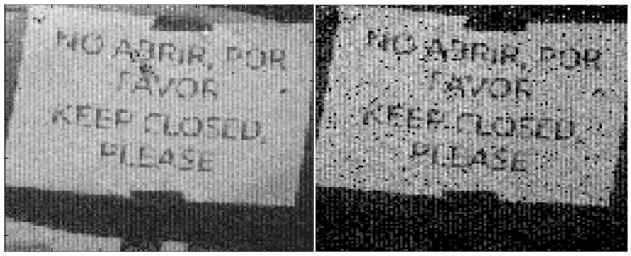

Figure 5. *PVTTS High Dynamic Range demonstration from* < 1 *lx (right) to* 1 *klx (left).*

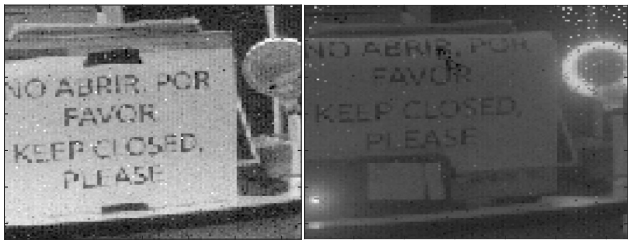

Figure 6. *PVTTS High Intra-Dynamic Range, as pixels work independently.*

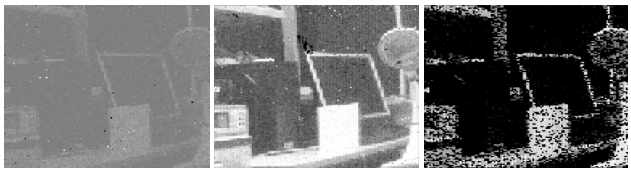

Figure 7. *Turning on the lights in our lab. From left to right: PVDVS, PVTTS and Dual Modes. It demonstrates the correct operation of the three modes.*

Electrical Characterization Results

As outlined in the previous sections, the PVTTS generates an event once the global ramp reaches V_{oc}, thereby encoding light intensity in the time domain. One of the main advantages of using this approach is that longer integration times are not required to capture information under low-light conditions. In fact, because the global ramp has a positive slope, dimly illuminated pixels trigger events earlier than brighter ones. Adjusting the ramp slope trades temporal resolution and event rate against timing variability caused by periphery collisions and FPGA-induced delays. A previous specification exercise set bounds so that FPGA and arbitration latency each remain below 1% of the ramp rise time, and the comparator offset below 10 mV; shallower ramps mitigate variability but reduce effective frame rate, while steeper ramps increase throughput until encoding errors appear. We observed that when the scene activity grows (more simultaneous requests), collisions/delays degrade the time encoding; Dual Mode alleviates this by restricting requests to pixels with confirmed contrast.

Fig. 8 illustrates this behavior: with a 6.552 ms ramp, the PVTTS encoding degrades due to greedy arbiters and FPGA latency, which prioritize pixels column-wise and disturb timestamp order; limiting readout to $\sim 28\%$ active pixels (Dual Mode) restores proper encoding, while $\sim 40\%$ activity begins to reintroduce errors.

Histograms of time-stamps across the array under a stable halogen source (8 klx) – see Fig. 9 – show normalized standard deviations of 16.75%, 13.62%, and 8.54% for mean timestamps of 4.95 ms, 49.5 ms, and 495 ms, respectively, confirming that slower ramps yield tighter encoding. The data correspond to the mean pixel value of 10 consecutive captures, being also affected by temporal noise.

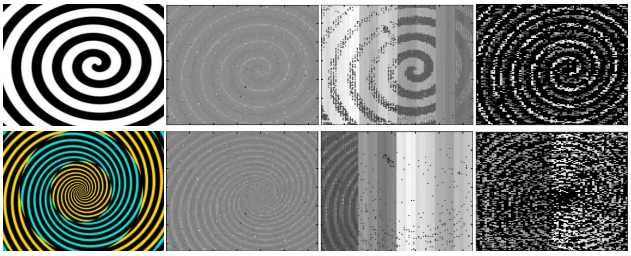

Figure 8. *From left to right: the original picture, Temporal Contrast Detection Mode, Exposure Measurement Mode, and Dual Mode outputs for a* 6.552 *ms ramp. In both cases the PVTTS is not able to properly encode light intensity into the time domain due to the delay induced by the FPGA during the readout, only corrected reducing the data throughput with the Dual Mode. Such mode provides a good performance for a reduced number of pixels detecting temporal variations on the scene (*28% *of pixels at the top), starting to be affected for a* 40% *of pixels requesting (bottom picture).*

Conclusions

We presented a proof-of-concept 128×128 pixel sensor implementing an alternative ATIS architecture by using a single photovoltaic diode per pixel to accomplish both event-driven temporal contrast (PVDVS) and time-encoded exposure (PVTTS). PVATIS supports three operating modes and addresses pixel-level constraints, by saving 5 transistors and using a single photodetector, reducing the noise level to twice the photon shot noise, and being self-biased, at the cost of lower bandwidth due to increased diode capacitance. The trade-off makes PVATIS particularly suitable for high-resolution, HDR, low-noise, and energy-efficient applications.

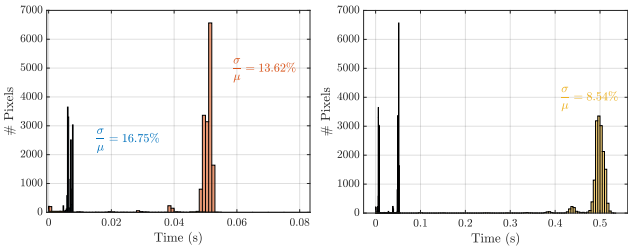

Figure 9. *Histogram of the number of pixels as a function of their timestamp, representing the Fixed-Pattern Noise of the PVTTS for three different ramp's slopes. The slower the deviation related to the mean, the better the illuminance is encoded into the time domain.*

Future work will complete characterization and extend the concept to MWIR/LWIR event-based imagers, where photovoltaic sensing is particularly beneficial.

References

[1] P. Lichtsteiner et al., "A 128× 128 120 dB 15 μs Latency Asynchronous Temporal Contrast Vision Sensor," in IEEE Journal of Solid-State Circuits, vol. 43, no. 2, pp. 566-576, Feb. 2008, doi: 10.1109/JSSC.2007.914337.

[2] Matthew G. McHarg et al., "Falcon Neuro: an event-based sensor on the International Space Station," Opt. Eng. 61(8) 085105 (31 August 2022) https://doi.org/10.1117/1.OE.61.8.085105.

[3] R. Fraenkel et al., "SWIFT EI: event-based SWIR sensor for tactical applications," Proc. SPIE 12534, Infrared Technology and Applications XLIX, 1253405 (13 June 2023); https://doi.org/10.1117/12.2663026.

[4] Y. Su et al., "An 8×8 Event-Based Vision Infrared Sensor ROIC With Adaptive Threshold Voltage Generation Circuit," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 71, no. 11, pp. 4708-4712, Nov. 2024, doi: 10.1109/TCSII.2024.3364753.

[5] C. Posch et al., "A Microbolometer Asynchronous Dynamic Vision Sensor for LWIR," in IEEE Sensors Journal, vol. 9, no. 6, pp. 654-664, June 2009, doi: 10.1109/JSEN.2009.2020658.

[6] M. He et al., "An Event-Driven High-Speed Imaging and Trace Detection ROIC for Cryogenic Infrared FPAs," 2024 IEEE International Symposium on Circuits and Systems (ISCAS), Singapore, Singapore, 2024, pp. 1-5, doi: 10.1109/ISCAS58744.2024.10558673.

[7] G. Gallego et al., "Event-Based Vision: A Survey," in IEEE Transactions on Pattern Analysis and Machine Intelligence, vol. 44, no. 1, pp. 154-180, 1 Jan. 2022, doi: 10.1109/TPAMI.2020.3008413.

[8] C. Posch et al., "An asynchronous time-based image sensor," 2008 IEEE International Symposium on Circuits and Systems (ISCAS), Seattle, WA, USA, 2008, pp. 2130-2133, doi: 10.1109/ISCAS.2008.4541871.

[9] R. Berner et al., "A 240×180 10mW 12us latency sparse-output vision sensor for mobile applications," 2013 Symposium on VLSI Circuits, Kyoto, Japan, 2013, pp. C186-C187.

[10] C. Posch et al., "Retinomorphic Event-Based Vision Sensors: Bioinspired Cameras With Spiking Output," in Proceedings of the IEEE, vol. 102, no. 10, pp. 1470-1484, Oct. 2014, doi: 10.1109/JPROC.2014.2346153.

[11] P. Fernández-Peramo et al., "A Photovoltaic Dynamic Vision Sensor," in IEEE Journal of Solid-State Circuits, doi: 10.1109/JSSC.2024.3524244.

[12] P. Fernández-Peramo et al., "Modeling the Photovoltaic Diode Region for High Dynamic Range Image Sensor Design," in IEEE Transactions on Electron Devices, vol. 73, no. 1, pp. 418-426, Jan. 2026, doi: 10.1109/TED.2025.3632828.

[13] A. Y. -C. Chiou et al., "A 137 dB Dynamic Range and 0.32 V Self-Powered CMOS Imager With Energy Harvesting Pixels," in IEEE Journal of Solid-State Circuits, vol. 51, no. 11, pp. 2769-2776, Nov. 2016, doi: 10.1109/JSSC.2016.2596765.

[14] S. O. Otim et al., "Characterization and Simple Fixed Pattern Noise Correction in Wide Dynamic Range "Logarithmic" Imagers," in IEEE Transactions on Instrumentation and Measurement, vol. 56, no. 5, pp. 1910-1916, Oct. 2007, doi: 10.1109/TIM.2007.903581.

[15] E. G. de Oliveira et al., "Effective cross comparison of mismatch effects on different logarithmic pixel sensor topologies," 2015 28th Symposium on Integrated Circuits and Systems Design (SBCCI), Salvador, Brazil, 2015, pp. 1-6.

[16] Y. Ni, "QLog Solar-Cell Mode Photodiode Logarithmic CMOS Pixel Using Charge Compression and Readout". Sensors 2018, 18, 584. https://doi.org/10.3390/s18020584

[17] R. Fragasse et al., "Signal and Noise Analysis of an Open-Circuit Voltage Pixel for Uncooled Infrared Image Sensors," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 68, no. 5, pp. 1827-1840, May 2021, doi: 10.1109/TCSI.2021.3068595.

[18] Y. Niet al., "Logarithmic InGaAs detectors with global shutter and active dark current reduction," Proc. SPIE 9485, Thermosense: Thermal Infrared Applications XXXVII, 94850L (12 May 2015); https://doi.org/10.1117/12.2176392

[19] M. Sivilotti, "Wiring considerations in analog VLSI systems, with application to field-programmable networks". California Institute of Technology, USA, 1991, doi:0.7907/stj4-kh72

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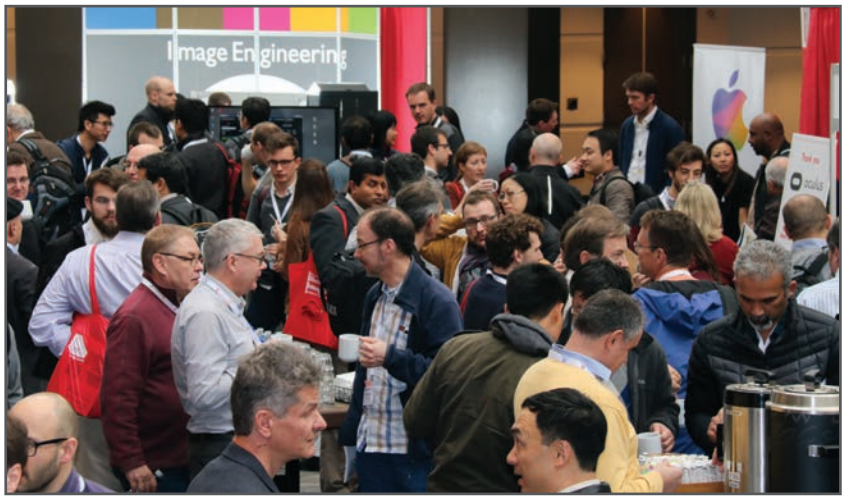

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