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Simulation of indirect time-of-flight pixel using high frequency operation low voltage trench gates

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Abstract

The integration of trench vertical transfer gates in an indirect time of flight pixel has been studied through TCAD & optical simulations. A small fast photo-gate pixel surpassing state of the art performances has been designed and optimized thanks to these advanced multiphysics simulations. Quantum efficiency of 40% is obtained and demodulation contrast of 89% at 200MHz is achieved while transfer gates operate at 1.0V biasing.

Introduction

The increasing market demand for depth sensing applications requires high resolution and low power consumption devices.

Indirect time-of-flight (iToF) is a suitable competitive solution. It reconstructs the depth information using an optical signal modulated in intensity at high frequency at hundreds of MHz. Fig. 1 introduces the phase difference measurement taking place in the sensor. The phase reference of the emitted signal (dashed blue line) is compared with the measured phase value from the received signal (doted red line). A modulation operation samples the photo-generated charges into different collection sites at different times for each pixel. The efficiency of charges transfer from the pixel to sensing nodes is given at the operation frequency f_{Mod} by the demodulation contrast (DMC) [1].

An efficient transfer depends on charge carriers path in the collection volume. In contrast, thick absorption layers are used to increase sensitivity of silicon devices to Near Infra-Red (NIR) wavelength. A trade-off is identified between quantum efficiency (QE) and DMC [1].

The improvement of transfer requirement is not exclusive to iToF solutions. Pixels for various applications integrate clever solutions to improve the charge collection in a pixel. It is the case of pinned photogate (PPG) pixel for visible light sensing [2]. Trench vertical gates (TVG) used as transfer gates (TG) allow an efficient charge transfer in the pixel collection volume. For a low DC biasing, closed TVG allow the storage of a significant number of charges in the pixel sensing zone while having a low dark current [2].

3D TCAD simulations have been carried out to investigate TVG into an iToF fast photogate (FPG) pixel. The increasing capability of numerical methods allows the prediction of trends and a deeper understanding of studied devices even within complex full 3D pixels [3]. It has been the case for iToF devices [4].

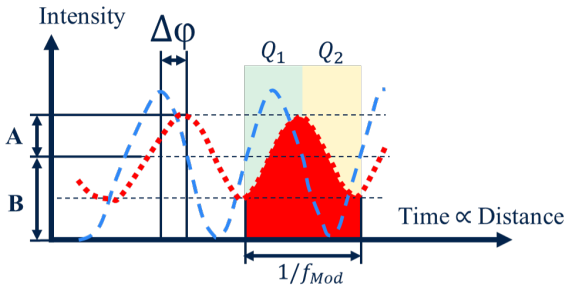

Figure 1. *Schematic iToF phase comparison operation. Dashed blue and doted red signals are respectively the emitted and the received light wave. Photo-generated measured charge, Q_1 and Q_2 are collected in separated sensing nodes. Light signal is modulated at the demodulation frequency f_{Mod}.*

Pixel structure and Simulation Methodology

We propose a small pitch FPG iToF pixel using TVGs for increased efficiency in charge transfer. The pixel fabrication process flow and operation have been simulated with TCAD [5]. The pixel is sensitive to NIR light and operates with a 940nm wavelength. Studied FPG pixel simulation focus on three main figures of merit: DMC, QE and power consumption. Nevertheless, as for the PPG [2], the proposed FPG iToF pixel could also be used for acquiring 2D intensity image. Performances for 2D imaging are estimated by simulating the maximum charges that can be stored in the pixel volume and measured in the output nodes, called the full-well capacity. Optimization focuses on 3D depth imaging; however, complementary simulation study evaluates full-well capacity for the proposed pixel.

Demodulation contrast, DMC

DMC value can be correlated to the transit time of photo-generated carriers in the pixel [4]. After photon absorption, generated electron/hole pairs drift in the pixel volume and are collected in the sensing nodes. Charge carrier transport is calculated by solving continuity equations. The considered electron mobility degradations are: two-dimensional Coulomb impurity, surface roughness and phonon-electron scattering.

Charge transit time depends mainly on drift field and carrier mobility. The DMC is given by the measured amplitude over offset ratio, indicated in fig. 1 respectively by A and B, which in

turn depend on the demodulation frequency f_{Mod}. Hence, in simulation an impulse stimulus of light is used to extract the current response measured in the sensing nodes OUT_1 and OUT_2. It is obtained for a specific bias condition of TGs illustrated in fig. 2.(a). Photo-generated charges are collected in OUT_1. The integration of the measured current values gives the collected charges in time for each sensing node. Fig. 3 shows the percentage of charges collected in OUT_1 and OUT_2.

The studied device is composed of two tap pixels, that means that during demodulation TG are toggled between *on* and off state twice per period. Because of that, the time domain is multiplied by the number of samples per period, also called the number of taps N_{tap}. The current response measured in OUT_1, i_{OUT_1} is post-processed through a fast Fourier transform (FFT). As all charges are measured for the duration of the simulation ($t >> \frac{1}{f_{Mod}}$), the obtained response can be normalized by the offset FFT response at f_{Mod} equals 0Hz. The obtained FFT has a real and an imaginary part. The real part gives the AC current response obtained in output as in eq. 1.

$$DMC(f_{Mod}) = Re\left\{\frac{fft[i_{OUT_1}(N_{tap}t)](f_{Mod})}{fft[i_{OUT_1}(N_{tap}t)](0)}\right\} \quad (1)$$

Quantum efficiency, QE

Optical simulations were carried out with a commercial finite-difference time-domain (FDTD) solver [6]. A complete stack was built, integrating micro-lens, antireflective layer, light structuration, metallic routing layers and deep trench insulator between pixels.

In FDTD simulation, the volumic optical absorption matrix is computed from the norm of the electric field [3].Quantum efficiency is computed from the percentage of absorbed power inside the sensitive volume normalized by the source power.

Optical stack optimization is required for each variant. Because of that, to compare different designs, DMC simulations were carried out while using an uniform optical generation in the volume of the pixel.

Power consumption

A periodic voltage signal with a high value $V_{TG}(on)$ and a low value $V_{TG}(off)$ is applied to TGs. Therefore, the overall capacitance $\widehat{C}_{TG}$ of the gate is charged and discharged periodically over the time during the whole demodulation phase. Equivalent average capacitance in the operation interval $[V_{TG}(off);V_{TG}(on)]$, C_{TG} can be estimated as in eq. 2 with capacitance simulations. AC-analysis are carried out to estimate the theoretical evolution of capacitance versus voltage $C_{TG}(V)$. The difference of potential, ΔV is the voltage excursion of a TG toggled between the *on* and the off state.

$$\widehat{C}_{TG} = \frac{\int_{V_{TG}(off)}^{V_{TG}(on)} C_{TG}(V)dV}{\Delta V} \quad (2)$$

Depending on gate biasing V_{TG}, equivalent capacitance C_{TG} can be impacted significantly as shown by eq. 3. By operating close to flat band voltage, V_{fb} and lower than threshold voltage, V_T, the inversion capacitance C_{inv} is neglected. Gate capacitance C_{ox} is then reduced by the depletion capacitance C_D, thanks to the depletion of the semiconductor surrounding the gate.

$$C_{TG} = \left(\frac{1}{C_D + C_{inv}} + \frac{1}{C_{ox}}\right)^{-1} \quad (3)$$

The power consumption P per pixel can be finally estimated according to eq. 4. It depends on the demodulation frequency f_{mod}, the squared value of the demodulation voltage swing ΔV and the overall capacitance per pixel that has to be charged and discharged for each demodulation cycle. Such a capacitance is given by the above mentioned $\widehat{C}_{TG}$ and C_{par} which is the parasitic capacitance related to the metal routing of the TG signal in the pixel, multiplied by the number of taps N_{tap}, i.e. the number of the gates in the pixel that are used for the demodulation. Aiming to optimize TG biasing, the capacitance is simulated in TCAD using small-signal AC-analysis.

$$P = N_{tap} f_{Mod}(\widehat{C}_{TG} + C_{par})\Delta V^2 \quad (4)$$

Results and Discussion

Several process and design proposals have been evaluated with 3D TCAD simulation. A cross-section of the simulated structure is presented in fig. 2.(b). Pixels are surrounded by deep trench isolation biased at V_{DT}. Deep trench MOS operates with low DC biasing in strong hole inversion regime and fully depletes the pixel volume [2]. Three implants are necessary: $^{(1)}$sensing nodes OUT_1 and OUT_2 N+ implant, $^{(2)}$ground *GND* P+ implant and $^{(3)}$deeper P- box implant. Poly-silicon inside TVG is etched. Etched trenches are filled with trench oxide (TO) for sensing node isolation.

According to FDTD simulation, QE of 40% can be obtained with a thick collection volume. Based on the charge response in fig. 3, an efficient charge transfer is achieved. The use of TVGs gives a solution with a good trade-off between QE and DMC. It is also seen that, parasitic light signal (PLS) measured in OUT_2 is close to 0%.

The designed iToF pixel could also acquire a performant 2D image. Indeed, two operation modes are identified, biasing is optimized for both.

Biasing optimization 3D iToF mode

TVGs with poly-silicon doped Phosphorus (N-type), were compared with Boron (P-type) doping. Fig. 4 shows the evolution of capacitance function of biasing of TVG obtained with small signal AC-analysis simulation. The shift in V_T with the use of N-type doped poly-silicon can reduce capacitance up to 30% in the interval of 0.0V to 1.0V. The capacitance with real application is also simulated by applying 2.5V to sensing nodes OUT_1 and OUT_2. The simulation is performed at low and high frequencies. As the pixel is already fully depleted, no high frequency change with C_D is observed. $\widehat{C}_{TG}$ is computed to 1.0fF per gate and C_{par} is approximated to 0.5fF per gate. Simulated structures in fig. 5.(c-d) illustrate using hole and electron densities the depletion regime between $V_{TG}(on)$ 1.0V and $V_{TG}(off)$ 0.0V.

For the same biasing, electrostatic potential lines are homogeneous from bottom to sensing nodes with no barrier observed for TVG high biasing of 1.0V, fig. 5.(a-b). Barrier observed with gates biased at 0.0V is significant and sufficient to prevent parasitic signal collection in OUT_2, fig. 3. It is observed with fig. 5 that

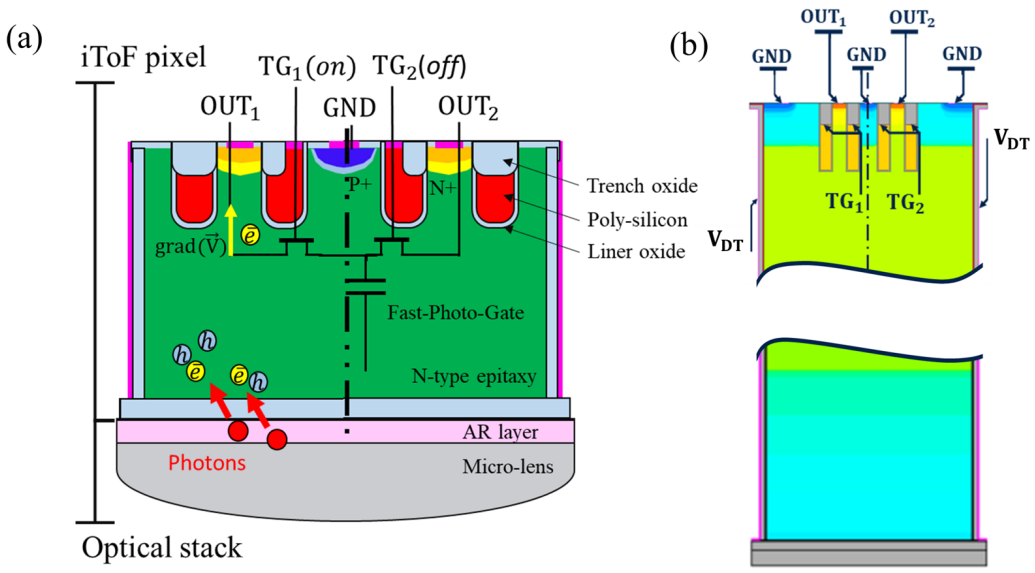

Figure 2. *FPG iToF pixel (a) schematic and (b) simulated structure cross section with trench gates, contacts and pixel deep trench isolation biased at V_{DT}.*

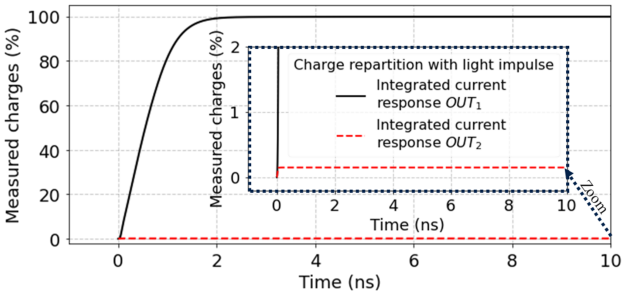

Figure 3. *Simulated charge percentage in time. Charge is obtained by integrating current response for a light impulsion stimulus.*

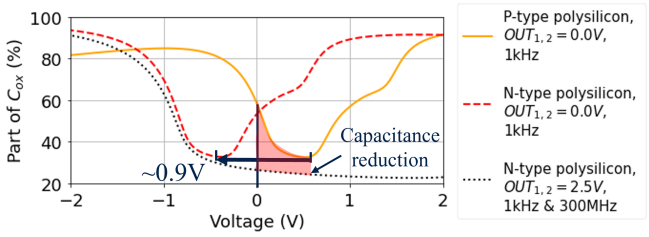

Figure 4. *Capacitance function of gate biasing for poly-silicon different doping types. A different reference potential for electrons is attempted for OUT_1 and OUT_2 for low and high frequencies. GND reference biasing for holes is 0.0V.*

the poly-silicon doping choice is suitable for iToF operation and that performant demodulation with TVG can be achieved while operating entirely in the depletion regime.

Biasing optimization 2D mode

Strong hole inversion is expected for a biasing lower than -1.0V when using the N-type poly-silicon doping shown in fig. 4. For a lower biasing condition e.g. TVG at –1.6V, a significantly high potential barrier is achieved, fig. 6. When this low biasing is applied to TVG, the photogenerated electrons are stored in the depleted pixel volume. The high potential barrier prevents the charges in the volume to leak to the output nodes. At a later time, transfer gates are activated for the read-out of electrons stored in the pixel volume. The total measurable charges for this operation is the full-well capacity. It is a key figure of merit for the 2D mode operation.

Full-well capacity is estimated over 16000 electrons for the studied case and it increases as the barrier height increases. Fig. 6 shows that a trade-off exists between 2D and 3D metrics, namely full-well capacity and DMC versus $TG(off)$ bias value. In spite of 2D high performances, the electrostatic potential in the volume of the FPG is optimized so that iToF 3D operation is facilitated. A $TG(off)$ bias value of 0V is chosen here for iToF operation.

TVG optimization

Trench oxide (TO) depth is identified as a crucial process parameter for the improvement of the pixel. Originally, the TO brick is intended to avoid leakage due to high electric field between TVG from highly doped zones [7]. Herein, aiming to reduce TVG oxide capacitor C_{TG}, deeper TO is proposed. With TO depth increase, shallow N+ sensing nodes can present transfer issues. Fig. 7 illustrates the problem identifying in fig. 7.(c) a zone where potential pockets preventing proper charge transfer can appear between N+ diffusion zones and TGs for deeper TO.

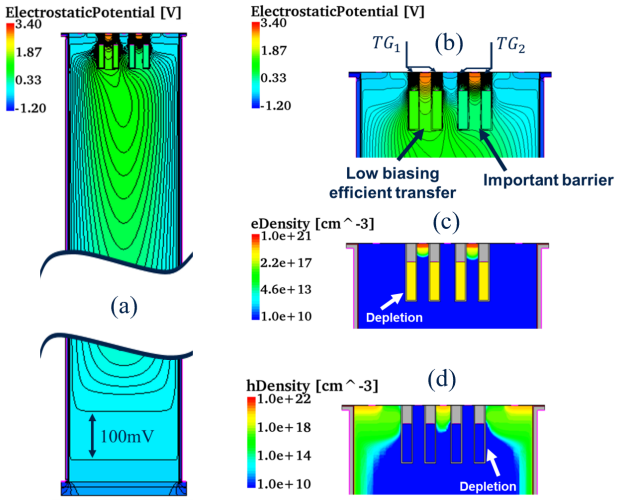

Figure 5. *FPG pixel electrical simulation operating in 3D mode. TG_1 is biased on with 1.0V and TG_2 is biased off with 0.0V. Cross-section (a) a view of the sensing volume electrostatic potential with equipotential lines each 100mV, (b) TVG transfer and potential barrier, (c) electron density for high TG biasing depletion regime and (d) hole density for low TG biasing depletion region.*

An optimum depth of TO is identified by the maximum of the figure of merit (FoM) presented in fig. 8. The FoM relation is given in eq. 5. It consists of the ratio between DMC and power consumption for one TVG. Fig. 8 shows that a DMC at 200MHz over 80% can be maintained while increasing TO depth to 50% of VTG depth. C_{TG} depending on the gate surface decreases significantly as shown by eq. 2. The best trade-off is identified around 45% TO depth for the studied shallow N+ implant and TVG depth. By implanting sensing nodes deeper a better transfer can be attained.

$$FoM = \frac{DMC(\%)}{Power(\frac{\mu W}{gate})} \tag{5}$$

Comparison with prior State-of-the-Art

3D simulations of planar gate solution have been carried out with same pixel thickness and pitch than TVG proposed solution. Fig. 9 presents the evolution of DMC at 200MHz and 300MHz between both solutions in simulation with same sensing zone depth. For TVG proposal, difference of potential could be as low as 0.8V, while maintaining better than state-of-the-art DMC performances over 88%. When compared to planar gate solution, TVGs iToF shows significantly higher performances in term of DMC.

FPG pixel has performant DMC values at 200MHz while operating at very low biasing. Indeed, to reduce TVG power consumption lower than planar TG consumption, TVGs drivers could operate with low reference voltage. Table I compares state-of-the-art solutions with simulated solution.

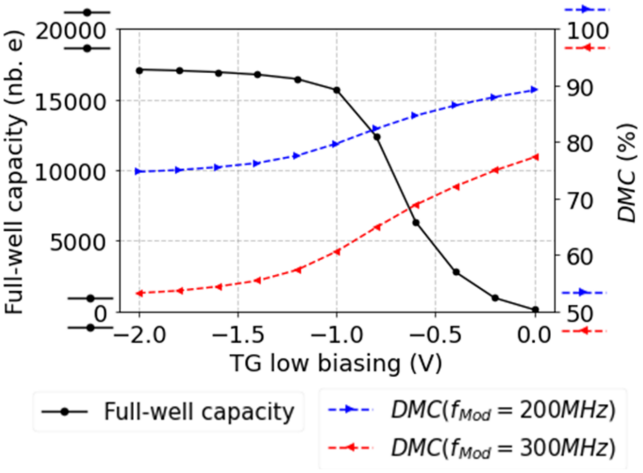

Figure 6. *Electrical simulation full-well and DMC results for FPG operating in 2D and 3D modes versus off biasing for 1.0V on biasing.*

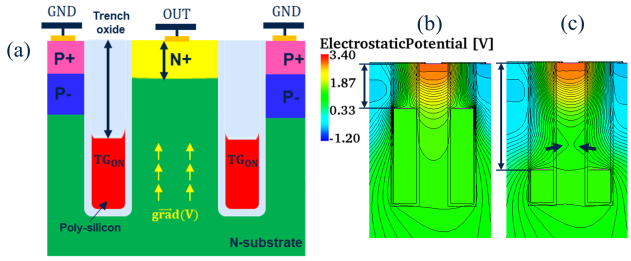

Figure 7. *(a) Schematic representation of N+ implantation depth and TO depth impact on charge transfer. Shallow N+ implantation with (b) shallow TO and (c) deeper TO.*

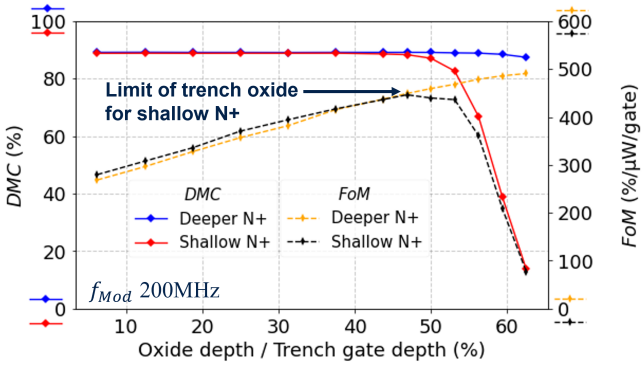

Figure 8. *DMC and FoM at 200MHz versus TO depth and TVG depth ratio.*

Trench Against Planar Gates iToF

iToF pixel	TVGs	Planar gates		
	This work	***Keel [8] (2021)***	***Tubert [9] (2021)***	***Ebiko [10] (2020)***
DMC @f_{Mod}	89% @200MHz	80% @200MHz	88.5% @200MHz	79% @200MHz
QE@940nm	40%	38%	18.5%	32%
Consumption p/ pixel eq. 5 @f_{Mod} @ΔV	$1.2\mu W$ (2-taps) @200MHz @1.0V	— @200MHz @1.05V	$1.4\mu W$ (2-taps) @200MHz @1.2V	— @200MHz @1.2V

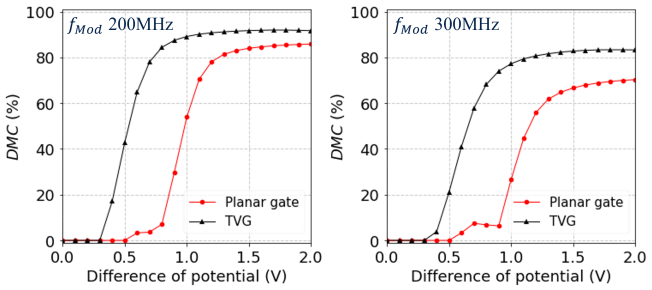

Figure 9. *Trench against planar gate iToF pixels best case, DMC at 200MHz and 300MHz function of difference of potential, ΔV between TGs.*

Conclusion

A small pitch trench vertical gate iToF pixel was validated using 3D TCAD simulations. The fast photogate solution shows in general better performances than state-of-the-art. Demodulation contrast (DMC) values of 89% are obtained at 200MHz and of 77% at 300MHz, while transfer gates operate at a 1.0V difference of potential. Such a low biasing operation allows a lower consumption per pixel than planar gates. Moreover, 3D optical FDTD simulations give a high quantum efficiency (QE) of 40%. Fig. 10 shows transmission electron microscopy (TEM) cuts of the trench vertical gates in promising fast photogate pixel design on-going fabrication.

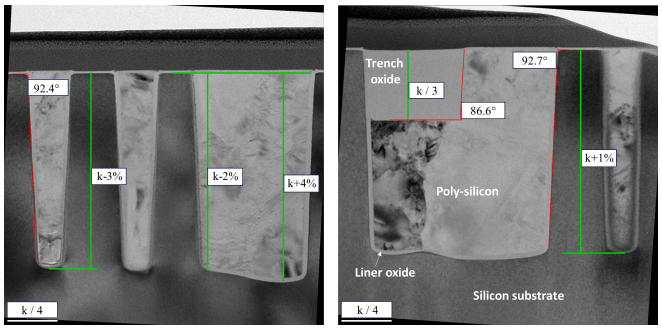

Figure 10. *TEM cut images of fabricated TVG in a designed reference FPG pixel. The targeted depth is indicated by k. TVG and trench oxide etching profiles are slightly flared to avoid the creation of filling voids during the fabrication process.*

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References

[1] R. Lange and P. Seitz, "Solid-State Time-of-Flight Range Camera," IEEE J. Quantum Electron., vol. 37, no. 3, pp. 390–397, 2001.

[2] F. Roy, "Fully Depleted, Trench-Pinned Photo Gate for CMOS Image Sensor Applications," Sensors, 2020.

[3] A. Crocherie, "From photons to electrons: a complete 3D simulation flow for CMOS image sensor." IEEE International Image Sensor Workshop, IISW, 2009.

[4] G. Mugny, "Demodulation contrast simulation for indirect time-of-flight sensors based on fast photo-diode," IEEE International Image Sensor Workshop, IISW, 2021.

[5] Sentaurus Device User Guide, version S-2021.06, June 2021.

[6] Lumerical, Inc., FDTD: 3D Electromagnetic Simulator, version 2022-r6, 2022.

[7] A. Suler, "Développement d'un pixel photogate éclairé par la face arrière," HAL Id: tel-03632251, pp. 62-64, 2022.

[8] I. Keel, "A 4-tap 3.5µm 1.2Mpixel indirect time-of-flight CMOS image sensor with peak current mitigation and multi-user interference cancellation," IEEE International Solid- State Circuits Conference, ISSCC, San Francisco, CA, USA, 2021, pp. 106-108.

[9] C. Tubert, "4.6µm Low Power Indirect Time-of-Flight Pixel Achieving 88.5% Demodulation Contrast at 200MHz for 0.54MPix Depth Camera,"IEEE European Solid State Circuits Conference, ESSCIRC, pp. 135–138, 2021.

[10] Y. Ebiko, "Low power consumption and high resolution 1280X960 Gate Assisted Photonic Demodulator pixel for indirect Time of flight," International Electron Devices Meeting, IEDM, vol. 2020-Decem, pp. 33.1.1-33.1.4, 2020.

Author Biography

Originally from Brazil, the author moved to France in 2015 to study electrical engineering in Institut National des Sciences Appliquées (INSA) Lyon. In 2020 the author obtained an engineering degree with a specialization in integrated electrical systems. The author then worked at STMicroelectronics in Crolles-FR until April 2021 when he started his PhD studies at the same company in partnership with Univ. Grenoble Alpes, Univ. Savoie Mont-Blanc, CNRS, Grenoble INP and IMEP-LaHC at Grenoble under the supervision of Anne Kaminski, Maryline Bawedin and Pascal Fonteneau aiming to develop new solutions for indirect time-of-flight pixels for 3D imaging applications.