https://doi.org/10.2352/EI.2024.36.7.ISS-282

Single slope single ramp column ADC with digital CDS for CMOS Image Sensors

Pedro Santos, Idham Hafizh, Jeffrey Prinzie, Paul Leroux, Guy Meynants; Katholieke Universiteit Leuven; ECS - ADVISE, Geel Campus, Belgium.

Abstract

This article presents a novel architecture of a single slope single ramp column analogue-to-digital converter (ADC) for CMOS image sensors (CIS). The outlined ADC uses a global single slope ramp (SSR) with two comparators and two counters per column, one for the pixel reset level and one for the pixel signal level. A common reference level is used to start the conversion, while the reset and signal levels are used to terminate the respective conversion. With this architecture, the pixel reset, and signal levels are converted within a single conversion cycle. When the counter results are ready, a digital correlated double sampling (CDS) output is achieved by subtracting the reset counter value from the signal counter value with a digital subtractor. This architecture provides speed, offset compensation, and input swing adjustment through the reference level. Furthermore, the implementation is less vulnerable to temporal row noise, which is then suitable for low-noise applications. A 12-bit column ADC was designed and implemented in a 1920 x 1080 resolution CIS demonstrator, using a 0.18 µm CIS process. With 200 MHz counter operation, the readout operation results in 25 frames per second.

Introduction and Background Context

Modern CMOS Image Sensors (CIS) rely on column-level analog-to-digital converters (ADCs) based on a ramp slope as a reference for comparison. A parallel conversion of multiple columns permits the achievement of higher speed and compact size.

The architecture design is based on the column-parallel single slope ramp (CPSSR) ADC for high-speed CMOS Image Sensors [1].

The single slope ramp ADC relies on 3 main blocks: the ramp generator, the column-level comparator, and the counter. For pipelined or interleaved operation two additional blocks may be used: a sample and hold block that captures the data to be converted and an SRAM block that stores the conversion result to be afterwards read during the data readout. In standard ramp ADCs, the conversion starts with the counter and the ramp value in the reset position. Then the analog input of the ADC is compared against the ramp whilst the counter is clocked. Once the difference between the ramp and the ADC column input is smaller than the comparator input offset, the comparator toggles, and the digital counter is stored in the memory. As each column has a counter and a comparator, the respective column input analogue value is compared, converted to a digital value and stored in the column SRAM. This method provides a compact and fast conversion method of the row pixel output values in one single conversion period.

Additionally, pixels of CMOS image sensors are the source of many noise components due to the complex operation of signal conversion and amplification. The same applies to the electronic readout and as in any electronic application, the noise impact should be minimized to improve output quality. To reduce noise from the pixel readout, correlated double sampling or CDS [2] [3] [4] [5] [6] is used. But even after CDS, readout electronics noise may also cause visible row and/or column patterns that are quite noticeable, especially in low light conditions which are therefore not acceptable. A source of this may be a noisy column amplifier reference or ramp reset level, which causes a large temporal variation of the row offset level (row noise). Another visible artefact may be excessive temporal noise in a column amplifier, resulting in a very noisy column. According to [3], systematic column and row offsets or other deviations should be 20 dB or more below the pixel noise to not be noticeable, thus schemes to reduce row and column noise must be in place when designing CMOS image sensors.

CDS operation can effectively reduce row and column noise by reducing the effects of reset noise of the floating diffusion (kTC noise), the flicker noise of the source follower (1/f noise) and the offset signal originating from the source follower.

CDS operation can be done in the analogue domain, the digital domain or even both combined. There are various SSR ADC designs with CDS feature implemented, being the most used column-level ADC architectures with digital CDS, present in recent designs that rely on two successive conversions [7] [8].

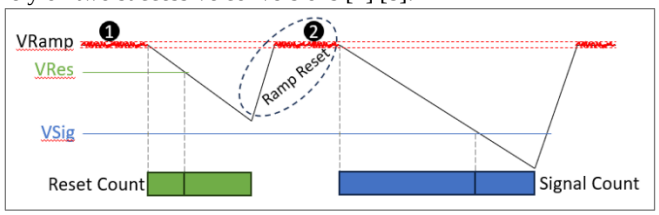

Figure 1. *ADC conversion principle presented by [8]*

Figure 1 presents its principle of operation: the pixel reset level conversion is followed by pixel signal level conversion. Both conversions rely on a separate ramp signal and an up-down counter performing the summation/subtraction. However, the ramp signal needs to be reset accurately to its original level in between both conversions - levels ❶ and ❷ - since any noise on the ramp reset will be seen as temporal row noise in the image. Another SSR ADC with a CDS proposal [5] suggests that both the signal and the reset levels are converted within a single ramp cycle. Figure 2 presents the ADC operation of this proposal.

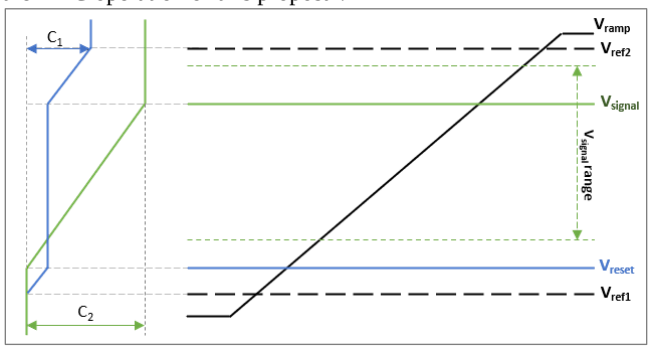

Figure 2. *ADC conversion principle presented by [5]*

For this, two reference voltages are used to start and stop the counters according to a 4-state complex structure: the first counter counts from V_{ref1} until V_{reset}, holding the value until V_{signal} and resuming counting from V_{signal} until V_{ref2}. This counting range is C_1; the second counter, therefore, counts from V_{reset} until V_{signal}, being this counting range C_2.

The final signal value is given by the relationship (1) [5]:

$$Final\ signal \sim \frac{C_2}{C_1+C_2} \sim \frac{V_{signal}-V_{reset}}{V_{ref2}-V_{ref1}} \quad (1)$$

Although this solution offers speed and implements CDS as expected, the final value (1) requires the adoption of a digital division per column, which adds complexity, area and power consumption.

Novel SSR ADC Architecture

The proposed scheme in this article uses, a single slope ramp for both the pixel reset and pixel signal levels conversion. Similar to other architectures [5], it converts both the pixel signal and pixel reset values during one ADC cycle, but, in this case, with simplicity, symmetry and power consumption saving in mind. A faster conversion is achieved and temporal row noise is drastically reduced. Digital CDS is applied with this architecture by subtracting the digital reset value from the digital signal value, which also cancels the comparator input offset. Figure 3 shows the operation diagram of this solution.

The presence of the V_{Ref} signal acts as a starting point reference to start the counting operation allowing a perfect adjustment of the ADC input ranges. The entire counter operation depends only on the V_{Ref} value and the input analogue values V_{Res} and V_{Sig}.

In comparison with the traditional ADC with CDS, this scheme requires full duplication of the comparator and counters. This scheme requires more area to accommodate two comparators, two counters, and a subtraction block. Therefore, a slight increase in power consumption is expected since the two counters are running in parallel at the beginning of the conversion operation until the reset level comparison is completed. However, the power penalty is compensated by the slower clock frequency that is required for its operation when compared with the classical schemes [7] [8].

Operation description

The conversion process starts with the ramp and the counters in the reset state. Regarding the ramp voltage level, since it uses a negative slope it represents that the reset level is a voltage level close to the supply level (for example 2.8V for a 3.3V supply). The comparison starts with the ramp reset release and the ramp starts to descend linearly with time. With the ramp reset release, both comparators from reset and signal paths are armed comparing the V_{Ref} signal against the ramp slope. When the difference between the V_{Ramp} and the V_{Ref} signal is smaller than the comparator input offset, the comparator toggles, triggering the start of the reset path and the signal path counters. Then the comparators are reset and armed again to compare the input signal against the V_{Ramp}: the input reset voltage V_{Res} for the reset path comparator and the input signal voltage V_{Sig} for the signal path comparator. It's important to note that a good understanding of the speed, stability and bandwidth of the comparators needs to be in place once for the reset path, some time is required to rearm the comparator for the second comparison. If V_{Ref} level is too close to the V_{Res} level, there is a chance that the comparator is not ready yet and misses the second comparison, leading to an incorrect (saturating) reset counter result. This counting scheme does cancel also comparator offset and delay variations.

Once the reset counter stops, the comparator remains in the toggle position and waits until the next row time.

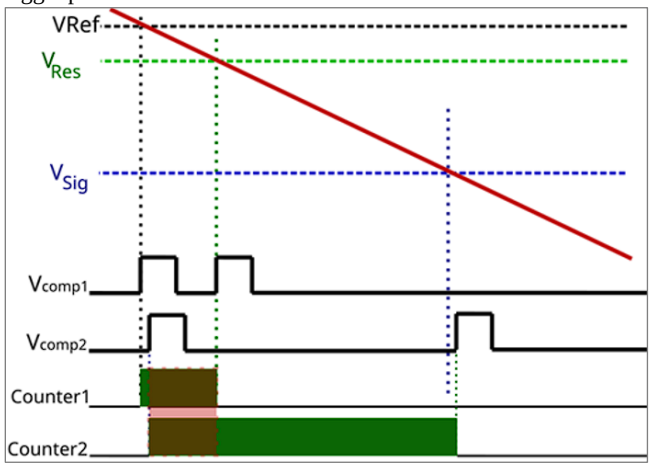

Figure 3. *Operation Diagram of the proposed SSDCR ADC*

Meanwhile, the signal path comparator tracks the V_{Sig} signal and compares it with the V_{Ramp} value. In the same way, when the difference between the V_{Ramp} and V_{Sig} is smaller than the comparator input offset, the comparator toggles, stopping the signal path counter. Then the two digital counter values are subtracted and the result is stored in the column SRAM block. The conversion ends when the ramp reaches the minimum value, being the ramp reset to the initial value.

It is important to mention that for this conversion with CDS, the ADC operation depends on the sampling and hold (storage) of the pixel reset and pixel signal values. This is achieved by the use of two sample and hold (S&H) blocks that capture the respective pixel reset and pixel signal values when the pixel output is set to the corresponding output level. Figure 4 shows the generic block diagram that presents the two signal and reset paths and where the two S&H, two comparators and two counter blocks are depicted. The use of the 4T pixel is shown as a reference however other pixel topologies are also possible. In low-noise applications, the S&H can also be an active stage whose gain is greater than unity.

When comparing this architecture with [5] [7] and [8], we can stress the improvements that this new architecture brings.

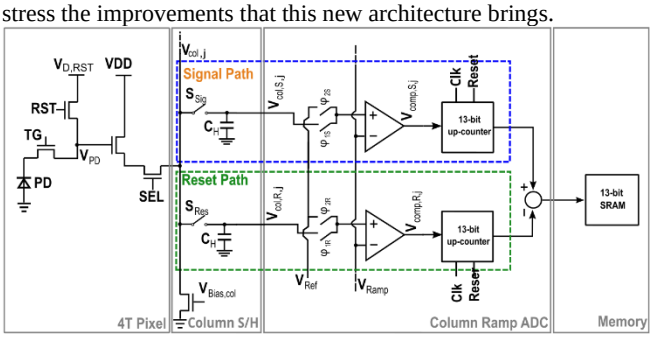

Figure 4. *Bock Diagram of the SSR ADC*

Speed: the speed that the A/D conversion can achieve is an important factor to allow faster sensor operations. Either in full sequential or pipeline operation, if the A/D conversion is slow, it

will limit the fastest acquisition and therefore the frame rate that can be acquired by the image sensor. In [7] and [8] the operation requires 2 ramps for the reset and signal conversions, meaning that the reset is initially converted with a counting range, then the ramp is reset and then the signal is also converted, with either up/down counting or with the addition of the 2 conversions. This sequential process is an important limitation for high-speed designs, and, adopting this new architecture or the architecture presented in [5] can perform the ADC faster.

Row noise: the use of the CDS, as already explained is important to keep the row and column noise low enough when compared with the pixel noise. Both [7] and [8] propose CDS operation, but the need to have a ramp reset in between the two comparison operations can lead to additional row noise that is not cancelled by the CDS operation. Besides the fact that a 2-ramp setup can introduce gain error, the ramp reset level for the signal conversion needs to be precisely tuned to the ramp reset level for the reset conversion, otherwise, it will result in row noise. This requires an accurate design for the ramp reset driver leading to additional complexity and appropriate time for ramp reset settling, impacting the overall A/D conversion speed. This design as well as the architecture presented in [5] use a single ramp for either conversion of the signal and the reset levels, resulting in a significant row and column noise reduction to suppression, since both conversions see the same reference regarding the ramp reset and ramp gain concerns.

Power: the power consumption in image sensors is a crucial aspect since multiple thermal noise components increase significantly with self-heating leading to a significant impact on the image sensor quality performance. The dark current is sensitive to temperature variation [9], thus a low-power device will lead to a lower dark current, and therefore less dark current shot noise and better performance. The current work, likewise described in the architectures [7] and [8], proposes power-efficient designs where the ADC complexity is kept low and the essential blocks can be designed to be power-efficient. In the case of [7] and [8] as the conversions of reset and signal values are done sequentially, the power required is split over time. Also the most power-consuming block – the counter – is operated only the time required to have a conversion. This time is short for the reset level and may be longer for the signal conversion. In the case of the outlined design, in spite that the two counters and comparators operate in parallel at the start of the conversion cycle, the power does not increase since the reset counters operate for a small time period and both conversions are made in a single ramp time. Additionally, a better trade-off between speed and power consumption is achieved since the counters can operate at a lower frequency than other architectures. For the case of [5], as the design includes a complex counting scheme as well as a column-level oscillator and digital division block, it is more power-hungry.

Complexity: Following the previous explanation, one can conclude that either the current design or the solutions presented in [7] and [8] show a relatively simple and straightforward implementation of the ramp ADC with CDS. In opposition, the solution proposed in [5], requires a fast comparator, two reference voltages, a state machine that controls a complex counting scheme, a column-level oscillator and a digital division block. When compared to classic ramp ADC designs with CDS, it clearly shows a more complex structure to accomplish the proposed conversion.

Prototype Implementation

To validate the presented architecture, a circuit-level demonstrator was developed, implementing the key elements that are presented in Figure 4. The image sensor prototype is a 1920x1080 matrix size (FHD), has a 12-bit SSR ADC and is designed in columns of 10 µm pitch and two readout sides of 960 columns each. Figure 5 shows the floor planning of the column-level implementation for this prototype.

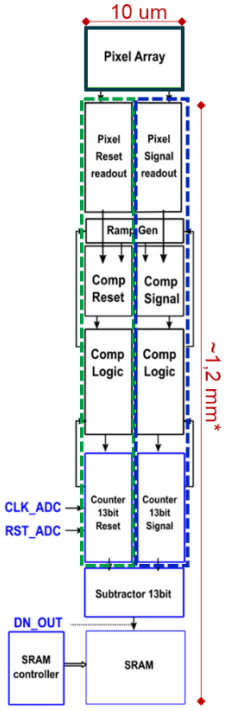

Figure 5. *Floorplan of the column-level implementation (*180nm Technology)*

The technology node is a 180nm CIS process. In terms of operation, the prototype can produce up to 25 frames per second in FHD mode and 12-bit ADC resolution. With this operation, the counters can operate up to 200MHz clock frequency.

The implementation follows the proposed diagram from Figure 4, where two exact copies of the S&H, comparator, decision logic and counter are placed per column, in this case designed in a pitch of 5 µm.

Another aspect to highlight is the ramp generator block: the base current for this block is located in the periphery of the readout block and a current is provided to a distributed capacitor placed across the columns of the readout block. The large distributed capacitance with wide metals delivers a stable ramp reference to all columns, reducing mismatch and propagation delay.

Layout considerations

As referred, the layout design is in general straightforward with basically block duplication within the column readout. However concerning the operation, since the ADC comparators toggle almost simultaneously for V_{Ref} capture, a significant kickback on the ramp may occur. To avoid this, buffers were introduced in between the ramp reference and the input of the comparators. A buffer is placed every 64 columns uniformly distributed across the readout block.

Another important aspect is the comparator design. For the specific design, a trade-off between speed, stability, mismatch and propagation delay was considered. The key elements to be considered crucial are mismatch and stability over a wide input

range, meaning that the propagation delay was on purpose longer than most of the designs. The specific of this design was to allow around 500ns propagation delay in a line time of 32 µs. In high-speed designs, this can be problematic. In this architecture, as the comparator is used to start and stop the respective counter operation, it can be accepted since the delay is removed by operation and the ramp slope and counter operation can accommodate the time reduction, as long as the delay does not vary significantly with the input voltage. The input devices of the comparator were designed with a relatively large W and L, to reduce mismatch.

The reference clock of the counters is the same for both reducing the jitter and phase delay addition to the conversion.

Another consideration is the addition/subtractor block. To keep this block simple an intentional offset voltage was added to the sample and hold block. In this way, one can keep the signal value always a bit higher than the reset value when the exposure is performed in absolute darkness, resulting in a positive digital output from the subtraction operation, simplifying the subtraction logic.

Results

Preliminary results have been obtained from the recently received prototypes of the device. Figure 6 shows the first measurements of the INL and DNL of the ADC when operating in 10-bit mode.

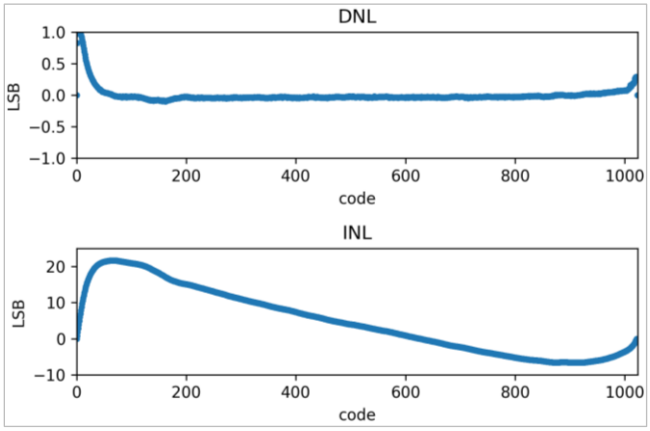

Figure 6. *INL and DNL first results of the prototype with the proposed ADC at 10-bit mode.*

The DNL figure is quite good with levels lower than 0.5LSB when the DN code is higher than 30DN. The reason for high DNL at very low light values is still unclear but the team believed that was a measurement setup fault since other measurements at dark and low light conditions do not show non-linearities.

The INL is yet larger than originally expected, however, we are in the early stage of the evaluation missing the settings optimization of the sensor and ADC operation. On the other hand for imaging applications the INL has a lower impact compared to other applications since the source follower is present in the pixels also has a non-linear response, making the ADC INL less relevant regarding the overall image quality.

Figure 7 shows crop and tiled images of the sensor being illuminated with uniform illumination and in different exposure settings. It is clear that the row noise is not visible in those sample images, meaning that the ADC with CDS operation is performing the noise reduction as expected.

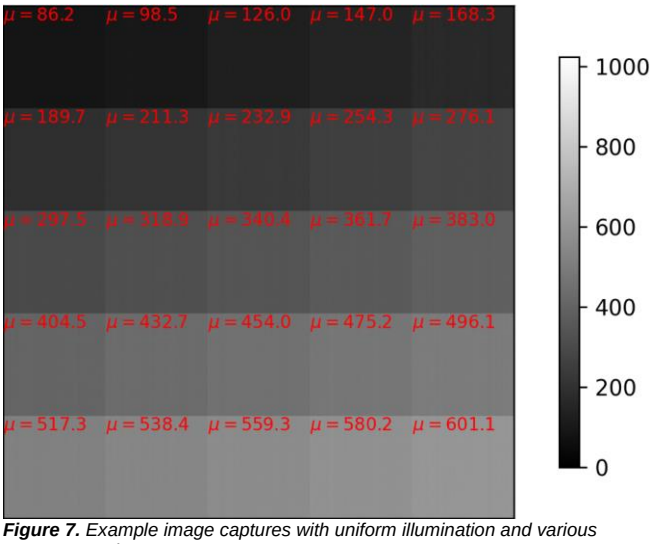

Figure 7. *Example image captures with uniform illumination and various exposure settings.*

At the moment of the publication of this article, a proper device characterization is being performed on the prototype device and a settings optimization is yet to be carried out. However, the proposed ADC design is performing as expected, delivering the row and column noise reduction according to the project expectations.

Conclusions

The proposed ADC architecture can deliver speed, good power efficiency, simple implementation and good row noise reduction compared to other solutions presented.

This ADC architecture was successfully designed and implemented in a device prototype with a significant matrix size to validate the implementation.

Thanks to the CDS operation, the readout noise reduction is effectively made.

The preliminary results show to be promising but a proper optimization needs to be carried out to fully understand the limitations and performance of this architecture in this specific design.

References

[1] K. Chen, M. Afgani, P. E. Danielsson and C. Svensson, “PASIC: A processor-A/D converter-sensor integrated circuit,” in *Int. Symp. On Circuits and Systems, pp. 1705-1708*, New-Orleans, LA, May 1-3, 1990.

[2] M. H. White, D. R. Lampe, F. C. Blaha and I. A. Mack, "Characterization of surface channel CCD image arrays at low light levels," in *IEEE Journal of Solid-State Circuits*, vol. 9, no. 1, pp. 1-12, Feb. 1974, doi: 10.1109/JSSC.1974.1050448.

[3] A. Theuwissen and G. Meynants, Welcome to the World of Single-Slope Column-Level Analog-to-Digital Converters for CMOS Image Sensors, now, 2021.

[4] X. Wang, J. Bogaerts, G. Vanhorebeek, K. Ruythoren, B. Ceulemans, G. Lapage, P. Willems and G. Meynants, “A 2.2 M CMOS image

sensor for high speed machine vision applications," in *Proc. SPIE, vol. 7536*, DOI: 10.1117/12.838880, 2010.

[5] J. Bogaerts, K. Ruythooren, A. Gvozdenovic, K. Van Esbroeck, B. Ceulemans, W. Ogiers, G. Arsinte, X. Wang and G. Meynants, High Speed 36 Gbps 12Mpixel global pipelined shutter CMOS image sensor with CDS, IISW WORKSHOP 2011, 2011.

[6] Y. Degerli, F. Lavernhe, P. Magnan and J. Farré, Non-stationary noise responses of some fully differential on-chip readout circuits suitable for CMOS image sensors, IEEE Transactions On Circuits And Systems—II: Analog And Digital Signal Processing, Vol. 46, No. 12, December 1999.

[7] S. Yoshihara, Y. Nitta, M. Kikuchi, K. Koseki, Y. Ito, Y. Inada, S. Kuramochi, H. Wakabayashi, M. Okano, H. Kuriyama, J. Inutsuka, A. Tajima, . T. Nakajima, Y. Kudoh, F. Koga, Y. Kasagi, S. Watanabe and T. Nomoto, A 1/1.8-inch 6.4 MPixel 60 frames/s CMOS Image, IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 41, NO. 12, December 2006.

[8] G. Meynants, J. Bogaerts, B. Wolfs, B. Ceulemans, T. DeRidder, A. Gvozdenovic, E. Gillisjans, X. Salmon and G. VandeVelde, 24 MPixel 36 x 24 mm2 14 bit image sensor in 110/90 nm CMOS technology, IISW WORKSHOP 2013, 2013.

[9] J.-P. Carrère, S. Place, J.-P. Oddou, D. Benoit and F. Roy, CMOS image sensor: Process impact on dark current, Waikoloa, HI, USA: 2014 IEEE International Reliability Physics Symposium, 01-05 June 2014.

Author Biography

Pedro Santos received his degree (2005) from University of Aveiro, and his M.Sc. (2013) from University of Madeira. In 2007, he joined Awaiba (Funchal) as an electronic engineer, developing analog and mixed-signal designs for CMOS image sensors focused on industrial and medical markets. In 2012 he became characterization team leader and in 2015 team manager after AMS acquisition. In 2022 he started a PhD in Radiation tolerant CMOS imagers at KU Leuven being currently a research assistant in the ADVISE research group, Campus Geel.

Idham Hafizh received his M.Sc. (2017) and Ph.D. (2020) from Politecnico di Milano, Italy. In 2021, he joined KU Leuven, Belgium, as a postdoctoral research assistant in the Advanced Integrated Sensing (ADVISE) research group, located in Campus Geel. His current research interests includes the development of image sensor pixels and their subsequent readout schemes.

Jeffrey Prinzie received his M.Sc. (2013) and Ph.D. (2017) and post-doctoral from KU Leuven, where in 2020 he became Assistant Professor. During his Ph.D., he worked in radiation tolerant ICs within the ADVISE research group (ESAT) KU Leuven and in collaboration with CERN. His main interests are radiation hard time-based mixed-signal circuits, (PLLs, TDCs and radiation sensors). Today, he is focusing on highly digital integrated circuits in collaboration and founding of CERN, ESA and FWO.

Paul Leroux received his M.Sc. (1999) and Ph.D. (2004) in electronic engineering from KU Leuven. He was Research Assistant (1999-2004) within MICAS(ESAT) research group. He founded the ADVISE research lab and since 2016 has been Chair of KU Leuven, Geel Campus. His focus is radiation hardened analog and mixed-signal IC design. He is the director of RADMEP project and the joint KU Leuven and SCK-CEN. Paul Leroux has (co)authored over 250 papers in international journals and conference proceedings and Senior Member of IEEE.

Guy Meynants received his M.Sc.(1994) and Ph.D.(1998) in electronic engineering from KU Leuven. He is an expert on CMOS image sensors, invented 33 patents and patent applications in the field of image sensors and analog circuit design, and co-authored 70 scientific publications. He has wide work experience: IMEC(1994), cofounder of FillFactory (2000), co-founder and CTO of CMOSIS(2007), and director at Photolitics(2019). He designed various CMOS image sensors for industrial, photography and space applications. Since 2021, Guy is professor at KU Leuven. He is a board member of the International Image Sensor Society.