https://doi.org/10.2352/EI.2023.35.6.ISS-328

The Simulation and Design of a Burst Mode 20Mfps Global Shutter High Conversion Gain CMOS Image Sensor in a Standard 180nm CMOS Image Sensor Process Using Sequential Transfer Gates

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Abstract

A sequential transfer-gate and photodiode optimization method for CMOS image sensors is described in this paper. This technique enables the design of large-scale, ultra-high speed, burst mode CMOS image sensors (CIS) through a low-cost, standard CMOS image sensor process without the need for process customization or an advanced CIS process. Additionally, sequential transfer gates show a clear advantage by minimizing the floating diffusion capacitance and improving image sensor conversion gain in large-scale pixels. The simulation results further establish that full charge transfer can be achieved within 12ns for a 20μm test pixel.

Introduction

Ultra-high speed (UHS) image sensors are widely used in scientific and industrial applications to elucidate the UHS phenomena, such as high-energy X-ray imaging. In recent years, a few published papers have reported the frame rates of burst mode UHS image sensors in the range of millions of frames per second (Mfps) [1,8]. However, these published works required either an advanced process, for example, 110nm front-side-illuminated (FSI) or 130nm back-side-illuminated (BSI) charge-coupled-device (CCD) or a process specifically customized to design and fabricate UHS image sensors, as shown in Table 2. This research has been conducted after the outbreak of COVID-19 when access to advanced technology or a customized process is extremely challenging. Therefore, a design method has been implemented in this study to push beyond process limitations to achieve high-speed charge transfer and high conversion gain based on a standard 180nm process.

As [9] points out, there could be a few bandwidth bottlenecks in high-speed image sensor designs. However, for burst-mode image sensors, incident image information is first stored in in-pixel memories (sample and hold capacitors) and then read out from the memories slowly. Therefore, in-pixel circuit readout time is greatly reduced, and the pixel charge transfer time eventually dominates the burst mode image sensor frame rate. It is widely accepted [14] that quick charge transfer time can be achieved with a strong electric field. [10-11] analytically describe the relationships between electrostatic potential and photodiode width for small-size pixels (the short-photodiode effect). [12, 17] utilized the above effect and created an electric field along the electron transfer path in the photodiode to achieve fast charge transfer without process modification; however, for this photodiode design, the fill factor is limited. [13] extended the above idea to a multi-finger pixel and achieved about 50ns charge transfer time for large-scale pixels. However, due to a wide transfer gate and a large floating diffusion area, as is shown in Figure 1, this design suffered a low conversation gain and high capacitive transfer-gate loading. Technology computer-aided design (TCAD) simulation shows that for a 20μm pitch pixel, the pixel has a conversion gain (CG) less than 10μv/e- (Figure 1).

To balance the recording length and frame rate for a burst mode image sensor, the capacitance of the in-pixel sample and hold capacitor is usually limited to a few tens of femtofarads (fF), for example, a 50fF per capacitor in [1]. The small capacitor's kT/C noise contributes significantly to the total input referred noise at the floating diffusion node with a small conversion gain. Based on the information reported, input referred noise is calculated to be 85e- and 167e- for [7] and [8], respectively. [6] introduced a passive CDS amplifier to reduce the input-referred noise and reported the lowest state-of-art noise number at 8.4e-, as shown in Table 2. The gain of the passive CDS amplifier is determined by the capacitance ratio of the NMOS capacitor at depletion mode versus inversion mode, which is process and voltage dependent and introduces unavoidable non-linearity to the entire image sensor on the order of 3% [6]. Furthermore, the settling of the amplified voltage also limited the frame rate of the burst mode image sensor. Therefore, a process-independent method is needed to reduce the input-referred noise and to maintain the fast charge transfer and high frame rate.

Charge Transfer Time Optimization

Figure 2 shows a simplified photodiode cross-section. Considering the short photodiode effect and applying the 1-D Poisson equation along the red dashed line, the maximum electrostatic potential in the photodiode is given by:

$$\psi_{max} \approx \frac{q \cdot N_D \cdot X_n^2}{2 \cdot \varepsilon_0 \cdot \varepsilon_r}\left(1 + \frac{N_D}{N_A}\right) \quad (1)$$

where ψ is the electrostatic potential in the photodiode, q is the elementary charge, N_D is the doping concentration of the photodiode, and N_A is the doping concentration of the substrate. Without modifying the doping concentration of the photodiode and substrate, X_n, the photodiode half width (half depletion width), is the only parameter to vary to form an electric field. Assuming the electric field is constant, the photodiode geometry shape is given by:

$$y = -\frac{q \cdot N_D \cdot X_n^2}{2 \cdot E \cdot \varepsilon_0 \cdot \varepsilon_r}\left(1 + \frac{N_D}{N_A}\right) + C_0 \quad (2)$$

where y and X_n are the photodiode coordinates. Plugging in the process parameters and setting the electric field in the photodiode along the charge transfer direction varies from 400V/cm to 900V/cm, one can obtain different photodiode geometry shapes, as is plotted in Figure 3. Simple TCAD pixel models with different photodiode shapes are used to simulate electron transfer time, as Figure 4 shows. The metal shielding over the photodiode creates an aperture and forces incident light to only illuminate the tip of the photodiode so that photo-generated electrons will travel through the longest path in the photodiodes to the FD node. TCAD simulation results of the charge transfer time of different photodiodes are listed in Table 1. The EConstant_800V/cm photodiode design is used in the proposed pixel design to balance the charge transfer time and fill factor tradeoff, as is displayed in Figure 5.

TX1, TX2, and TX3 in Figure 5 represent the three sequential transfer gates. Its operational timing is shown in Figure 6, where the red, green, blue, and cyan curves stand for the voltage of TX1, TX2, TX3, and floating diffusion, respectively. The yellow and gray represent the total number of electrons in the upper and lower photodiode. At the beginning of charge transfer, TX1, TX2, and TX3 all turn on simultaneously, where TX1's voltage is higher than TX2's, and TX2's voltage is higher than TX3's. At the end of the charge transfer, TX3 turns off first, followed by TX2, and eventually, by TX1. The TCAD transient simulation shows that charges can be fully transferred within 12 ns.

Conversion Gain and Noise Optimization

Compared to the baseline pixel in [13], the floating diffusion area in this design can be significantly decreased, as the Figure 5 red box shows. Additionally, unlike the traditional pixel, the proposed pixel does not directly transfer photoelectrons from the photodiode to the floating diffusion (FD) node. Therefore, it is safe to move the TX1 gate away from the floating diffusion node, as is illustrated in the cross-section in Figure 7, which effectively reduces the overlap capacitance between FD and TX1 gates and reduces dark current due to gate-induced-drain-leakage (DIGL) at floating diffusion node, and increases the conversion gain. The TCAD transient simulation in Figure 6 shows that conversion gain is calculated to be 138μv/e-.

In order to further reduce the input-referred noise, a correlated-double-sampling (CDS) circuit is implemented in the pixel, as figure 7 shows, where the AC coupling cap between the first source-follower (SF) and second SF takes the voltage difference of pixel reset voltage and signal voltage and store it on the in-pixel sample and hold (S/H) capacitors. In total, 108 S/H capacitors were laid out in 52.8um pitch. The theoretical calculation and simulation yield only 5.6e- input referred noise is achieved at the FD node, much smaller than the 8.4e- noise reported in [6].

Conclusions and Future Work

A 20Mfps global-shutter burst mode CMOS image sensor with 5.6e- input-referred noise and 108 frame recording length was designed and simulated in a standard 180nm FSI process. By carefully optimizing the photodiode shape and introducing the sequential transfer gates, complete charge transfer was achieved within 12 ns. Additionally, the sequential transfer gate showed a clear advantage in minimizing the floating diffusion area, reducing the floating diffusion capacitance, and improving conversion gain. The sensor has been taped out, and sample dies are expected to return from the foundry in March 2023, with the characterization following receipt.

One of this design's applications is to enable the viewing of the dynamic response of materials under different stresses. Videos with millions of frames per second capturing the changes under a bright X-ray source will give an insight into the properties of the material under study, which may yield potential improvements to the material. This design is phase three of a series of projects. In phase one [16,18], we have demonstrated that the high energy X-ray (20-50Kev) quantum efficiency (QE) of a sensor designed in the same standard process can be increased by >10x with a Photon-Attenuation-Layer (PAL) deposited on top of the sensor. Therefore, the deposition of PAL onto this high-speed burst mode sensor will also be scheduled after the characterization.

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Acknowledgments

The authors are grateful to Jeph Wang and Bob Reinovsky from Los Alamos National Laboratory and Department of Energy for sponsoring this research (Contract No. 89233218CNA000001), Xuezhou Cao, Guang Yang, Jifeng Liu for discussion, and X-Fab for fabrication of this sensor.

Author Biography

Xin Yue received his Bachelor of Science from the Wuhan University of Technology (2011) and his Master of Science from the University of Southern California (2013). He was employed as a staff mixed-signal circuit design engineer at Forza Silicon, CA, for 7 years. Currently, he is pursuing his Ph.D. in engineering sciences from Dartmouth College. His work predominantly focuses on ultra-high speed, low noise, and advanced image sensor design.

Figures and Tables

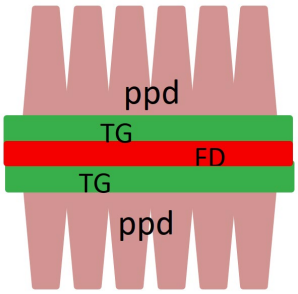

Figure 1. *High speed pixel layout of [13]*

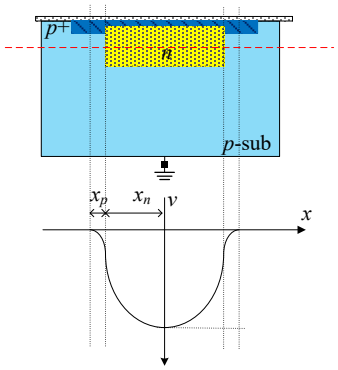

Figure 2*. A simplified pinned photodiode*

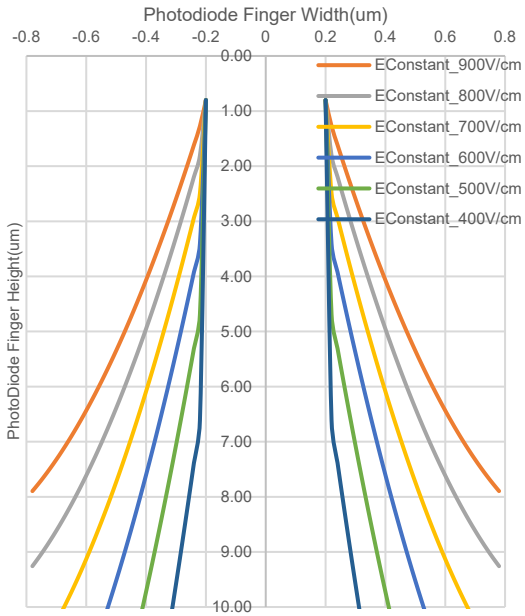

Figure 3*. Photodiode fingers with different electric field*

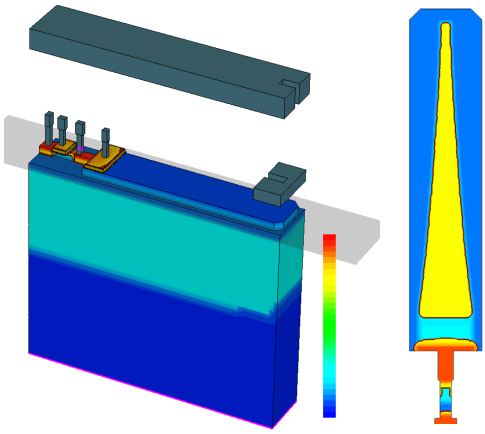

Figure 4. *TCAD model of sample pixel (right) and its cut-plane(left)*

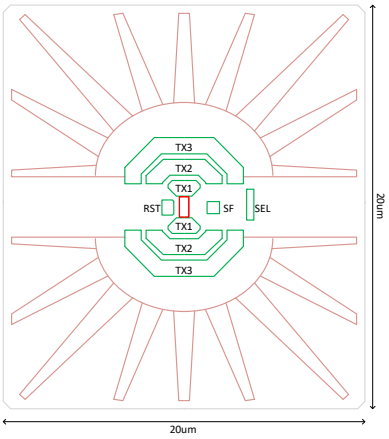

Figure 5. *High speed pixel core layout*

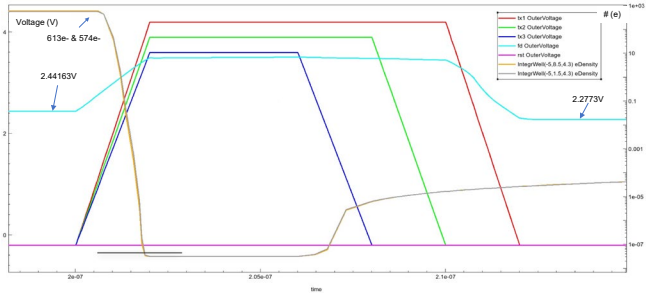

Figure 6. *Transient TCAD simulation of charge transfer*

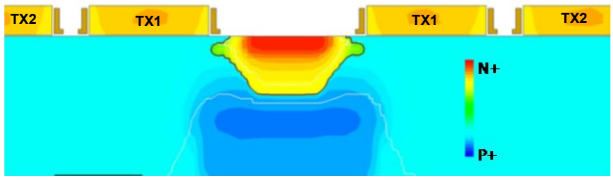

Figure 7. *Cross-section of the low capacitance floating diffusion*

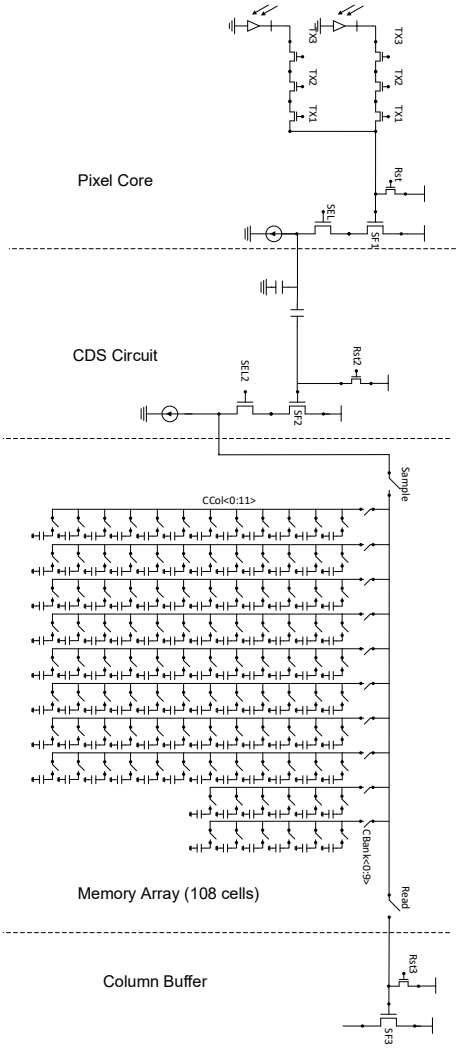

Figure 8. *High-speed high conversion gain pixel schematic*

Charge Transfer Time of Different Photodiodes					
CTE	90%	99%	99.5%	99.9%	Unit
Econstant_400	10.2	41.2	51.3	75.2	ns
Econstant_500	0.67	17.4	25.8	47.0	ns
Econstant_600	0.67	5.01	11.0	28.3	ns
Econstant_700	0.74	1.51	5.16	19.3	ns
Econstant_800	0.82	1.18	3.78	15.5	ns

Table 1. *Charge transfer time of different photodiode designs*

Performace Comparasion Between SOAs									
Ref	Process (nm)	Process Customization	Pixel Size	CG (uV/e-)	FWC (Ke-)	Frame Rate (Mfps)	Record Length	Noise (e-)	DR (dB)
[1] 2019	180 FSI	Yes	35*70	99	11	100	368	N/R	N/R
[2] 2013	180 FSI	Yes	32*32	74	N/R	10	128	N/R	N/R
[3] 2017	180 FSI	Yes	32*32	112	10	10	480	N/R	N/R
[4] 2018	130 BSI CCD	Yes	72.5*72.5	N/R	N/R	25	1220	N/R	N/R
[5] 2019	130 BSI CCD	Yes	12.7*12.7	N/R	7	100	5	N/R	N/R
[6] 2018	130 BSI	N/R	30*30	105	6	20	108	8.4	57
[7] 2022	110 FSI	Yes	22.4*22.4	32	33	303	12	85	51
[8] 2016	110 FSI	Yes	11.2*5.6	N/R	10	200	15	>167	30
This Work 2022	180 FSI	No	52.8*52.8	138	8	>20	108	5.6	>62

Table 2. *Performance comparison between SOAs*