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A 2.2µm three-wafer stacked back side illuminated voltage domain global shutter CMOS image sensor

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Abstract

We developed a 2.2µm pixel pitch Back Side Illuminated (BSI) Voltage Domain Global Shutter (VDGS) image sensor with the three-wafer stacked technology. Each wafer is connected by Stacked Pixel Level Connection (SPLC) and the middle and logic wafers are connected using a Back side Through Silicon Via (BTSV). The separation of the sensing, charge storage, and logic functions to different wafers allows process optimization in each wafer, improving overall chip performance. The peripheral circuit region is reduced by 75% compared to the previous product [1] without degrading image sensor performance.

Introduction

Due to the emergence of machine vision, augmented reality (AR), virtual reality (VR), and automotive connectivity in recent years, the necessity for chip miniaturization has grown. These emerging, next-generation applications, which are centered on user experience and comfort, require their constituent chips, devices, and parts to be smaller, lighter, and more accessible. AR/VR applications, especially demand smaller components due to their primary application towards wearable technology, in which the user experience would be negatively impacted by large features and bulk. Therefore, chips and devices intended for next-generation consumer applications must be small and modular, to support module miniaturization and promote user comfort.

For next-generation image sensors, new strategies must be implemented to facilitate chip miniaturization. Our 1st generation Voltage Domain Global Shutter (VDGS) image sensors are fabricated using 2-Layer pixel technology. The Application Specific Integrated Circuit (ASIC) in a two-wafer stacked chip is relegated to the periphery, posing additional challenges to scalability. Therefore, chip size reduction is difficult in existing 2-Layer pixel stacked image sensors.

To enable the chip miniaturization required for technological advancement and innovation, we developed a three-wafer stacked VDGS image sensor, presented in this work. The addition of a third wafer in the three-wafer stacking scheme also facilitates chip size decrease by rearranging circuitry elements to conserve space. As shown in Figure 1, a significant portion of the space in a two-wafer stacked VDGS chip is not optimized for sensing. By relocating logic components in the middle wafer to the bottom wafer, redundant space outside the array is reduced in the entire stack, simultaneously increasing the fill factor of the pixel array.

In this work, we combined the space efficiency of the three-wafer stacked technology with the performance of global shutter, and successfully developed a Back Side Illuminated (BSI) VDGS device with the smallest chip size reported in literature so far. The final peripheral area size of our three-stacked sensor is 75% smaller than a conventional stacked sensor [1] with comparable performance. The development and performance of this sensor are described in the following sections.

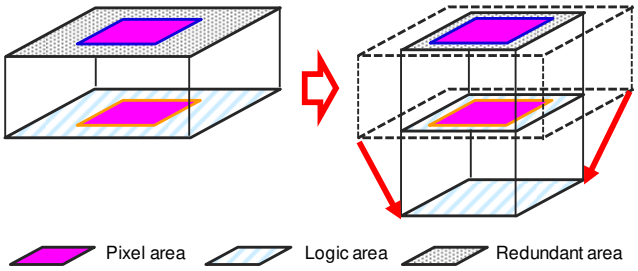

Figure 1. Peripheral shrinkage from two-wafer stack (Left) to three-wafer (Right)

Device Structure and Architecture

Figure. 2 shows a cross section of the three-wafer stacked BSI image sensor structure. The sensor wafer is located at the top, and contains the photodiode (PD) array, which includes the PD itself, as well as a Transfer Gate (TG), a Floating Diffusion (FD), a Reset Transistor (RST), a Dual Conversion Gain transistor (DCG), a 1st stage Source Follower (SF1), and a Global Shutter switch transistor (GS). In our device, the sensor wafer is thicker, enhancing Near-Infrared (NIR) sensitivity. Full depth Deep Trench Isolation (DTI) is implemented, providing complete pixel isolation and rendering high NIR light Modulation Transfer Function (MTF) performance.

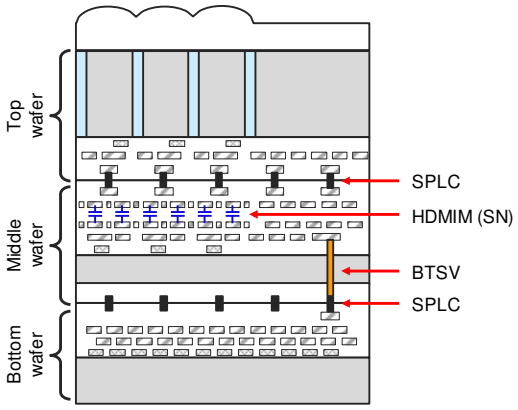

Figure 2. Cross section of three-wafer stacked structure

The middle wafer contains sensing components, including a Storage Node (SN) which uses a High Density (HD) Metal-

Insulator-Metal (MIM) capacitor to store signals. The top and middle wafers are connected via Stacked Pixel Level Connection (SPLC) at the pixel level, connecting the PD and SN at each pixel (Figure 2). All metal layers, including HDMIM capacitors, are placed between the top wafer and the middle wafer to insulate the SN from parasitic light leakage, therefore achieving higher Shutter Efficiency (SE). Additionally, the middle wafer includes a bias transistor (bias), two SWitch transistors (SWrst, SWsig), two SN Capacitors (Crst, Csig), two 2nd stage Source Followers (SF2), and two 2nd Row Select transistors (RS). The pixel schematic of the three-wafer stacked VDGS sensor is shown in Figure 3. Due to the relegation of additional pixel circuitry to the middle wafer, the sensor wafer contains only the PD array, making it possible to reduce pixel size to 2.2um, resulting in high fill factor and full well capacity (FWC) > 12,000e-. Thus, the sensor architecture is compatible with the previous generation two-wafer stack VDGS image sensor [1].

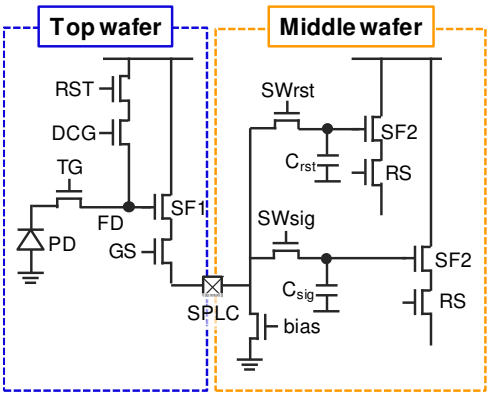

Figure 3. Schematic of the voltage domain global shutter pixel

The bottommost wafer contains the ASIC components, which are connected to the middle wafer using a Back side Through Silicon Via (BTSV) in a face-to-back configuration (Figure 2), facilitating signal transfer from SN to ASIC. Existing three-wafer stack technologies only use Through Silicon Via (TSV) to connect the wafers [2], which limits chip size shrinkage due to the necessity of a Keep-Out Zone (KOZ) (Figure 4). As BTSV process on the middle wafer requires much smaller KOZ, our proposed structure better facilitates peripheral region reduction and chip size shrinkage comparable to two-wafer stacked technology [3].

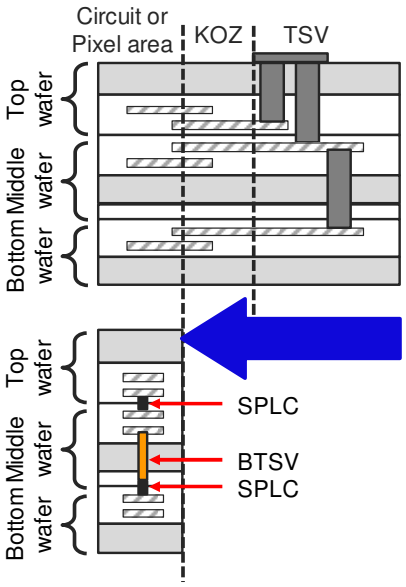

Figure 4. KOZ and TSV (conventional, top), and SPLC with BTSV (our work, bottom)

In addition to chip size miniaturization, three-wafer stack technology facilitates process optimization and cost reduction. In three-wafer stacked image sensors, image sensing, charge storage, and ASIC functionality are separated into dedicated wafers, allowing fabrication processes to be customized for each specific purpose. The top, sensor wafer can withstand more thermal processing, specific BSI processes, and other procedures to improve optical and electrical performance, without considering the impact of these processes on the circuitry. In our device, the backside of the sensor wafer is treated with IR enhancement processes [4], which boosts NIR Quantum Efficiency (QE). Additionally, the middle wafer can be separately optimized for cost (less metallization, lower-cost metals) and pixel circuit performance (low noise, integration of specific devices such as HDMIM). The logic wafer can be independently processed based on functionality, such as low power consumption, high speed, or embedded devices (e.g.: memory). The separation of processes for each wafer in the stack allows the optimization of the overall device performance.

Although separate wafer processing in the three-wafer stack technology may increase the total wafer consumption, the relative cost is only increased for larger chip sizes. The cost benefit of three-wafer stack chip is enhanced in small area sensor with reduced array size compared to two-wafer stack technology (Figure 5). Thus, the cost of the three-wafer stack technology is manageable for consumer applications with smaller chip size.

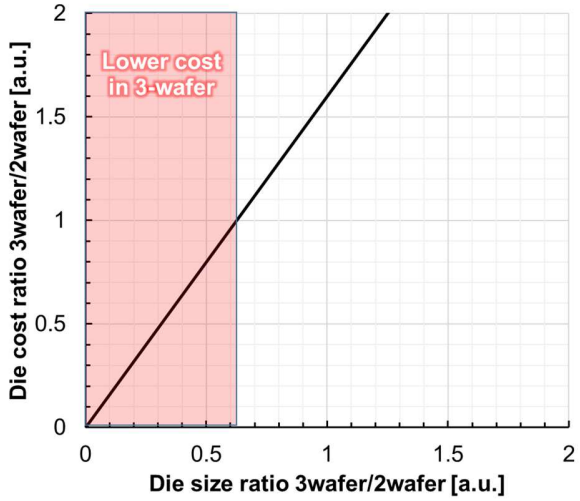

Figure 5. Die dost trade-off for 2wafer or 3wafer

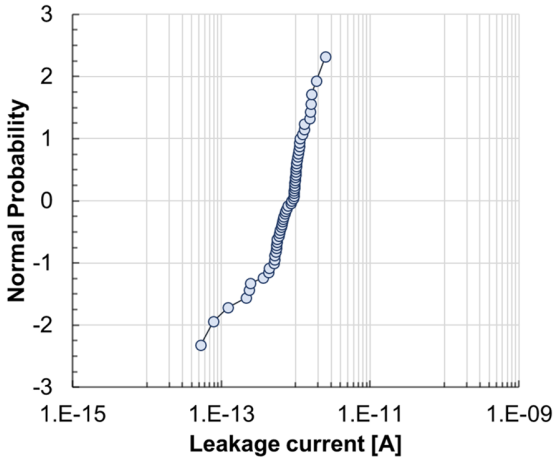

Figure 7. Normal probability plot of leakage current between BTSV and Si

Measurement Result

BTSV characteristics

The electrical properties of BTSV were investigated using a test module. Figure 6 shows the resistance distributions of the chain module. The pitch of the adjacent BTSV connection is 2.2µm, and the number of connections is 2.5kea. The solid circles are the resistance per BTSV in the chain. The tight distribution shown by this device confirms good connectivity between the stacked wafers.

Figure 7 shows the leakage current measurement result. The 2.5kea connections of BTSV are located in the module. The leakage current is well suppressed and maintained under 10pA.

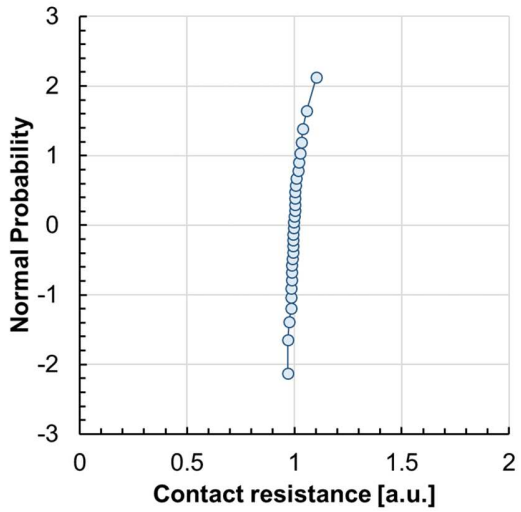

Figure 6. Normal probability plot of BTSV contact resistance

Shutter Efficiency

Figure 8 illustrates SE performance of the 2.2µm VDGS CIS (this work) under 940nm light condition. The dark region between blades appears completely black. VDGS CIS demonstrated in this work achieved over 100dB SE making it the smallest pixel pitch device with the highest SE (Table 1).

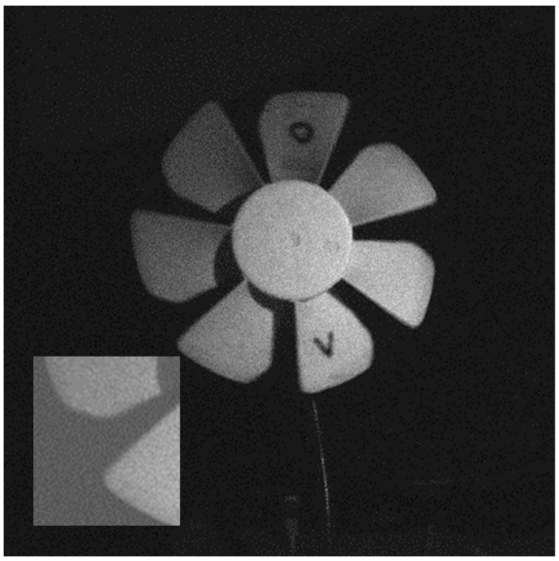

Figure 8. Captured image with GS operation. Integration time=0.379msec; 240fps; F2.8

Table 1. Comparison of CIS performance

	This work	IEDM 2019 [1]	IISW 2021 [5]	ISSCC 2020 [6]	IEDM 2020 [7]	ISSCC 2019 [8]	IEDM 2018 [9]
Pixel pitch	2.2μm	2.2μm	4.95μm	2.3μm	4.6μm	2.7μm	2.74μm
Device structure	3-wafer stacked BSI	Stacked BSI	Stacked BSI	Stacked BSI	Stacked BSI	Stacked BSI	BSI
GS type	Voltage Domain	Voltage Domain	Voltage Domain	Voltage Domain	Voltage Domain	Voltage Domain	Charge Domain
FWC	12 ke^-	12 ke^-@LCG	14 ke^-	12 ke^-@LCG 6 ke^-@HCG	3.8k(PD)/51k(FD) /9M(TTS)	10 ke^-	10 ke^-
Shutter Efficiency (PLS)	< -100 dB	< -100dB	-	-85dB	-55dB < -140dB (Mem/PD)	-86dB	-80dB
RN	3.1 e^-	3.1 e^-	2.6 e^-	2.1 e^-	4.2e-	3.5 e^-	1.85 e^-
QE@940nm	36%	38%	-	42%	42%	36%	-
Sensitivity	37.5 ke^-/lux.s	35 ke^-/lux.s	-	18 ke^-/lux.s	108 ke^-/lux.s	5000 mV/lux.s	23.9 ke^-/lux.s

Quantum Efficiency and MTF

In this work, the sensor wafer, which is a thick silicon, is treated with IR enhancement processes, yielding high NIR QE (Figure 9), and the MTF in NIR light (Figure 10) is comparable with the previous sensor. The half Nyquist frequency (Ny/2) at 940nm demonstrated 58%. Full depth DTI reduces both the electrical and the optical cross talk among adjacent pixels.

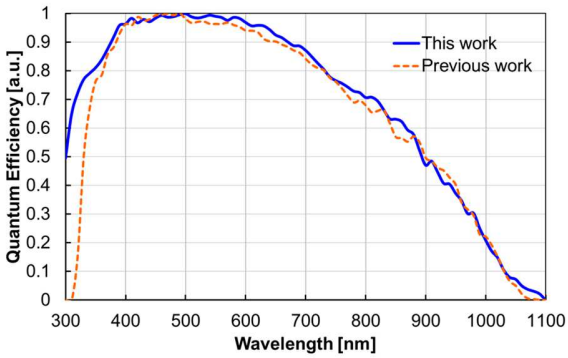

Figure 9. QE curve comparison with the previous work [1]

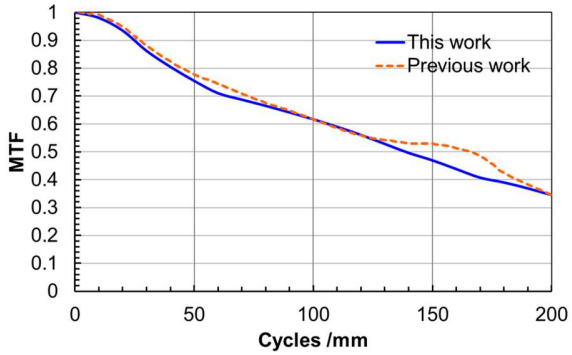

Figure 10. MTF comparison with the previous work [1]

Pixel performance

In this work, the storage nodes located in the middle wafer are processed with the standard logic process. The pixel performance summary (Table. 2) shows an adequate random noise performance and fixed pattern noise. The random noise mainly originates from the storage node, while the HDMIM capacitor helps to reduce the temporal noise. As shown in Table. 1, this sensor demonstrates the same performance as the previous generation two-wafer stack sensor despite subjecting the sensor wafer to additional thermal and PD-specific processes in the sensor wafer.

Table 2. Pixel performance summary

Parameter	Value
Pixel pitch	2.2μm x 2.2μm
GS mode	V-domain
Process Technology	45nm sensor/65nm logic/40nm logic 3-wafer stacked BSI
CG	Dual CG : 67/256 μV/e^-
FWC	3500 e^-/ 12000 e^-
Effective Shutter Efficiency@940nm	< -100 dB
RN	3.1 e^-
FPN	1.8 e^-
PRNU	0.6%
QE @940nm/850nm	36%/57%
MTF@940nm, Ny/2	58%
Sensitivity @940nm	82500 e-/μW.cm^2.sec

Conclusions

We developed a three-wafer stacked VDGS CMOS image sensor, which is presented in this work. This sensor relegates a part of the logic area from the pixel wafers to a dedicated ASIC wafer at the bottom of the wafer stack, thus increasing effective pixel area while reducing chip size. The utility of a highly robust BTSV enhances circuit design flexibility and reduces chip size. As a result, the peripheral circuit region is reduced by 75% compared to the previous product, while maintaining the image sensor performance of previous generation two-wafer stack VDGS.

Acknowledgment

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Author Biography

Shimpei Fukuoka received his BS in electronics from Tokyo University of Agriculture and Technology (2009). Since 2021, he has worked in the Research and Development at OMNIVISION in Japan. His work has focus on the development of image sensor and the process integration.