

3-Layer Stacked Pixel-Parallel CMOS Image Sensors Using Hybrid Bonding of SOI Wafers

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Abstract

We report 3-layer stacked pixel-parallel CMOS image sensors developed for the first time. The hybrid bonding of silicon-on-insulator wafers through damascened Au electrodes in a SiO₂ insulator on the front and backside realizes both face-to-face and face-to-back bonding, developing a multi-layer stacked device. A 3-layered pixel circuit is developed to confirm the linear response of 16-bit digital signal output. A prototype sensor with 160 × 120 pixels successfully captures video images, demonstrating the feasibility of multi-layered sensors of high performance as well as multi-functions including signal processing, memory, and computing for applications such as high-quality video cameras, measurements, recognition, robots, and various IoT devices.

Introduction

Image sensors have improved performances including resolution and frame rate to meet the escalating demand of high-quality video systems such as ultra-high-definition television and three-dimensional (3D) imaging. Stacked sensors have been technology boosters to reduce the pixel size, increase the number of parallelism for signal processing, and add various functionalities. Stacked sensors use the through-silicon via (TSV) technology in the early stages [1-3]. Although a 3-layer stacked sensor has been reported [3], signal processing is limited to column-parallel because no TSV can be integrated inside pixels due to their dimensions. Recently, the hybrid bonding technology for pixel-

wise interconnection has been utilized, realizing pixel-parallel signal processing [4-5] for further functionality. However, the conventional hybrid-bonded sensor is only a 2-layer stacked one because the wafer should be bonded face-to-face, limiting the degree of freedom in sensor design. To overcome this problem, we have proposed a 3D integration technology using Au/SiO₂ hybrid bonding of silicon-on-insulator (SOI) wafers (Figure 1) [6]. The adoption of SOI wafers allows the face-to-back bonding in the same manner as the face-to-face bonding; electrodes on the backside of a device layer are formed after the handle layer removal, enabling more than three layers to be stacked with pixel-wise interconnection.

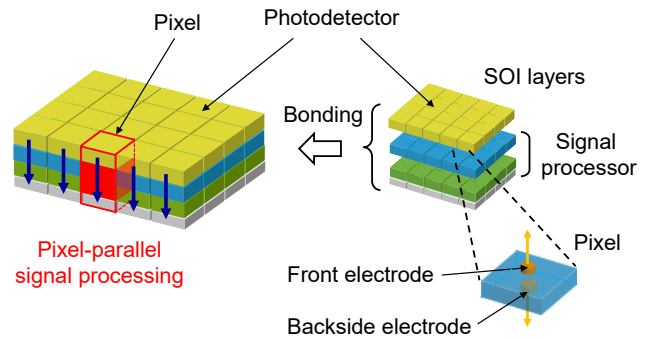
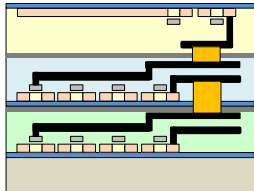
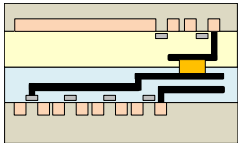
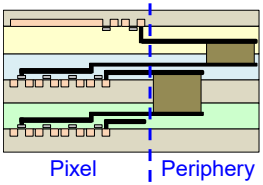


Figure 1. Schematic diagram of 3D integrated technology using SOI wafers.

Table 1: Schematics of stacked image sensors and their technology features.

	(a) This work	(b) Refs. [4-5]	(c) Refs. [1-3]
			
Technology feature	Hybrid bonding of SOI	Hybrid bonding	TSV
Bonding orientation	Face-to-face and Face-to-back	Face-to-face	Face-to-face and/or Face-to-back
Number of layers	3	2	2-3
Parallel of processing	Pixel-parallel	Pixel-parallel	Column-parallel

The diagram illustrates the architecture of a 16-bit digital photodetector. It is divided into three main sections: the Upper layer, the Middle layer, and the Lower layer. The Upper layer includes a photodiode (PD) and a feedback capacitor (FD) connected to an inverting amplifier. The amplifier's output, V_{OUT} , is fed back to the PD and also serves as the input to a 16-bit counter. The counter is composed of four 4-bit counters, with the first and third counters labeled 'Counter 1st bit' and 'Counter 16th bit' respectively. The counter's output is split into three 8-bit segments: 'Lower 8 bits', 'Middle 8 bits', and 'Lower 8 bits'. A pulse generation circuit, consisting of a pulse generator and a delay element, is connected to the counter's input. The output of the counter is connected to the output of the circuit. The diagram also shows the input voltage V_{RST} and the output voltage V_{OUT} .

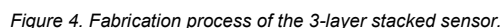
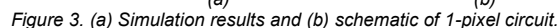
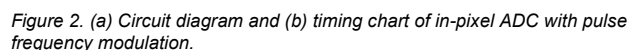


Figure 2 shows a pixel circuit diagram including a PD, a pulse generation circuit, and counters, comprising an in-pixel ADC with a pulse frequency modulation [7]. Whenever the floating diffusion (FD) potential (V_{FD}) reaches the threshold voltage (V_{TH}) of the comparator, a pulse is generated, resulting in pulse numbers corresponding to the illuminance to be stored in the counters. Schematic and SPICE simulation results are shown in Figure 3. The upper and lower bits of the 16-bit counters are split into the middle and lower layers to reduce the pixel size.

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The developed sensor chip is shown in Figure 5. The pixel size was $39\text{ }\mu\text{m}$ square made by the $0.2\text{-}\mu\text{m}$ FDSOI logic process; owing to the 16-bit-counter circuit distributed in two layers, the pixel size reduced to 52% of the previous 2-layered sensor [10]. The PD was dedicatedly designed to work in the 50-nm thick device layer. The chip size was 20 mm square. We confirmed no delamination of wafers even after grinding of the handle layer and chip dicing.

A cross-sectional scanning electron microscope (SEM) image of the 3-layer stacked sensor is shown in Figure 6. We observed no void or separation at the bonded interfaces. The diameter of the Au electrodes was $5\text{ }\mu\text{m}$.

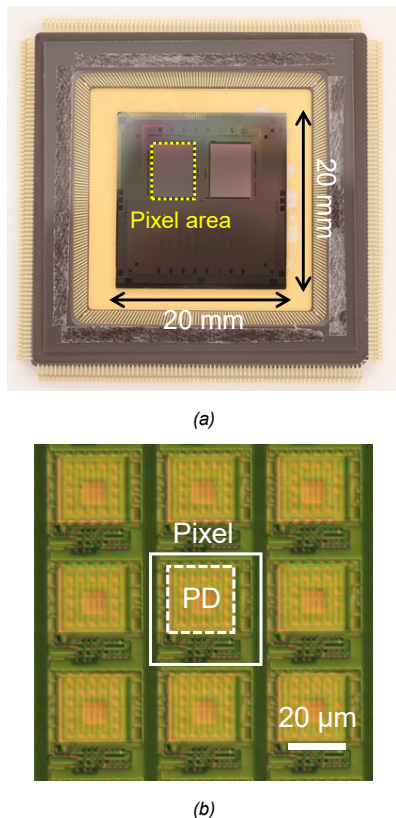


Figure 5. Photographs of the (a) developed sensor chip and (b) pixels.

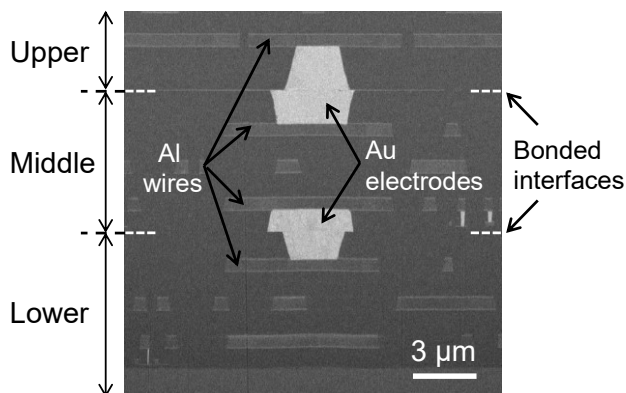


Figure 6. Cross-sectional SEM image of the 3-layer stacked sensor.

Measurement Results

Input-output characteristics of the test pixel circuit were measured (Figure 7). The test pixel was designed without a PD but with an electrical current input instead of photocurrent. We confirmed the linear response of the 16-bit digital signal output generated by the counters in the middle and lower layers, indicating the high bit-depth and wide dynamic range of the ADC with excellent linearity.

Figure 8 shows the input-output characteristics of the 3-layer stacked sensor, where the median value for all pixels was plotted. The output was unchanged in the lower illuminance due to the dark current of the PD in FDSOI, where PD is subject to surface trap. The dark current could be suppressed using the CMOS image sensor process for the PD layer instead of FDSOI, as demonstrated in the previous 2-layered sensor [10]. The output increased corresponding to the input in the higher illuminance. An example of a QQVGA video image captured by the developed sensor is shown in Figure 9, where the lower 8-bit output signal was displayed after a dark signal was subtracted. The frame rate was set to be 30 fps. We successfully confirmed the operation of the 3-layer stacked pixel-parallel CMOS image sensor for the first time.

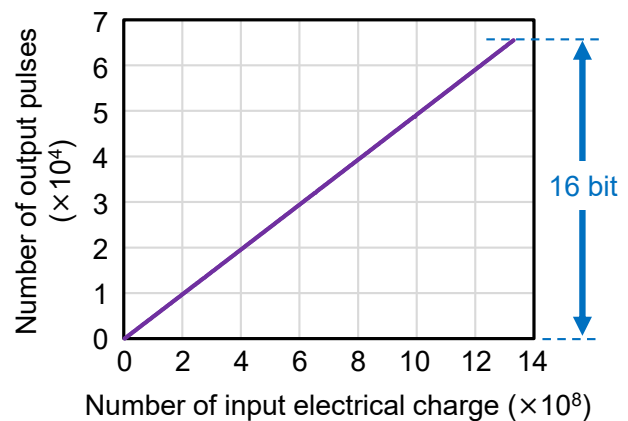


Figure 7. Input-output characteristics measured on the test pixel circuit.

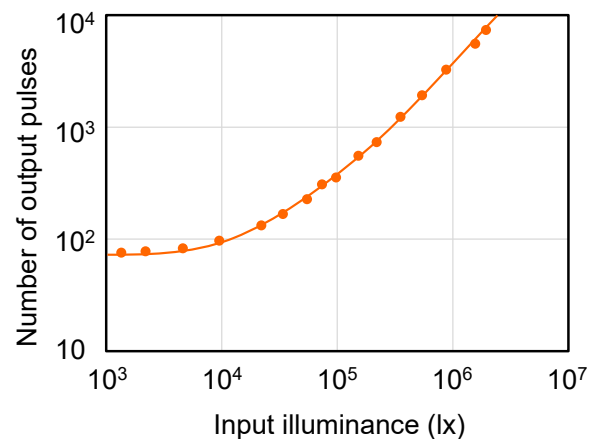


Figure 8. Input-output characteristics of the 3-layer stacked sensor.



Figure 9. Example of QQVGA (160×120 pixels) video image captured by the developed sensor.

Conclusion

A 3-layer stacked pixel-parallel CMOS image sensor was developed using the hybrid bonding of SOI wafers. The SOI process allows face-to-back bonding to accommodate more than three layers of devices. A thin Si layer was introduced as a bonding medium to ensure bonding strength. The developed sensor successfully captured video images, with all pixels operating as pixel-parallel ADCs without pixel defects. The multi-layer stacking process is promising not only for image sensors of ultimate performances but also for various integrated devices such as logic circuits, memories, microelectromechanical systems, and sensors.

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Author Biography

Masahide Goto received the B.S., M.S., and Ph.D. degrees in electrical engineering from the University of Tokyo, Tokyo, Japan, in 1998, 2000, and 2013, respectively. He joined the Japan Broadcasting Corporation (NHK), Tokyo, Japan, in 2000, where he has been with the Science & Technology Research Laboratories. His current research interests include CMOS image sensors, 3-D integration technologies, and digital holography. He is a senior member of the IEEE.