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Design and Analysis on Low-Power and Low-Noise Single Slope ADC for Digital Pixel Sensors

Hyun-Yong Jung, Myonglae Chu, Min-Woong Seo, Suksan Kim, Jiyoun Song, Sang-Gwon Lee, Sung-Jae Byun, Minkyung Kim, Daehee Bae, Junan Lee, Sung-Yong Kim, Jongyeon Lee, Jonghyun Go, Jae-kyu Lee, Chang-Rok Moon, Hyoung-Sub Kim; Samsung Electronics Co., Ltd.; Hwaseong-si, Gyeonggi-do, Republic of Korea

Abstract

A Low-power and low-noise digital pixel sensor (DPS) is presented in this paper. To design and analyze the random noise (RN) of the developed DPS, especially, we utilize a novel simulation method called transient-based AC noise simulation (TBAS) which can effectively help to estimate the noise components of the low-powered single-slope (SS) analog-to-digital converter (ADC). Based on this noise analysis, the high performance DPS has been successfully designed and demonstrated.

Introduction

CMOS image sensor (CIS) are widely used in various applications such as the mobile products, the automotive and the machine vision. In particular, large-pixel or global shutter CIS has been currently regarded as the next generation product, the importance of low-power ADCs is emerging. A single-slope (SS) analog-to-digital converter (ADC) is mainly used for the mature CIS design, and the comparator in the SS ADC is a key building block determining noise characteristic of the CIS [1]. Therefore, an accurate noise estimation of the comparator is essential. For a noise simulation, the frequency noise simulation (FNS) based on system transfer function (TF) and noise power spectral density (PSD) is generally used. Also, in a case of the more precise noise estimation, the transient noise simulation (TNS) can be a great alternative, because it includes all noise factors of simulated circuitry such as the time-varying noises. However, the TNS requires lots of simulation processes and times [2], [3]. In general, the FNS manner is hard to calculate the exact noise level compared with the TNS manner, because of a time-varying nonlinear system (TVNS) resulting in bandwidth (BW) modulation by a ramp signal [3]. Fig.1 shows BWs extracted by the frequency simulation (FS) and the transient simulation (TS) without and with TVNS, respectively. As can be seen from Fig. 1, the extracted BWs by FS and TS are quite different. To improve the noise estimation capability, we need the fast and accurate noise simulation method including TVNS.

In this paper, the transient-based AC simulation (TBAS) based on TVNS analysis with the time-efficient and accurate results is introduced for designing the higher-performance DPS. In addition, the low-power and low-noise DPS with the sub-threshold-operating pixel-level ADC has been successfully developed and demonstrated.

Noise Analysis and Design Method

Noise Analysis

Fig. 2(a) shows a simplified active pixel sensor (APS) schematic including four pixel transistors and single-step SS ADC with its timing diagram. After RG goes to low, $V_{FD\text{-}RST}$ for reset level and $V_{FD\text{-}SIG}$ for signal level are sequentially sampled, and they are converted to D_{RST} and D_{SIG}, respectively. The amplifier's offset, KTC noise, and low-frequency noise such as flicker noise are reduced and cancelled out by a digital correlated double sampling (DCDS) and auto-zeroing implementation. Thanks to these operations, ADC noise itself becomes the dominant factor to determine the sensor noise performance. As mentioned above, therefore, the well-functioned noise simulator is necessary to analyze the ADC noise, and it makes possible to design the low-noise image sensor.

Fig. 2(b) shows a conventional schematic diagram of SS ADC. For the A/D conversion, the SS ADC basically consists of 2-stage operational trans-conductance amplifier (OTA) with the time-varying signal, ramp signal (V_{RAMP}). After the analog pixel data and the ramp signal for reference are inputted to 1st-stage OTA, the output of the 2nd-stage OTA (V_{CMP}) called the comparator including the timing jitter ($\sigma_{ti,\,rms}$), which reflects the actual noise BW, is latched when the dc level of pixel data and ramp slope are crossed at the same potential. The digital count value written to the memories is determined by V_{CMP}.

For the proper noise calculation, the TF must be considered with TVNS affected by ramp slope (dV_{IN}/dt) [5]. To explain the noise analyzing method, the equivalent circuit of the amplifier and the step-ramp input are shown in Fig. 3(a). During the ramping phase, the capacitor voltage (V_{OUT}) which is charged by a noisy current source and ramp operation is presented as Fig. 3(b). The waveform can be separated into the average ramp of the dc current source (G_mV_{IN}) and a noise current (I_n) integrating on C_O. As V_{OUT} crosses its common mode ($V_{OUT,CM}$), then V_{OUT} is toggled and decision delay (t_i) decides the width of the time window(W(t)) in time-varying system as shown in Fig. 3(c). At the end of time window, a statistical distribution can describe the noise waveform. The voltage noise variance, σ_{On}^2, is converted to the time-noise variance, $\sigma_{ti,rms}^2$. The noise function of the comparator including a ramp slope such as a SS ADC can be given as [3]

$$V_n(f)^2 = I_n \times H_{OTA}(f)^2 \times H_W(f)^2 \tag{1}$$

$$H_{OTA}(f)^2 = \frac{1}{1+(2\pi f\tau_O)^2} \tag{2}$$

$$H_W(f)^2 = \frac{1-2e^{-\frac{t_i}{\tau_O}}\cos(2\pi f t_i)+e^{-\frac{2t_i}{\tau_O}}}{1-2e^{-\frac{t_i}{\tau_O}}+e^{-\frac{2t_i}{\tau_O}}} \tag{3}$$

in frequency domain, where $V_n(f)$ is output-referred noise PSD, I_n is input-referred noise PSD, τ_O is a steady-state time constant of the comparator, $H_{OTA}(f)$ is a TF of OTA and $H_W(f)$ is a BW modulation TF of the TVNS amplifier. As shown in Eq. (1), total noise is determined by a product with $H_{OTA}(f)$ and $H_W(f)$. Thus, the total integrated noise of the image sensor with SS ADC can define as shown in Fig. 4. $I_{n,OTA}$ and $O_{n,SF}$ is input-referred noise PSD of

OTA and output-referred noise PSD of the source follower, respectively. Finally, total noise is expressed as

$$\sigma_{ti}^2 = \int_0^{\infty} (I_{n,OTA} + O_{n,SF}) \times V_n(f)^2 \times H_{CDS}(f)^2 df \quad (4)$$

$$H_{CDS}(f)^2 = 4\sin(\pi f T_{CDS})^2 \quad (5)$$

Where T_{CDS} is time distance between D_{RST} and D_{SIG}.

Transient-Based AC simulation

The TBAS is the novel noise estimation method combining results of both TS and FS. To complete the TFs of Eq. (2), (3), and (5), the parameters of $I_{n,OTA}$ and τ_O are extracted from the FS, and the parameters of T_{CDS} and τ_i are extracted from the TS. Fig. 5 shows the actual comparator waveforms of the SS-ADC implementation for defining the used constants. t_i is defined as the time interval from the cross point of the V_{RAMP} and V_{PIX} to the time where 1st-stage OTA output (V_{O1}) crosses its common mode voltage (V_{CM1}). T_{CDS} is defined as the time interval of V_{CMP}'s both falling edges for the reset and the signal A/D conversion periods.

Table 1 shows the noise comparison results with FNS, TNS, and TBAS for SS ADC using high- and low-power comparators. The FNS is implemented by the conventional steady-state AC simulation and the TNS is performed by Monte Carlo simulation with 500 different noise seeds. As shown in table 1, noise estimations with TBAS are closer to the TNS values than FNS's results, because the FNS includes no windowed BW component, $H_W(f)$, modulated by the step-ramp input. In addition, the TBAS has much shorter simulation running time than that of the TNS, because the TNS typically needs lots of simulation numbers and should include wide band, especially, higher frequency. The both noise simulation results of TNS and FNS at consuming the high and low powers are quite different. According to the Eq. (1), when the high-powered comparator is used, the time ratio, t_i/τ_O, is normally larger than the factor of 2. In this case, noise BW calculated by the FNS is comparable with that in the TNS. On the other hand, the time ratio is getting smaller with consuming the less power, the BW modulation effect is greatly increased compared with the high-power consuming case.

Measurement Results

Fig. 6 shows the block diagram of the developed 2-stack DPS. The prototype chip is composed of a pixel substrate and a logic substrate. The top chip on the pixel-substrate side, which is fabricated in 65 nm CIS process, includes an APS array. The bottom chip on the logic-substrate side, which is integrated in 28 nm logic process, has the pixel-level ADC with a small bias current, analog peripheral circuits, and logic blocks for the image signal process (ISP).

Fig. 7 shows the noise analysis results implemented by the TBAS. The TFs of SS ADC are shown in Fig. 7(a). The finalized TF (blue solid line) is achieved by combining the H_{OTA}, H_W, and H_{CDS}. Using this TF, we can easily analyze each noise component of SS ADC including the thermal and flicker noises as shown in Fig. 7(b). In addition, TBAS makes it possible to confirm each transistor's noise contribution in the circuitry as can be seen from Fig. 7(c) and Fig. 7(d).

The input-referred temporal random noise results of the developed DPS as a function of analog gain are shown in Fig. 8. We can confirm that the simulation results with TBAS are sufficiently good matched with the actual measurement data in comparison with the conventional AC noise simulation.

Lastly, the die micrographs of the top and bottom chips are shown in Fig. 9(a). The fabricated top and bottom chips have been bonded and then it is packaged for the evaluation. All functions and sensor performances have been successfully evaluated and demonstrated [6]. Fig. 9(b) shows the sample image s with fast-moving object (a fan with approx. 5000 rpm) which is captured by the developed low-powered DPS.

Conclusion

The novel noise estimation method, which includes the modified BW modulated by time-varying step-ramp input, has been suggested and utilized to design the low-power and low-noise SS ADC for the DPS. The effectiveness of TBAS has been fully demonstrated in this paper, and we believe this method can be very helpful to develop the advanced CMOS image sensors.

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Author Biography

Hyun-Yong Jung received the B.S. degree in electrical and electronic Engineering from the Korea Advanced Institute of Science and Technology, Korea, in 2010 and the M.S. and Ph.D. degree in electrical and electronic Engineering from the Yonsei University, Seoul, Korea, in 2017. From 2017, he is working for Samsung Electronics as a CIS engineer. His research interests include silicon photonics, optoelectronic integrated circuits, global shutter, digital pixel, low noise and low power image sensor.

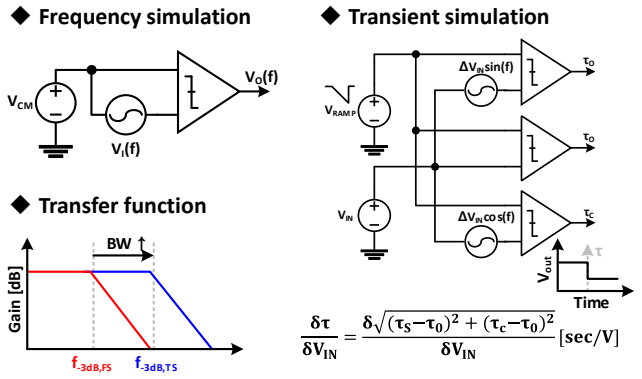


Figure 1. Transfer function extracted by the frequency and transient simulation.

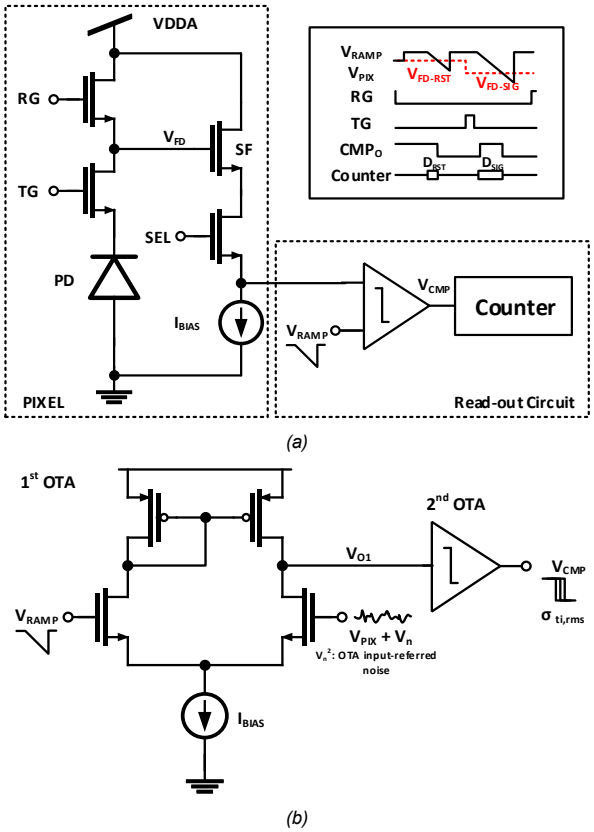


Figure 2. (a) Simplified pixel read-out circuit, timing diagram and (b) Comparator schematic.

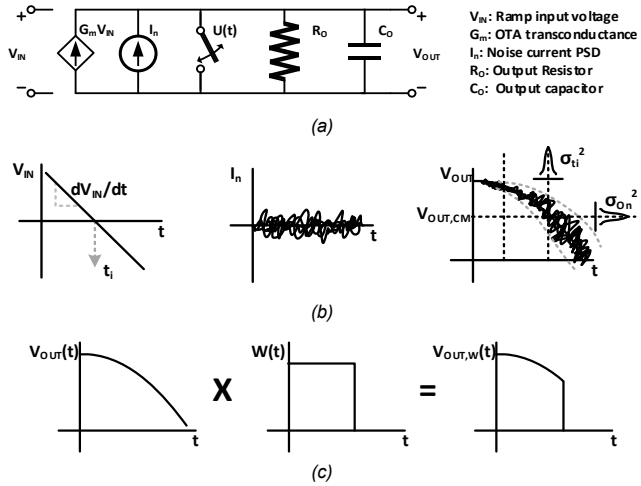


Figure 3. (a) Equivalent circuit of amplifier, (b) corresponding noisy output with ramp input, and (c) system impulse response with time window.

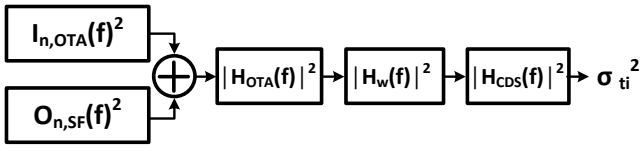


Figure 4. Image sensor noise with various transfer functions.

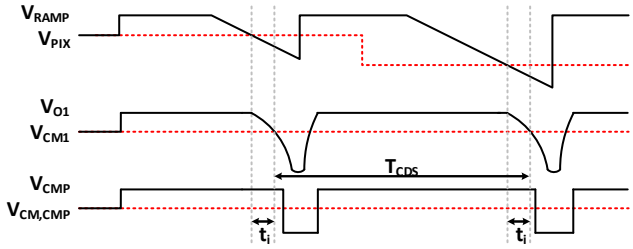
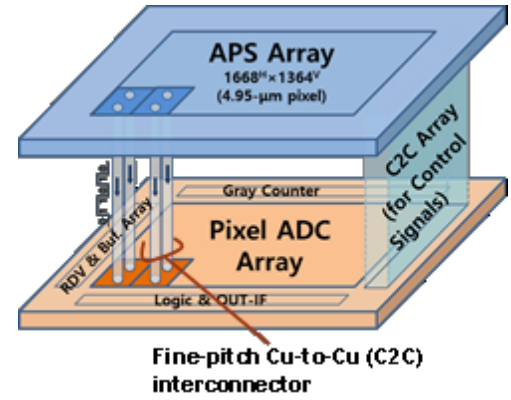


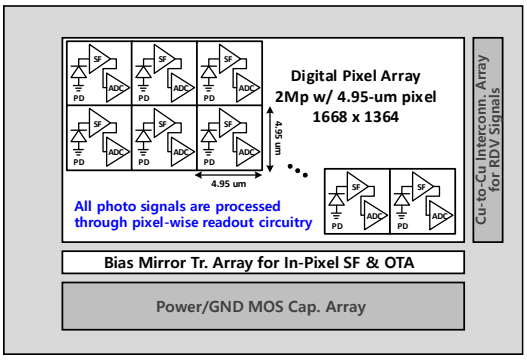
Figure 5. Comparator waveforms for the constants definition.

Table 1. Noise comparison with various simulation methods for high- and low-power comparator.

		FNS	TNS	TBAS
Hi-Power (Strong inversion)	f-3dB	0.79 MHz	N/A	1.28 MHz
	Noise	102 µVrms	109 µVrms	112 µVrms
Lo-Power (Sub threshold)	f-3dB	42.9 kHz	N/A	150.4 kHz
	Noise	248 µVrms	344 µVrms	356 µVrms

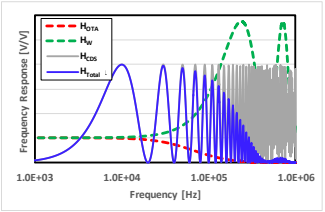


(a)

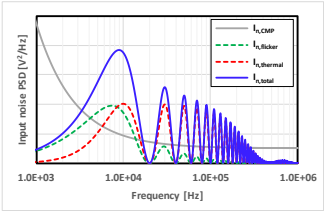


(b)

Figure 6. (a) A 2-stacked DPS block diagram and (b) sensor architecture.



(a)



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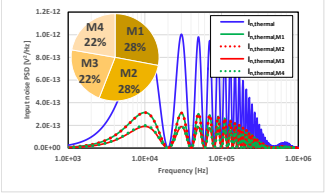
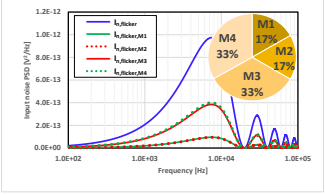


(c)



(d)

Figure 7. (a) SS ADC transfer functions and (b) input-referred noise PSD and total noise for each noise components. (c) Thermal and (d) flicker noise PSD from each MOSFET in ADC. Insets are noise contribution.

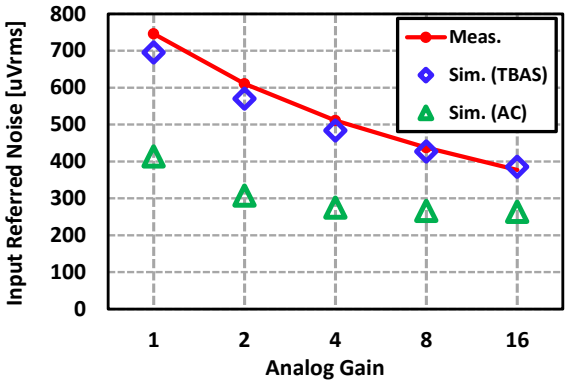
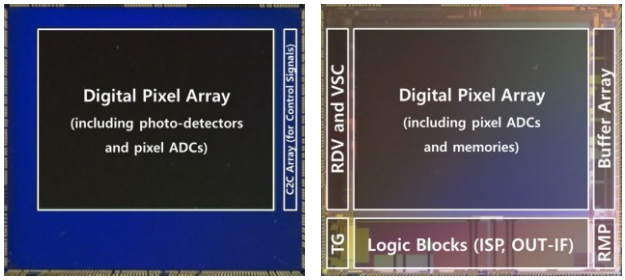
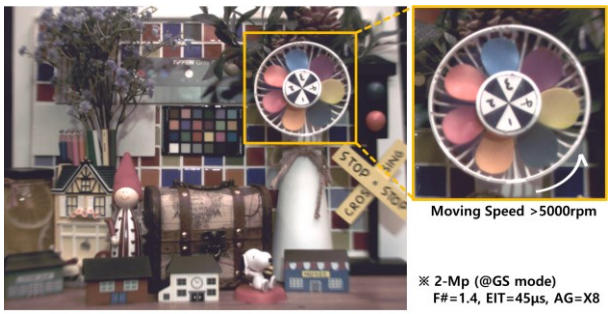


Figure 8. Simulated and measured random noise with the various analog gain.



(a)



(b)

Figure 9. (a) Implemented DPS microphotograph and (b) 2Mp global-shutter sample image with fast-moving fan.