https://doi.org/10.2352/EI.2022.34.7.ISS-155

An Offset Calibration Technique for CIS Column-Parallel SAR ADCs Using Memory

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Abstract

A column-parallel 10-bit SAR ADC for high-speed image sensors has been implemented. A fast offset calibration technique using memory is proposed to compensate for the offset mismatch, accompanied by an ADC designed for a narrow space the size of a single column pitch. The memory accumulates the variation of the offset to track the offset within two cycles. After applying the offset calibration technique, the offset variation of the ADC measured in each column is improved from 4.27LSB to 0.39LSB. The fixed-pattern noise (FPN) is also improved from 4.14LSB to 0.34LSB. This calibration method covers an offset range of ±32LSB. The implemented ADC achieves a maximum speed of 500kS/s. The maximum frame rate of the sensor is 3000fps. The power consumption of the sensor, excluding the LVDS interface, is 71mW. This sensor is designed in a TowerJazz CIS 180nm process with one poly four metal. The supply voltage of the analog and digital domains is 3.3V and 1.8V, respectively.

Introduction

Recently, many researchers have performed R&D on high frame rate image sensors. The advent of a wide variety of applications such as machine vision, and the demand for high quality video images strongly justify the research for high frame rate sensors [1-3]. These R&Ds have mainly improved the frame rate of the sensor by increasing the number of ADCs [4-5] or designing a different type of ADC [2-3]. In particular, due to the limitations of the single-slope ADC, such as inefficient data conversion and speed limitation of the counter, SAR ADCs or cyclic ADCs have been designed to overcome these limitations. As a result, research on high frame rate image sensors has achieved a horizontal line time of less than 2μs [2-4]. In most cases, designing a SAR ADC is more beneficial for achieving high-speed data conversion than a cyclic ADC due to its efficient data conversion using a binary search algorithm. However, though the SAR ADC has an efficient algorithm for high-speed data conversion, its designed silicon area and noise performance introduce limitations. In particular, the SAR ADC has many unit capacitors that occupy a relatively large silicon area. As a result, very often, pixels in multiple (neighboring) columns share the same ADC due to lack of space [2], [6-7]. This structural problem leads to channel mismatch, such as offset, so a large bandwidth is required for fast data conversion of the SAR ADC. Furthermore, the offset mismatch impacts the fixed-pattern noise (FPN), and the large bandwidth compromise temporal noise performance.

In this paper, we propose a fast offset calibration technique for the SAR ADC. This offset calibration technique is expected to suppress the offset mismatch which occurs in a SAR ADC designed for a narrow space of a one-pixel pitch. To implement this fast offset calibration, memory designed for each column accumulates the offset variation. This accumulated offset information in turn compensates for the offset during the offset calibration period by controlling the potential level of the capacitor DAC's output. As a result, the image sensor can use the SAR ADC in a column-parallel structure to enhance the frame rate while relaxing the specification of the SAR ADC at each column. Therefore, this paper will review the image sensor's readout circuit chain and its operation timing in Section 2. Section 3 will discuss the offset calibration method using memory. Finally, this paper will show the measurement results in Section 4.

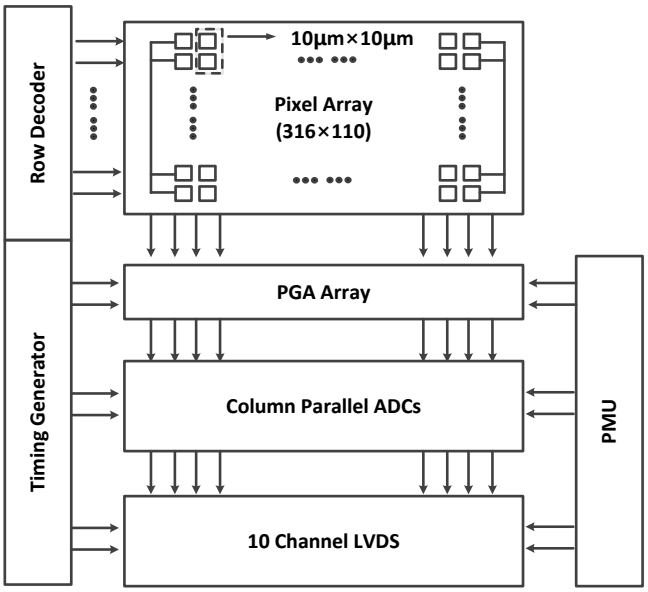

Figure 1. Block diagram of the sensor

Readout Architecture with SAR ADC

Sensor architecture overview

Figure 1 shows a block diagram of the sensor, which has a 316 × 110 pixel array. Since this sensor employs a column-parallel structure, the analog front end consists of 316 ADCs and 316 Programmable Gain Amplifiers (PGAs). Moreover 10 LVDSs are used as an interface to the outside world. An I^2C interface defines the register setup for each circuit block. The power management unit (PMU) contains reference generators and a bandgap reference (BGR). The row decoder creates the pixel control signals. Figure 2 depicts the readout circuit chain of this sensor including the SAR ADC and the PGA. The maximum analog gain supported by the PGA is 8x. The SAR ADC has 1026 unit capacitors in the positive and negative parts of the capacitor DAC; the unit capacitor size is 0.56fF. The control logic controls the negative part of the DAC for data conversion while the positive part of the DAC controls the offset calibration. The sensor accepts an external clock, CLK_{EXT}, to control the sensor; this external clock is divided into an internal clock by the clock divider, as shown in Figure 2. In addition, the internal clock is reshaped into a signal CLK_{COMP} to control the comparator, as shown in Figure 3.

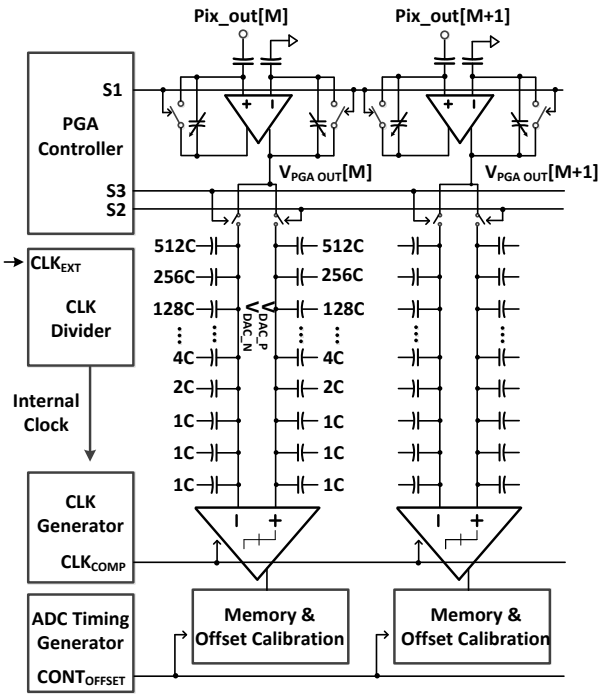

Figure 2. Block diagram of readout chain

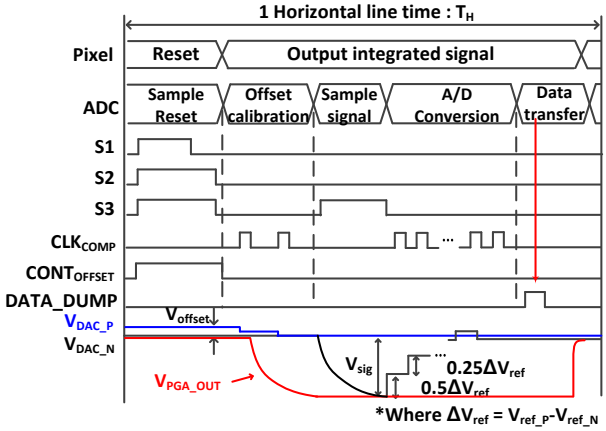

Figure 3. Timing diagram for PGA and ADC in one horizontal line time

Figure 3 shows a timing diagram for controlling the ADCs and the pixels within one horizontal line time. At the beginning of one horizontal line time, the PGA resets itself by turning on S1. At the same time, the ADC samples the reset level of the pixel, VCM, on the capacitor DAC by turning on S2 and S3. The PGA completes the reset operation after turning off S1, while the ADC also finish its sampling by turning off S2 and S3. After sampling, the ADC performs the offset calibration for two cycles, and the pixel starts transmitting the integrated signal to the PGA. In the next phase, the ADC samples the integrated signal from the PGA with S3 turned on. After the sampling is completed by turning off S3, the potential at V_{DAC_N} is $V_{CM} - V_{sig}$. The V_{sig} is the signal resulting from charge integration at the pixel. The ADC converts the signal using a binary search method during the subsequent ten cycles starting from the MSB part. After ten cycles, the digital

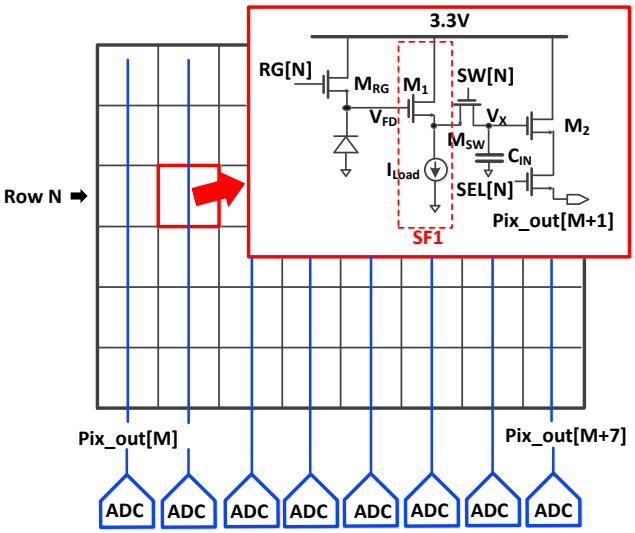

Figure 4. Pixel array and circuit diagram with 3T pixel and sampling net work

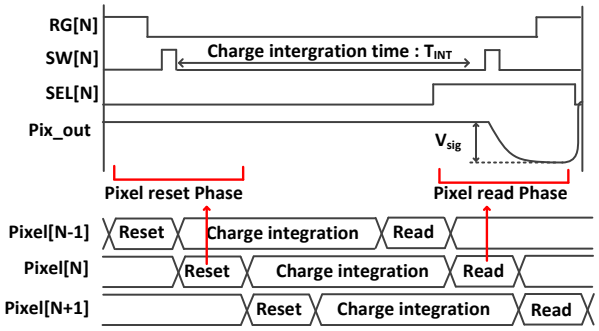

Figure 5. Timing diagram example for controlling single pixel

codes are stored in the register array and transmitted to the interface at the rising edge of DUMP_DATA shown in Figure 2.

3T pixel structure with sampling network

Figure 4 shows a circuit diagram of a single-pixel included in a pixel array. As shown in Figure 4, the sensor generates signals by means of a 3T pixel. The 3T pixel has the advantage in speed compared to a 4T pixel. Specifically, the 3T pixel can output the signal immediately, and the only factor controlling the speed is the current applied in the source follower. All outputs of the pixels located in the single column are connected to a single output line, which enables the sensor to read the pixel sequentially by using the ADC located at each column. Figure 5 illustrates the timing diagram for controlling the pixel array containing this 3T pixel structure. Since the sensor employs a rolling shutter method, the sensor reads out the lines sequentially. In addition, the sensor resets each line sequentially to maintain the same charge integration time. In this work, the ADC calibrates the comparator before the analog-to-digital conversion, the pixel must output reset level first. The sampling network is designed with the 3T pixel to enable this readout sequence.

The pixel control procedure consists of three phases: reset, charge integration, and reading. First, in the reset phase, the row decoder turns on the reset gate, M_{RG}, to reset the pixel before the

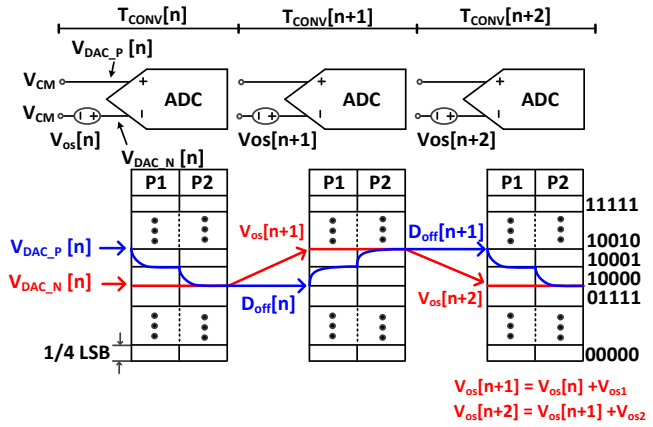

Figure 6. Simplified principle of offset calibration

photodiode starts integrating the charge. After the pixel reset, the row decoder turns off the reset gate, M_{RG}, by controlling the signal RG, and then samples the reset level of the pixel on the sampling capacitor C_{IN} by turning on the switch M_{SW}. The capacitor C_{IN} preserves the sampled reset level until the pixel reading phase. In the meantime, the photodiode starts integrating charge generated by incoming light. The holding time of the sampled reset level is equal to the integration time, T_{INT}. In the pixel reading phase, the reset level preserved on C_{IN} is output to the PGA first through the output of the source follower, V_{PIX_OUT}. Next, the signal level is sampled on the C_{IN} after the sampling of the reset level of the ADC is completed. This sampled signal level is also output to the PGA during the offset calibration period. The ADC samples this signal level from the PGA after completing the offset calibration. In the pixel reset and reading phase, since the signals from the photodiodes are output through an internal source follower (SF1), as shown in Figure 4, the current sources must be activated. However, enormous power consumption is inevitable when all internal current sources are operating simultaneously. Therefore, only the current sources of the two rows in the pixel reset and the pixel reading phase are working at every horizontal line time to reduce power consumption.

Offset Calibration Technique and Advantages

The offset calibration algorithm

In this readout architecture, two factors can introduce FPN. The first factor is the variation of the pixel reset level, and the second factor is the offset inside the ADC. The PGA regulates the pixel reset level difference with the auto-zeroing technique in this work. Previous research has shown that this auto-zeroing technique has already demonstrated the effect on FPN performance [11]. However, this technique cannot compensate for the offset inside an ADC because the ADC samples the signal that the PGA regulates. Therefore, the offset inside the ADC will directly appear in the image as FPN. Figure 6 shows the simplified principle of the offset calibration technique used in this work. Theoretically, the offset is fixed noise. However, any variation occurs in the environment of the ADC could change this offset slightly. The proposed offset calibration algorithm compensates for this offset variation at each horizontal line time by performing background operations.

In Figure 6, we assume that the offset, V_{off}, is positioned at the top plate of the negative capacitor DAC, V_{DAC_N}, and that this offset varies slightly in each conversion phase. Once the offset calibration starts, the ADC samples the reset level, V_{CM}, at its positive and negative inputs. At n-th horizontal line time, $T_{CONV}[n]$, the potential level $V_{DAC\_N}[n]$ including offset variation is $V_{CM} + V_{off}[n]$. As shown in Figure 6, when the offset calibration algorithm calibrates the offset at $T_{CONV}[n]$, the memory stores this offset information as a digital output, $D_{off}[n]$. At the next horizontal line time, $T_{CONV}[n+1]$, the offset level changes again, and the offset increment $V_{off}[n+1] - V_{off}[n]$ is V_{os1}, as shown in Figure 6. When the ADC starts the offset calibration at $T_{CONV}[n+1]$, the ADC loads the previous offset information, $D_{off}[n]$. Therefore, the ADC only has the newly added offset V_{os1}, which the ADC calibrates within two cycles. Therefore, the offset calibration logic easily estimates the offset increment corresponding to V_{os1}, and the memory accumulates this offset information to generate new offset information as a digital output, $D_{off}[n+1]$. At the next horizontal line time, $T_{CONV}[n+2]$, if the offset is changed by V_{os2} again, the offset calibration starts estimating using the information $D_{off}[n+1]$. In the same way, the offset calibration algorithm continuously compensates for the offset, so the offset information is updated.

This offset calibration algorithm has two critical advantages. The first advantage is that the algorithm calibrates the offset within two cycles. Since this algorithm continuously retrieves the previous offset information from the memory, the offset that is newly added in each conversion phase is relatively small. Therefore, it is possible to compensate the offset within a short amount of time. The second advantage is that this ADC does not need an adder or subtractor. This offset calibration controls the positive part of the capacitor DAC. After two cycles of the offset calibration period, the SAR ADC sets the potential V_{DAC_P} as a 0 code level. As a result, the DAC control automatically subtracts the offset level from the signal level.

The capacitor DAC control for calibration

Figure 7 shows an example of the capacitor DAC control accompanied by a 5b up-down counter for the offset calibration at one horizontal line time. Since two digits in the LSB part of the counter refer to 0.5LSB and 0.25LSB, respectively, the unit capacitors controlled by these LSB parts use the reference voltage V_{refP2}, V_{refN2} and V_{refC}, as shown in Figure 7(a). This offset calibration logic controls the positive part of the capacitor DAC. The signal $CONT_{OFFSET}$ illustrated in Figure 3 controls the switch network of the positive part of capacitor DAC to transfer the offset information from the previous offset calibration period. At the beginning of the horizontal line time, the ADC samples the reset level, while the signal $CONT_{OFFSET}$ is in a high state. The switch control logic connects the bottom plate of all capacitors except the 4C to the negative reference, as shown in Figure 7(a). If we assume that the offset exists in the negative part of the DAC, the signals sampled on each DAC are $V_{CM} + V_{off}$ and V_{CM}, respectively. The controller turns off switches S2 and S3 when the ADC completes the sampling of the reset level. After completing the reset sampling, control signal $CONT_{OFFSET}$ becomes low-state. At the falling edge of signal $CONT_{OFFSET}$, the bottom plate of the DAC is connected to the output of the up-down counter, as shown in Figure 7(b). As a result, the mathematical representation of the signal in the positive part of the capacitor DAC is:

$$V_{DAC\_P} = V_{CM} - (D_{INIT} - D_{MEM}) \times V_{1/4LSB}$$

where $V_{1/4LSB}$ is the analog signal corresponding to 0.25LSB, and D_{INIT} and D_{MEM} are the initial values of the counter output and the digital code memorized at the counter, respectively. Therefore,

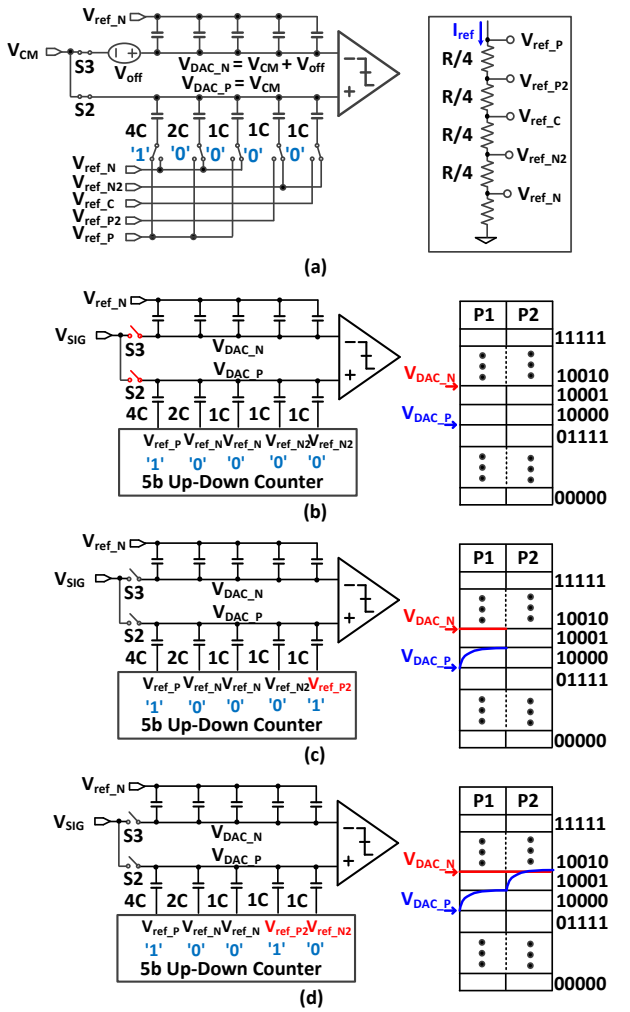

Figure 7. Switch control method for offset calibration

if the value registered is '10000', the potential at the positive part of the DAC is maintained in the same state as V_{CM}, as shown in Figure 7(b). In the first comparison phase, in Figure 7(b), the potential at the negative part is higher than that at the positive part. After the comparison, the comparator output becomes low-state, and the counter adds a 1LSB code. As a result, the potential at the output of the positive part of the capacitor DAC adds $V_{1/4\ LSB}$, as shown in Figure 7(c). In the second comparison phase, the potential at the negative part is still higher than that in the positive part. When the comparator completes the second comparison, the comparator output becomes low-state again, and the counter adds a 1LSB code again. Consequently, the offset is compensated, as shown in Figure 7(d), and the counter saves the digital outputs generated from the offset calibration until the next offset calibration. Since the counter retains the output until the next offset calibration, the offset can be re-estimated in the next calibration period. We use an 8b up-down counter in this work, with and offset cover range of ±32LSB.

Measurement result and discussion

The measurement environment

The proposed CMOS image sensor has been fabricated in a TowerJazz 0.18μm CIS process technology. The chip size is

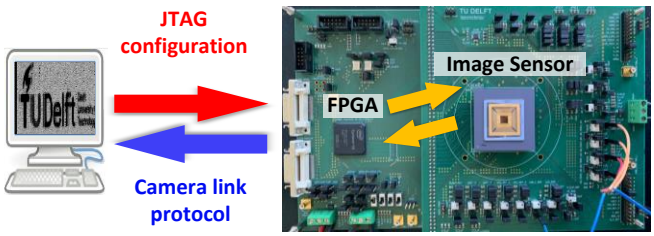

Figure 8. Test environment setup with a PCB and FPGA

5.0mm × 5.0mm, while the core area of the pixel array is 110 × 316. Within this pixel array, the sensor effectively uses a 300 × 90 pixel array. An Altera Cyclone10 FPGA provides the digital control signals and captures the image sensor's output data. LabVIEW receives the data transmitted through the camera-link interface from the FPGA, and the post-processing is done in MATLAB. Since this system does not output any code below 0, post-processing is performed during the measurement in dark conditions. Figure 8 shows the combination of the test setup with the FPGA.

In this work, the sensor receives a maximum clock of 50MHz from the FPGA. The speed of the clock distributed inside cannot support exceed 50MHz due to a process limitation. Therefore, the maximum speed measured of the ADC is 500kS/s. Since the maximum speed of the LVDS interface is 1Gb/s, the shortest horizontal line time the sensor can support is 4μs, while the maximum frame measured rate is 3000fps. Finally, Table 1 shows a summary of the performance, and Figure 10 shows a microphotograph of the test chip.

Table 1. Performance summary

Process		TowerJazz 0.18μm CIS process(1P4M)
Pixel array		316(H) × 110(V) Effective pixel array : 300(H) × 90(V)
Pixel size		10μm × 10μm
Conversion gain		58.24μV/e-
Full well capacity (FWC)		8042e-
Noise performance	Read noise	712.8μV(=12.2e-)
	VFPN	0.34LSB(with offset calibration)
	HFPN	0.07LSB
DR		56.3dB
Frame rate		maximum : 3000fps
ADC resolution		10
ADC saturation level		500mV
ADC sampling rate		maximum : 500kS/s
LVDS speed		1Gb/s (10 Channels)
Power consumption	Analog + Digital + PIxel	78.5mW @ 3000fps 71mW @ 730fps
	LVDS interface	59.4mW(10 Channels)

The measurement result and analysis

To verify the effect of this offset calibration technique, 100 images are captured in a dark environment. The ADC offset and the vertical fixed pattern noise (VFPN) are characterized after averaging these images. Specifically, the offset calibration logic requires time to set the register value at an appropriate point. Therefore, this algorithm needs a maximum of 128 horizontal line times because cover range of ±32LSB. For this reason, the first frame is excluded from the analysis. Figure 9 shows the impact of this technique on image quality. In this figure, the averaged images

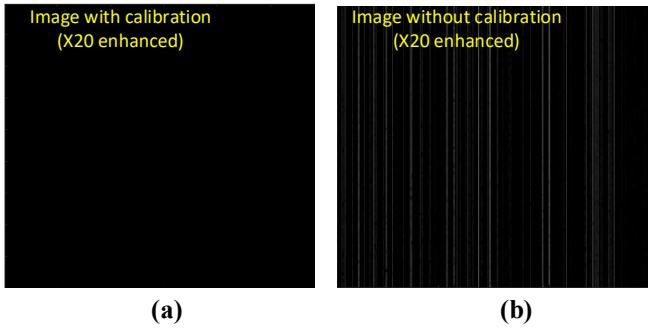

Figure 9. Image taken in a dark environment (a) with offset calibration and (b) without offset calibration

have been enhanced by 20 times. Figure 9(b) shows that the VFPN is observed when the offset calibration is not applied. On the other hand, the offset calibration technique does improve the image quality, as depicted in Figure 9(a).

After post-processing, the data show that the offset calibration improves the ADC offset variation from 4.27LSB to 0.39LSB. In addition, the averaged offset measured of the ADC is -0.6LSB after post-processing. The main reason for the offset is that switch S3 introduces offset due to the coupling effect of the junction capacitor. In the same way, the VFPN is improved from 4.14LSB to 0.34LSB after the offset calibration is applied.

Table 2 shows the impact of this offset calibration on the VFPN performance of this image sensor. As described in the table, the sensor has better VFPN performance when the sensor uses digital CDS because the digital CDS eliminates the error induced by the circuit [9]. However, this CDS inevitably has a long horizontal line time because, in this case, the ADC must convert the data two times. On the other hand, the analog CDS cannot compensate for the offset originating from the readout circuit. Therefore, if the comparator is not calibrated accurately, the sensor's VFPN performance is impacted [6], [8]. If a sufficient comparator offset calibration technique is applied to the sensor, which uses analog CDS, the VFPN performance is substantially improved [10]. In addition, this design requires a smaller area for the offset calibration technique than [10], which is designed with an offset sampling technique, because this calibration circuit consists of a digital circuit, as described in the previous section. Finally, this technique has a robust effect on the offset calibration compared to the offset sampling method [10].

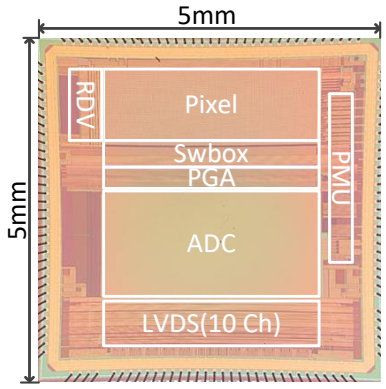

Figure 10. Test micrograph of the fabricated chip

Table 2. Performance comparison

Year	2022	2014	2018	2015	2018
Ref	This work	[8]	[6]	[9]	[10]
Technology	180nm	180nm	90nm	180nm	180nm
Pixel array	300×90	920×256	1920×1440	256×128	190×160
Pixel pitch	10$_\mu$m	1.85$_\mu$m	1.4$_\mu$m	4.4$_\mu$m	25$_\mu$m
Frame rate	3000 fps	9 fps	50 fps	90 fps	3000 fps
Power consumption	78.5 mW	21.2 mW	64 mW	4.4 mW	623 mW
Conversion gain	58.24$_\mu$V	70$_\mu$V	N/A	60$_\mu$V	202.85$_\mu$V
Analog gain	×1 – ×8	-	-	×1 – ×4	×1 – ×8
ADC type	SAR	SAR	SAR	SAR	SAR
ADC resolution	10	9	10	12	14
Temporal noise	710.52$_\mu$V (12.2e-)	5.3mV (75.7e-)	273.6$_\mu$V	268.8$_\mu$V (4.48e-)	2.3mV (11.5e-)
Dynamic range	56.3 dB	50.6 dB	66.5 dB	68.1 dB	68.7 dB
VFPN	0.34 LSB (0.03%)	0.5%	0.23%	0.17 LSB	0.12%
CDS type	Analog	Mixed	Analog	Digital	Analog
Comparator offset	Calibrated	Calibrated	-	-	Calibrated

Conclusion

A CMOS image sensor with a column-parallel SAR ADC has been realized. We suggest the application of a fast offset calibration technique to compensate for the offset induced by the ADC, which is designed for a narrow space. Memory enables the implementation of this offset calibration. The memory accumulates the offset variation and compensates the offset within two cycles. As a result, the offset calibration technique improves the VFPN performance of the sensor from 4.14LSB to 0.39LSB. This technique also enables the sensor to be designed with a column-parallel structure that can enhance the frame rate of the sensor. In conclusion, this work suggests that the SAR ADC design in a column-parallel structure can improve an image sensor's frame rate.

Acknowledgement

This work was supported by the SENSATION project, sponsored by the Dutch government and the EC. The authors would like to thank TowerJazz for their support in fabricating the silicon dies.

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