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Efficient In-Cabin Monitoring Solution Using TI TDA2P× SOCs

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Abstract

In-Cabin Monitoring Systems (ICMS) are functional safety systems designed to monitor driver and/or passengers inside an automobile. Driver Monitoring System (DMS) and Occupant Monitoring System (OMS) are two variants of ICMS. Camera based ICMS present a unique set of imaging challenges to system designers in terms of new 4×4 *RGB-IR color filter array (CFA) sensor format, smaller form factor, target applications in human and machine vision, low light image quality, thermal noise, image resolution and color accuracy. This paper presents an efficient camera ICMS implementation on Texas Instrument's TDA2P× automotive system-on-chip solution with focus on a new software-hardware (SW-HW) pipeline for image signal processing(ISP) of the* 4×4 *RGB-IR CFA. The proposed SW-HW solution achieves real-time 2MP-60fps processing simultaneously producing full resolution color and Ir images. The software portion of the pipeline can be run on vector processing engine EVE using only 12% of the available resource and 45% of the ISP hardware resource. This allows implementation of high-end ICMS systems using other available compute resources.*

Introduction

More than 90% of road accidents are attributed to driver errors, of which 41% due to driver's inattention, internal and external distractions, and inadequate surveillance[1, 2]. Leaving a child unattended in a parked car especially the one exposed to the sun, even for a few minutes, can lead to heat-stroke and death[3]. In-Cabin Monitoring Systems (ICMS) designed to monitor vehicle occupants using one or more cameras commonly along with other sensing modalities can help prevent such accidents and fatalities[4]. As an example ICMS provides a significant level of feedback to advanced driver assistance systems (ADAS), electronic control units (ECUs), and autonomous driving systems to compensate for and help correct common errors introduced by drivers. An example would be a scenario where the driver is distracted and the vehicle alerts the driver or maneuvers to avoid a collision[5].

ICMS can be divided in two broad classes- 1) Driver Monitoring Systems (DMS) and 2) Occupant Monitoring Systems (OMS). DMS monitor driver state and OMS monitor all occupants of a vehicle including passengers and children. The constituent tasks of DMS like- driver's head pose, body pose and gaze monitoring can be efficiently implemented using camera based ICMS. Whereas tasks like vital signs monitoring can be implemented using Radar sensing. Time-of-Flight sensor can also be used in the systems. Additionally, ICMS may also support non safety applications such as video-conferencing, personalized configuration and gesture based control.

Camera based ICMS commonly use Ir imaging with active illumination for safety applications and many non-safety applications require color imaging. These requirements are driving adoption of sensors that capture perfectly-aligned RGB and infrared (IR) images simultaneously, especially the ones with 4×4 color filter array (CFA) patterns. The 4×4 RGB-IR CFA pattern most commonly used has 50% green pixels, 25% infra-red pixels, and 12.5% each of the red and blue pixels[6]. In addition to the imaging requirement for higher resolution, wide angle lenses and dual-band filter (DBF), new CFA require that the image signal processing (ISP) pipeline addresses requirements of both machine and human vision applications. New CFA pattern and changed optical system present a new set of challenges- raw domain processing for lens shading correction (LSC) and defective pixel correction (DPC), up-sampling of the Ir channel to full resolution to compensate sub-sampled signal as compared to Ir only camera sensors, demosaicing of the RGB color channels to obtain full resolution color image, and Ir de-pollution of the color images[7, 8, 9, 10].

This paper presents an efficient camera ICMS implementation on Texas Instrument's TDA2P× automotive system-on-chip (SoC) solution including a novel 4×4 RGB-IR CFA processing scheme. The remainder of paper is organized as follows- Section 2 presents the proposed approach to implement camera based ICMS on embedded application processor TDA2P×. Setion 3 presents the resource utilization estimates for various processors, application specific hardware accelerators and sample ISP outputs for the proposed SW-HW solution pipeline. Final section presents the concluding remarks.

Proposed System Architecture

While implementing DMS on any SoC, the first task is to partition the functions into groups. Figure 1 shows a functional block diagram of a camera based ICMS. The ISP stage is positioned at beginning of the functional ICMS pipeline and plays an important role in overall system. In view of the requirements discussed earlier, system designers need to overcome the challenges in an efficient manner[11]. The obstacles designers face are- most existing ISPs are designed to process only 2×2 CFA patterns, and the compute requirement of various functional blocks is diverse. This section presents the proposed approach to the design camera ICMS based on Texas Instrument's system-on-chip(SoC) solutions, particularly TDA2P× platform SoCs.

Implementation of a typical camera based ICMS on TDA2Px

TDA2P× platform is a SoC solution that integrates multiple compute cores, co-processors and peripherals to address requirements of multiple ADAS applications as heterogeneous compute architectures are more suitable for these the applications. Applications such as front camera, surround view, auto-valet parking, high-way driving and in-cabin monitoring[12]. TDA2P× con-

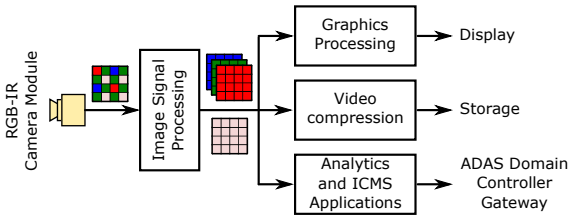

Figure 1. *Typical functional blocks of a camera based ICMS*

tains dual cores of ARM Cortex A15 as host or application CPU, POWERVRTM SGX544 GPU, two cores of c66x DSP, two cores of a vector processor Embedded Vision Engine (EVE), integrated ISP, high definition image and video accelerator (IVA-HD) and Display Sub-system (DSS). A block diagram of the SoC is presented in the Figure 2.

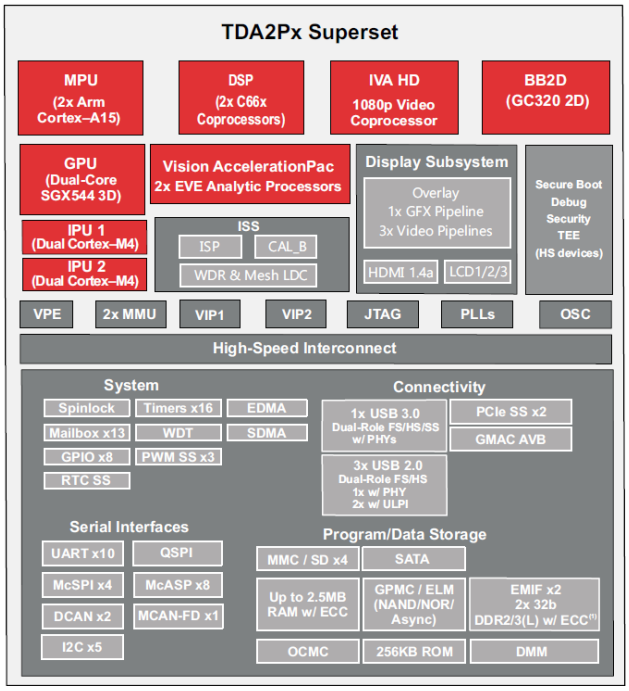

Figure 2. *TDA2X block diagram*

Considering the requirements of typical ICMS TDA2P× can be used to develop an efficient system. However, like many existing ISPs the ISP integrated on TDA2P× is also designed to handle only 2×2 CFA patterns[13]. To address this limitation and enable ISP of the 4×4 RGB-IR processing a software-hardware (SW-HW) ISP pipeline is presented here. The SW-HW pipeline converts the problem of demosaicing of the RGB color channels to full resolution into two parts where an intermediate 2×2 Bayer CFA pattern is generated from the input raw image using SW running on programmable cores and this Bayer CFA image is demosaiced by the HW ISP block. The intermediate 2×2 Bayer CFA pattern is generated by increasing density of red and blue pixels to 25%. As an example this can be achieved by interpolating the blue pixel values at originally Ir locations and red pixel values at the originally blue locations. The SW block can further implement the extraction and up-sampling of the Ir image along with

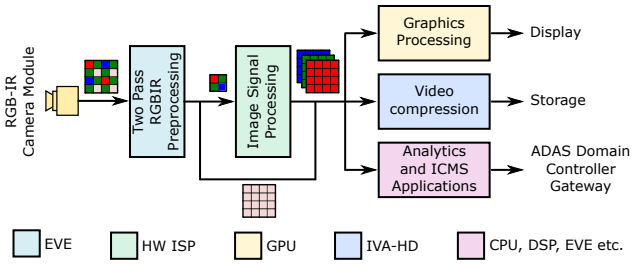

Figure 3. *ICMS functionality mapping on various compute blocks on TDA2P× SoC*

suppression of Ir cross-talk in color pixels. The effective ICMS system implementation with functionalities mapped on different compute cores is shown in Figure 3. In an alternate implementation of the system, extraction and up-sampling of the Ir image can also be performed by the HW ISP.

RGB-IR Pre-processing Scheme

Here we present the detailed SW-HW approach of ISP. The multi-pass approach to ISP processing uses EVE for SW preprocessing of the sensor raw data and ISP HW to convert the predicted Bayer pattern to full resolution color images. The overall functional flow can be summarized as

1. Application processor stores the raw sensor data received over camera interface into the system memory
2. First pass processing:
   (a) EVE reads the raw CFA data to extract $1/4$ resolution Ir channel and write back into DDR
   (b) The HW ISP resizes the extracted Ir plane along with optional DPC, noise filtering(NF), black level compensation(BLC), LSC, gamma correction and edge enhancement(EE) operations. The up-sampled Ir output is written out to DDR for consumption by machine vision applications.
3. Second pass processing:
   (a) EVE re-reads the raw CFA data to increase blue/red pixel density to 25% and create a Bayer CFA pattern that is written out to DDR. This step can also optionally read the previously up-sampled Ir to perform Ir subtraction for cross-talk suppression.
   (b) The HW ISP processes newly created Bayer CFA to generate color output with optional DPC, NF, BLC, LSC, EE, color correction and tone-mapping operations. The color output is written to DDR for consumption by machine/human vision applications.

Method for creation of Bayer pattern

As described earlier in this section a Bayer pattern can be created from RGB-IR CFA pattern by interpolating the red pixel values at original Ir locations and blue pixel values at the original red locations. The green pixels which already constitute 50% of the raw pixels do not need any processing. To interpolate the red pixel values at the originally blue locations one can use nearby *four* red pixels located vertically and horizontally at distance of 2 pixels. For efficient implementation and to reduce aliasing, for

calculating red pixel value at blue location gradient directed linear interpolation scheme is used. Here, the gradient information from green channel is used determine the interpolation direction. If the horizontal gradient exceeds its vertical gradient by an amount at least equal to a threshold (T) then the interpolation is performed using vertical neighbors. Similarly when the vertical gradient exceeds the horizontal gradient by an amount at least equal to the threshold, then the interpolation is performed using vertical neighbors. If the difference between the horizontal and vertical gradient is below the threshold, simple averaging is performed. Thus the output red pixel value R_{out} at a blue location (i, j) is defined in Eq. 1.

$$R_{out}(i,j) = \alpha * (raw(i,j-2) + raw(i,j+2)/2) + (1-\alpha) * (raw(i-2,j) + raw(i+2,j)/2)) \quad (1)$$

Where the weighting factor α is defined in Eq. 2.

$$\alpha = \begin{cases} 1 & \text{if } |raw(i,j-1) - raw(i,j+1)| + T < |raw(i-1,j) - raw(i+1,j)| \\ 0 & \text{if } |raw(i-1,j) - raw(i+1,j)| + T < |raw(i,j-1) - raw(i,j+1)| \\ 0.5 & \text{otherwise} \end{cases} \quad (2)$$

To interpolate the blue pixel values at the original Ir locations one can use *two* diagonally adjacent blue pixels. In the 4×4 RGB-IR CFA pattern blue pixels neighboring an Ir pixel can be in one of the two orthogonal directions. Thus, interpolation needs to handle both the scenarios appropriately. In the proposed approach we use simple linear interpolation for blue pixels.

Ir subtraction method

The light sensitive element in each pixel of a CMOS image sensor array is a silicon photo-diode. These photo-diodes are sensitive to photons in visible and in NIR bands. CFA modulates the sensitivity of each pixel to make them sensitive to specific wavelengths. The RGB-IR cameras use DBF filter to simultaneously capture the visible and Ir wavelength light. This results in red, green and blue pixels remaining sensitive to Ir wavelengths. This warrants subtraction of Ir signal from these pixels to remove contamination. In the proposed SW-HW pipeline during second pass a fraction of up-sampled Ir signal is subtracted from the newly created Bayer image cross-talk suppression. Where the fraction of Ir to be subtracted is a programmable parameter. The Ir subtracted Bayer value ($Bayer'$)at location (i, j) thus is calculated as

$$Bayer'(i,j) = Bayer(i,j) - \beta * Ir(i,j) \quad (3)$$

where $Bayer$ is the newly created Bayer pattern image and Ir is the up-sampled Ir channel image.

In addition to the ISP of RGB-IR processing presented here the TDA2P× SoC can support features like-

- HDR imaging– with hardware capable of multi-exposure merge and locally adaptive tone mapping,
- Image distortion correction- needed for wide angle lenses-with LDC hardware block which uses Mesh LUT and bi-cubic interpolation , running machine vision and Human Vision. TDA2P ISP has a hardware block
- Running machine vision algorithms- such as face detection, eye gaze and body pose monitoring, facial recognition, emotion detection, generic object detection etc., using C66x DSPs and *two* EVEs and dual core A15 CPU. THese resources can be used to run both traditional computer vision and modern algorithms like CNNs.
- Video/image compression for storage and streaming- using IVA-HD video accelerator engine.

System Resources Utilization and ISP Results

Implantation of the SW-HW ISP pipeline even in the *two*-pass mode has been found out to be very efficient on TDA2P×. The approach is estimated to use nearly 12% of the EVE and 45% of the ISP HW for the RGB-IR camera producing both color and Ir outputs for 2MP input raw images at 60 frames per second, see Table 1. The additional compute requirement on EVE is nearly 1 Cycle/pixel and a very small overhead.

Resource utilization on TDA2P× for the SW-HW pipeline

Compute resource	Utilization
EVE	120MHz (12%)
ISP HW	240MHz (45%)
DDR Bandwidth	1800 MBPS

Figure 4 presents a sample input and simultaneous Ir and color outputs that can be obtained using the SW-HW pipelined ISP presented in this paper. The output color image shows excellent reconstruction with mean chroma error of 13.8 with the X-Rite color checker chart and white balance error of 1.1(Figure 5).

Conclusion

This paper presented implementation of a camera based ICMS system on TI's TDA2P× SoC while addressing imaging challenges presented by the new sensor CFA pattern and optical system. The challenges addressed include efficient and high quality Ir up-sampling, color demosaicing and cross-talk suppression. The presented SW-HW ISP pipeline can efficiently utilize the available compute resources (EVE + ISP HW) for multi-pass implementation leaving large percentage of compute resources available for running other functional components of the ICMS system especially the machine vision algorithms and analytics applications.

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Figure 4. *(a)Input raw 4×4 RGB-IR image (b)Extracted Ir image (c) Reconstructed color image outout of the SW-HW pipeline*

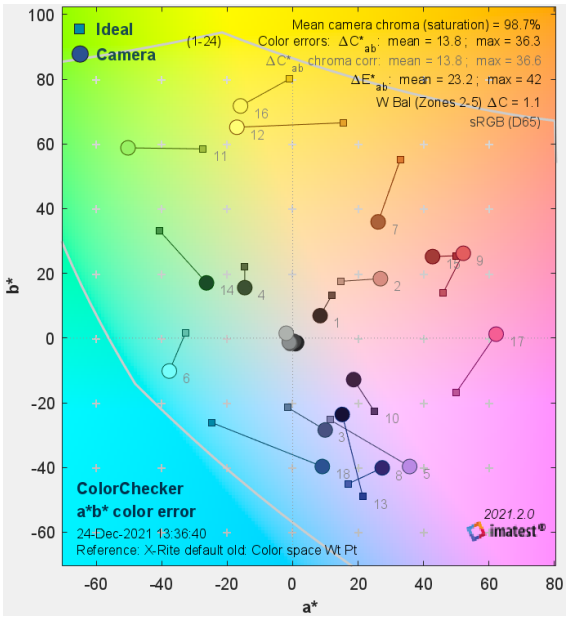

Figure 5. *Color checker a*b* color error plot*

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Author Biography

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