https://doi.org/10.2352/ISSN.2470-1173.2021.7.ISS-092

A Proposal of Analog Correlated Multiple Sampling with High Density Capacitors for Low Noise CMOS Image Sensors

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Abstract

In this paper we propose a low power consumption high speed analog correlated multiple sampling (CMS) technique with high density switched capacitors for low noise CMOS image sensors. A CIS with 256 analog memories per pixel using high density trench capacitors was employed in order to verify the noise reduction effect dependent on operation timings. The noise characteristics were measured at sampling numbers of M=1~64 with various CMS sampling period of 10ns to 1μs and time interval between reset and signal samplings, thanks to the high flexibility owing to the proposed analog CMS technique. The measurement results agree well with the theoretical calculation results, showing that conducting CMS with highly correlated signals is effective in noise reduction.

Introduction

Recently, low noise performance of CMOS image sensors (CIS) is required in order to obtain high SNR clear image in both consumer and scientific usage. As noise reduction techniques, reduction of source follower (SF) low frequency noise [1-2], reduction of floating diffusion (FD) capacitance to increase conversion gain (CG) [2-4], the optimization of pixel source follower and column readout circuit have been extensively studied [4-7].

Correlated multiple sampling (CMS) technique has been reported to be effective in reduction of low frequency noise of in-pixel source follower, which is one of the main noise sources in CIS [8]. As for the types of CMS, digital CMS using column parallel ADC and analog CMS using switched capacitor integrators have been proposed [9]. Using single slope ADC [10], sampling period of CMS is limited by the conversion time of ADC, thus a higher clock rate is necessary in order to shorten the CMS sampling period. To improve the effective speed of ADC operation, differential slope ADC that can operate twice faster than conventional single slope ADC was reported to be useful [11]. Conditional CMS scheme has also been proposed to effectively achieve high speed operation [12]. In addition, parallel CMS using multiple number of ADCs per column enabled by 3D stacking technology has been proposed to optimize CMS sampling period [13]. For analog CMS using switched capacitor integrators, signal range has a tradeoff between the number of sampling. Folding integration/cyclic cascade ADC has been reported to be useful to solve this issue and to achieve both high speed and low noise performances [14]. In these methods generally, in order to shorten CMS period for a larger number of multiple sampling, higher circuit speed is required for ADC and/or amplifiers, which tends to results in a larger power consumption. For parallel CMS scheme, circuit operation speed per ADC can be suppressed compared to the serial CMS counterpart, however it requires multiple ADC circuits per column, leading to a restriction of number of multiple sampling.

Another way to achieve analog CMS operation is to introduce multiple number of sample/hold switches and capacitors as analog memories in parallel and operate signal sampling in each analog memory. Here placing multiple number of analog memories per column has been proposed for signal processing function such as binning with neighbor pixels or a high framerate imaging with on-chip signal storage [15-16]. Here the multiple sampling can be controlled by simple sample/hold switches as to be explained later and this operation does not require high speed circuits or multiple number of ADCs. However, the capacitor area increases as number of sampling raises. A method of reducing the number of switched capacitors to n for 2^n sampling has been reported to be useful for suppressing the total number of capacitors for CMS [17]. Yet, suppressing the capacitor area has been a challenge for this scheme. Recently high-density capacitors such as high-k MIM capacitor and deep Si trench capacitor have been developed and utilized for in-pixel or on-chip passive circuit elements for CIS [18]-[25]. By these capacitors, the area of switched capacitors can be reduced, so that the number of CMS can be increased. This makes the analog CMS with multiple switched capacitors an attractive method for low power consumption and low noise signal readout for CIS.

This work proposes an analog CMS with charge sharing function using multiple switched capacitors formed by high density capacitors. As a feasibility study, the effect of analog CMS is to be verified using a global shutter CIS with 256 high density trench capacitor analog memories placed adjacent to each pixel, and the optimization of operation timing is conducted through both theoretical calculation and experimental results.

Summary of CMS theory and proposed analog CMS circuit

CMS is a technique that can reduce low frequency noise including 1/f noise of in-pixel source follower and column amplifier noise at the previous stage of CMS circuit, by taking a difference between the average of reset level voltage and the average of signal level voltage, both sampled multiple times.
The output voltage of CMS circuit V_o is expressed as

$$V_O = \frac{1}{M}\sum_{i=1}^{M}\{V_R(i) - V_S(i)\} \quad (1)$$

where $V_R(i)$ and $V_S(i)$ are the reset and signal level voltage of pixel output which are sampled M times [8]. Figure 1 shows the timing diagram of CMS; where M, T_0 and N are the number of sampling, sampling period and the multiples of T_0 for time interval between reset level and signal level samplings.

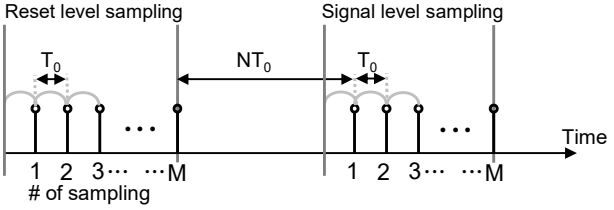

Figure 1. Timing diagram of the correlated multiple sampling.

The transfer function of CMS obtained by z-transformation which represents the time delay of sampling is given by

$$H(z) = \frac{1}{M}\sum_{i=0}^{M-1} Z^{-i}\left\{1 - Z^{-(M+N-1)}\right\} \quad (2)$$

when $Z=e^{j\omega T_0}$, $|H(\omega)|^2$ can be written as

$$|H(\omega)|^2 = \frac{4}{M^2}\cdot\frac{\sin^2\frac{\omega M T_0}{2}}{\sin^2\frac{\omega T_0}{2}}\cdot\sin^2\frac{\omega(M+N-1)T_0}{2} \quad (3)$$

Using equation (3), the noise power generated by the readout circuit P_{noise} is calculated as

$$P_{noise} = \int_0^{\infty} S_{np}(f)\frac{1}{1+\left(\frac{f}{f_c}\right)^2}|H(f)|^2 df \quad (4)$$

where $S_{np}(f)$ is the noise power spectrum in the previous stage of CMS circuit and f_c is the cut-off frequency of the readout circuit. These equations show readout noise can be reduced by increasing sampling number M and shortening sampling interval between reset level to signal level sampling NT_0.

The proposed analog CMS circuit structure is presented in Figure 2. By shifting the sampling timing of each switched capacitors, multiple sampling is conducted and different voltages are held in switched capacitors. Using high density capacitors can suppress the area penalty in spite of increasing the number of multiple sampling. For example, by using Si trench capacitors, more than 5 times as much capacitance density as that of MOS capacitors can be achieved [23]. Although the efficiency of area usage by Si trench capacitors is remarkable, there is a few things to consider. Si trench capacitors require additional manufacturing processes. The threshold voltage of the Si trench capacitors needs to be sufficiently low in order to achieve constant capacitance across a signal range. In addition, the leakage current must be low in order to hold analog voltage signal. In order to achieve above mentioned requirements, the impurity profile around Si trench was optimized, and high integrity SiO_2 with controlled thickness was utilized [23]. In this circuit, analog CMS is conducted by subtracting the charge-shared signal level voltage from that of reset level voltage. The increase in capacitance value of switched capacitor can reduce thermal noise and the gain loss from parasitic capacitance. In addition, the signal voltage range does not increase as the number of sampling increases so that the number of multiple sampling is scalable in the proposed method as long as the capacitor's area is allowed.

Furthermore, this analog CMS circuit can operate at high speed without increasing power consumption because each sampling is conducted only by shifting the turning off timings of the analog switches.

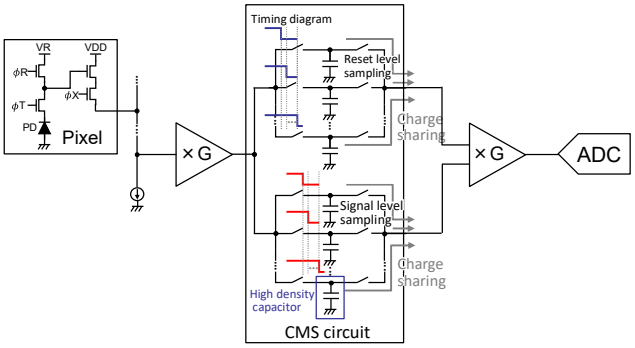

Figure 2. Column parallel analog CMS circuit with high density capacitors.

Experimental results and discussion

Figure 3 shows the micrograph of the fabricated chip with $80^H \times 81^V$ effective pixels employed for measurement in this work. This sensor has been originally designed for global shutter ultra-high speed imaging application [26]. The chip was fabricated by using a 0.18 µm 1-Poly-Si 5-Metal layer CMOS sensor technology. The size of square pixel is 48 µm by 48 µm each, and in-pixel 256 analog memories with a capacitance of 50 fF were used. The analog memories are composed of Si trench capacitors with the capacitance density of 30fF/µm^2 [23]. The design specification is summarized in Table1. Consequently, an analog memory array is prepared for each pixel with a limited capacitance value. Thus, to reduce the thermal noise generated in the CMS circuit, the capacitance of each switched capacitor is preferred to be 1pF or more, which is to be placed as column parallel manner. Figure 4 shows pixel circuit diagram of the chip used for measurement in this work; figure 5 shows its CMS operation timing. The in-pixel CDS circuit was not used in the CMS operation for the measurement so that the individual reset and signal level voltages were sampled and held in in-pixel 256 analog memories at each sampling period. Here, the sampling period used for the measurements was 50 ns, unless otherwise specified. Each signal was output from the MEM_OUT node and the output buffer to outside of the chip, and averaged to prove the CMS effect. Here, signal readout from the CMS circuit to the chip output was carried out much slower than the CMS period, the noise arising latter stage of the CMS circuit will be suppressed by the square root of the sampling number M. In order to analyze the CMS effect toward the noise arising at the previous stage of the CMS circuit, total noise and noise after CMS circuit were measured, and the noise characteristics before the CMS circuit were extracted. Note that the measured noise values hereafter are in the form of input referred noise voltage at the floating diffusion.

The measured noise characteristics before and after memory array are shown in figure 6. The total input referred noise at the sampling number M = 1 was 1.61 mV_{rms} and it was suppressed to 262 μV_{rms} at M = 64, in addition, the CDS noise was 1.60 mV_{rms}; this measurement result confirmed the noise reduction effect of CMS. Figure 7 shows the noise source estimation of measured input referred noise before memory array. The estimation is based on fitting calculated noise from equation (4) to measured noise by separating $S_{np}(f)$ into 1/f noise and random noise which includes thermal noise. The results indicates that the main noise source changed from random noise to 1/f noise as the number of sampling increases and the noise reduction effect was different from the frequency response of each noise.

Figure 8 shows the influence of multiples of sampling period between reset level to signal level sampling N to the noise reduction effect of CMS operation. In this measurement, the CMS operation from N = 7 to N = 100 was effectively available by selecting data from 256 memories. The calculated noise was estimated from equation (4) and the average of measured noise at M = 1 from N = 7 to N = 100. This figure shows that the effect of reducing sampling period between reset level to signal level sampling NT_0 became more prominent as the number of sampling increases. This indicates, considering also from figure 7, shortening sampling period between reset level to signal level sampling NT_0 is efficient to 1/f noise reduction.

Although there is some remained noise before and after the memory array, the latter can be reduced by optimizing the signal readout circuit. About the former, thermal noise at analog memories is one of the main noise component so that to increase capacitance of each analog memory is to be effective for further noise reduction.

Figure 9 represents the total input referred noise from T_0 = 10ns to T_0 = 1us. 100MHz sampling was conducted at T_0 = 10ns which confirmed CMS was also effective for the very short sampling period. At T_0 = 1μs and M =56, 64, the characteristic of CMS noise reduction was slightly offset which might be caused by the increase in sampling time and relatively uncorrelated signals were sampled.

The sensor used in this work is originally designed for global shutter high-speed imaging, not aiming to achieve photon counting. Thus, signal readout noise needs to be suppressed for photon counting usage. To achieve photon counting, a CIS dedicated to the proposed analog CMS with multiple switched capacitors in column is to be evaluated as a future work. The sensor is expected to achieve photon counting level sensitivity by reducing the FD capacitance to achieve high CG, and by using high-gain column amplifier to reduce the noise in the subsequent circuit, in addition to the CMS noise reduction technique proposed here.

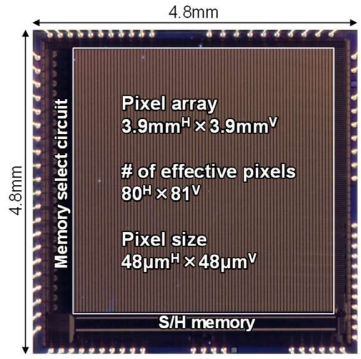

Figure 3. Micrograph of the fabricated chip

Table 1. Design specifications of the developed CIS.

Technology	0.18μm 1P5M CMOS with pinned PD
Voltage supply	3.3 V
Chip size	4.8mm^{H} × 4.8mm^{V}
Pixel pitch	48μm^{H} × 48μm^{V}
# of pixels	80^{H} × 81^{V}
# of analog memories	256

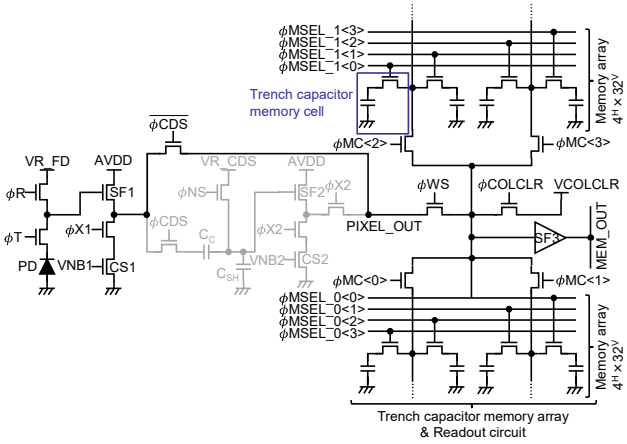

Figure 4. Pixel circuit diagram of the CMOS image sensor used for measurement in this work.

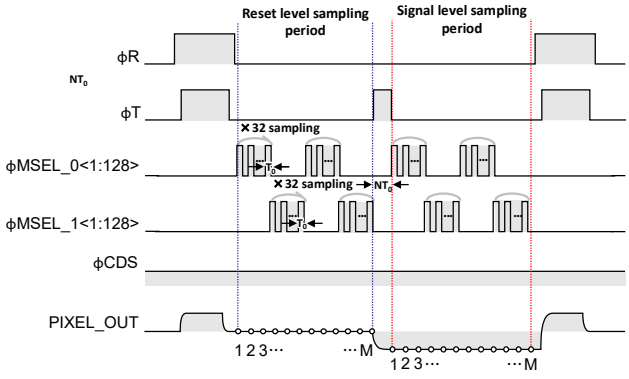

Figure 5. Timing diagram of CMS operation.

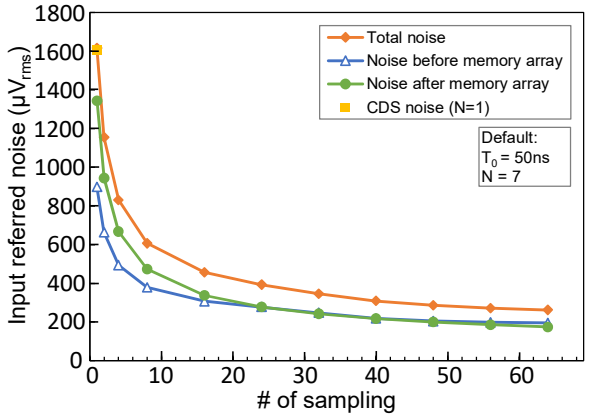

Figure 6. Measured input referred noise as a function of the number of sampling M.

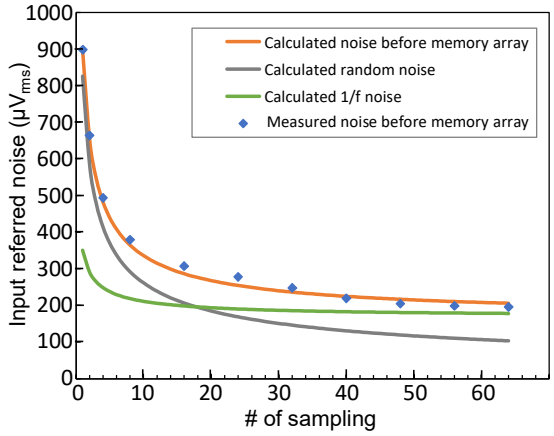

Figure 7. Noise source estimation of Measured input referred noise before memory array

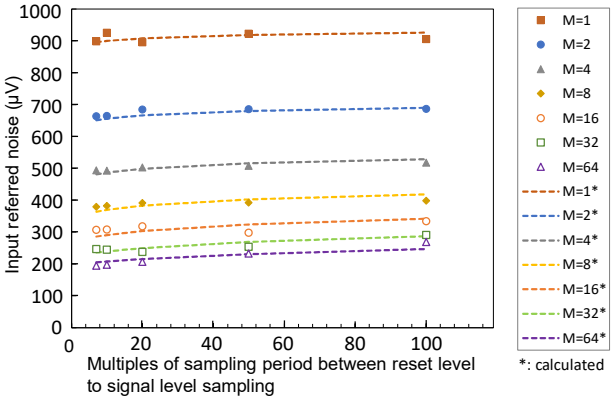

Figure 8. Measured input referred noise before memory array as a function of the multiple of sampling period between reset and signal level sampling.

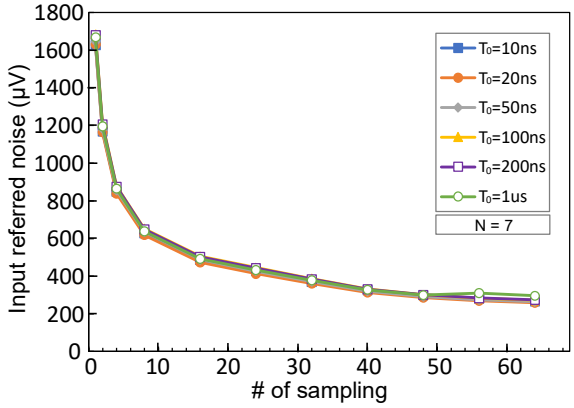

Figure 9. Measured input referred total noise as a function of the number of sampling M and sampling period T_0

Conclusion

In this work, a fast and low power consumption analog CMS circuit with high-density capacitors was proposed. The theoretical and experimental results confirmed that the noise could be effectively reduced by shortening sampling period and acquiring the highly correlated signals. In addition to the conventional noise reduction techniques, by using the proposed analog CMS circuit and optimizing the operation timing, a low noise image sensor with photon counting level sensitivity would be achieved.

References

[1] Xinyang Wang et al., "A CMOS Image sensor with a buried-channel Source Follower," ISSCC Dig. Tech. Papers, pp. 62-595, 2008.

[2] S. Wakashima et al., "A linear response single exposure CMOS image sensor with 0.5e- readout noise and 76ke- full well capacity," 2015 Symposium on VLSI Circuits Digest of Technical Papers, pp. C88-C89, Kyoto, June 2015.

[3] J. Ma et al., "A pump-gate jot device with high conversion gain for a quanta image sensor," IEEE J. Electron Devices Soc. 2015, vol. 3, no. 2, pp. 73-77, 2015.

[4] M.-W. Seo et al., "A 0.27e⁻rms read noise 220- μV/e⁻ conversion gain reset-gate-less CMOS image sensor with 0.11-μm CIS process," IEEE Electron Device Lett., Vol.36, No.2, pp.1344-1377, 2015.

[5] Y. Chen et al., "Column-parallel digital correlated multiple sampling for low-noise CMOS image sensors," IEEE Sensors Journal, 12, 4, pp. 793-799, 2012.

[6] A. Boukhayma et al, "A sub-0.5 electron read noise VGA image sensor in a standard CMOS process," IEEE Journal of Solid-State Circuits, vol.51(9), 2016.

[7] P. Vu et al., "Low noise high dynamic range 2.3Mpixel CMOS image sensor capable of 100Hz frame rate at full HD resolution," Proc. Intl. Image Sensor Workshop, pp. 161-164, 2011.

[8] N. Kawai et al., "Effectiveness of a correlated multiple sampling differential average for reducing 1/f noise," IEICE Electron. Exp., vol. 2, no. 13, pp. 379-383, 2005.

[9] S. Kawahito et al., "Noise reduction effects of column-parallel correlated multiple sampling and source-follower driving current

switching for CMOS image sensors," International Image Sensor Workshop, June 2009.

[10] Y. Chen et al., "Column-parallel digital correlated multiple sampling for low-noise CMOS image sensors," IEEE Sensors Journal, 12, 4, pp. 793-799, 2012.

[11] K. Kitamura et al., "A two conversions/sample, differential slope multiple sampling ADC with accelerated counter architecture," in Proc. Int. Image Sensor Workshop, 2015.

[12] S.-F. Yeh, et al., "A 0.66e-rms temporal-readout-noise 3DStacked CMOS image sensor with conditional correlated multiple sampling (CCMS) technique," Symposium on VLSI Circuits Dig.Tec. Papers, pp. C84-C95, 2015.

[13] H. Wakabayashi et al, "A 1/1.7-inch 20Mpixel back-illuminated stacked CMOS image sensor with multi-functional modes," ITE Transactions on Media Technology and Applications, 4, 2, pp. 136-141, 2016

[14] T. Wang, "A 19-bit column-parallel folding-integration/cyclic cascaded ADC with a pre-charging technique for CMOS image sensors," IEICE Electronics Express, 14, 2, pp. 1-12, 2017.

[15] Z. Zhou et al., "Frame-transfer CMOS active pixel sensor with pixel binning", IEEE Trans. Electron Devices, vol. 44, no. 10, pp. 1764-1768, 1997.

[16] Y. Tochigi et al., "A global-shutter CMOS image sensor with readout speed of 1 Tpixel/s burst and 780 Mpixel/s continuous," IEEE ISSCC Dig. Tech. Papers, pp. 382-383, 2012.

[17] A. Boukhayma et al., "A correlated multiple sampling passive switched capacitor circuit for low light CMOS image sensors," ICNF, 2015.

[18] G. D. Wilk, "High-k gate dielectrics: Current status and materials properties considerations," Journal of Applied Physics, vol.89 (10), 2001.

[19] Y.L. Tu et al., "Characterization and comparison of high-k metal-insulator-metal (MiM) capacitors in 0.13 /spl mu/m Cu BEOL for mixed-mode and RF applications," Symposium on VLSI Technology, pp. 79-80, 2003.

[20] K. Nishimura et al., "An 8K4K-resolution 60fps 450ke—saturation signal organic-photoconductive-film global-shutter CMOS image sensor with in-pixel noise canceller," in IEEE ISSCC Dig. Tech. Papers, pp. 82–83, 2018.

[21] M. Takase et al., "An over 120 dB wide-dynamic-range 3.0 um pixel image sensor with in-pixel capacitor of 41.7 fF/um2 and high reliability enabled by BEOL 3D capacitor process," in Proc. IEEE Symp. VLSI Technol., pp. 71–72, 2018.

[22] J.-K. Lee et al., "A 2.1e^- Temporal noise and -105dB parasitic light sensitivity backside illuminated 2.3μm-pixel voltage-domain global shutter CMOS image Sensor Using High-Capacity DRAM Capacitor Technology," ISSCC Imagers and ToF Sensors, pp.102-104, 2020.

[23] M. Suzuki et al., "An over 1 Mfps global shutter CMOS image sensor with 480 frame storage using vertical analog memory integration", IEDM Tech. Dig., pp. 8.5.1-8.5.4, 2016.

[24] M. Murata et al., "A high near-infrared sensitivity over 70-dB SNR CMOS image sensor with lateral overflow integration trench capacitor," IEEE Transactions on Electron Devices, vol. 67, no.4, pp. 1653-1659, 2020.

[25] A. Tournier et al., "A HDR 98dB 3.2um charge domain global shutter CMOS image sensor," in IEDM Tech. Dig., pp. 229–232, 2018.

[26] M. Suzuki et al., "Over 100 Million Frames per Second 368 Frames Global Shutter Burst CMOS Image Sensor with Pixel-wise Trench Capacitor Memory Array," Sensors, vol. 20, no. 4, 2020.

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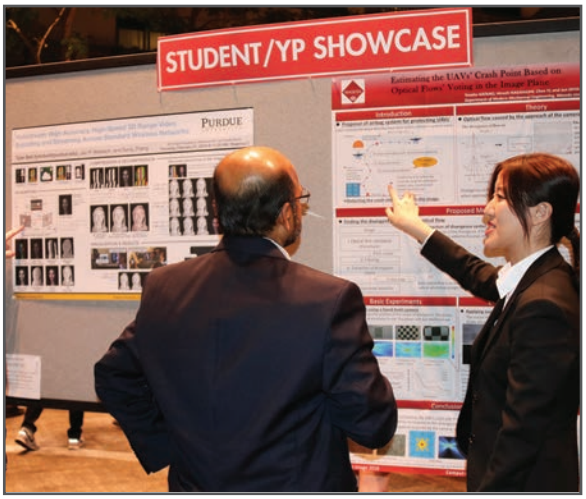

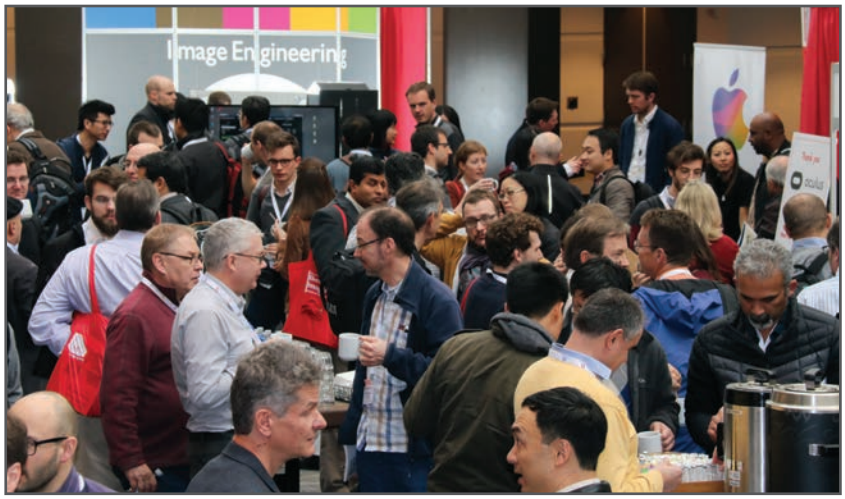

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