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A Low-Voltage 0.7 µm Pixel with 6000 e- Full-Well Capacity for a Low-Power CMOS Image Sensor

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Abstract

A low-voltage pixel with 0.7 µm pitch was designed for a low-power CMOS image sensor. By reducing a pixel power supply voltage (V_{pix}), power consumption for pixel was reduced, but full-well capacity (FWC) was also decreased. However, by lowering the conversion gain (CG) and applying a negative voltage to the ground (N_{GND}) of the pixel, FWC of 6000 e- was achieved without any degradation of both charge transfer lags and backflow noise. In addition, the signal linearity in the reduced analog-to-digital (ADC) range was improved by optimizing the source follower (SF). For dark performances, white spots and dark current worsened by N_{GND} were significantly improved by forcing more negative voltage to the transfer gate (TG) when it was turned off.

Introduction

Several cameras are being mounted on smart mobile devices, and demands for rear cameras with a high resolution of 108-Megapixel are increasing for detailed images. Hence, a pixel pitch has been continuously reduced down to 0.7 µm within a limited optical format and a chip size [1]. For pixel architectures, the Tetracell structure provided a high-sensitivity image in a dark environment by merging four pixels into one. In addition, a re-mosaic function for converting a Tetra pattern into a Bayer pattern provided a high resolution image, and also a dual conversion gain technique provided a wide dynamic range [2]. However, as these functions are used and performances for still shots and videos are enhanced, power consumption has increased. Therefore, it is very important to reduce power consumption for high-resolution CMOS image sensors (CIS).

There are two methods to reduce power consumption in terms of pixel and analog designs: a pixel bias current or a pixel power supply voltage (V_{pix}) reduction. If it reduces the pixel bias current which is the constant current flowing in the source follower (SF) transistor, the signal settling can be delayed and this results in degrading image quality in the high speed operation. In particular, this settling risk becomes more sensitive in the case of large mobile sensors of more than 100 million pixels due to long row drivers. Hence, from the pixel design viewpoint, the reduction in V_{pix} has a relatively small risk as long as voltage is optimally allocated for each portion. In this work, a 0.7 µm low-voltage pixel was demonstrated for a low-power CIS by reducing V_{pix} by 0.6 V.

Pixel engineering for low power

0.7 µm Tetracell pixel architecture

As shown in Fig. 1, a low-voltage pixel has a pitch of 0.7 µm and is formed of full-depth deep trench isolations to completely block electrical and optical crosstalk. In addition, the grid technology in Tetracell structure was used for color filter isolation, so as to prevent the light from moving to adjacent pixels [3].

Voltage budget in pixel

Electron-hole pair is created when photons are absorbed into silicon in a pixel, and the photodiode (PD) is filled with these generated electrons. Subsequently, these stored electrons in PD are transferred into a floating node (FD) when the transfer gate (TG) is turned on. Pixel output signal (V_{out}) which is an input signal of analog-to-digital converters (ADC) is finally determined after converting electrons into voltages unit through SF stage. At this time, it is important that the quantitative range of V_{out} from dark to light condition is determined within the ADC input range.

As shown in Fig. 2, voltage should be assigned to several stages within the pixel. First, clock feedthrough in a reset transistor (RG) occurs when switching from a high state to a low state, thus FD voltage level (V_{FD}) is become lower than the V_{pix}. Then this voltage is changed through SF stage according to the threshold voltage (V_T) and voltage gain in SF. Plus, this decreases slightly by a voltage drop due to channel resistance in selection transistor (SEL) even though it is very small when SEL is turned on. Thereafter the reset voltage level is determined, which indicates the output voltage in a dark environment. Second, a full-saturation voltage level in a light environment must be designed considering the load transistor limitations. Also, the actual ADC range is reduced by process variations occurring during mass production. In conclusion, the maximum output swing range is determined by the difference between the reset level and the full-saturation level, and the image sensor must operate within this range.

Signal linearity and full-well capacity

Although the ADC input range in the conventional pixel is wide enough for the operation of CIS, this range decreases because the reset level is lowered when V_{pix} is reduced, as shown in Fig. 3. V_{out} was cut by the reduced V_{pix} whereas the voltage drops by other transistors such as RG, SF, and SEL were almost same. Lowering the full-saturation level as another method to widen the ADC range was also difficult, because it was defined by the load transistor and the process variations. Hence, it decreased the FD dynamic ranage and thus the V_{out} swing range for the low-power CIS should be reduced within the limited ADC input range.

In addition to the above, it was very important whether the V_{out} signal was linear between the reset level and the full-saturation level. If the signal was not linear, a color distortion occurred during color reproduction with a white balance function. Signal linearity was governed by SF in a pixel thus it was important to design constant V_{out}-to-V_{FD} gain in the operation range. In addition, V_T in SF was necessary to be optimized for the signal linearity; otherwise V_{out} in dark condition can be cut and lowered by V_{pix}. As shown in Fig. 4, the signal linearity in the low-voltage pixel is deviated under low light conditions. However, this was improved with SF threshold voltage and process optimization. As a result, the color distortion of

low-voltage pixels, related to signal linearity, was improved to an equivalent level compared to conventional pixels.

As another problem with the reduced ADC range, the dynamic range was also decreased; because all the full-well capacity (FWC) of PD cannot be reflected in the output signal. That is, the signal in bit units would be fully saturated even if it uses less than the physical FWC of PD. Therefore, in order to reflect all the PD FWC into images, it was necessary to lower conversion gain (CG) which converts electrons into voltage units, according to the reduction ratio of the ADC range. As shown in Fig. 5, CG is reduced by 15% through the adjustment of FD capacitances; thereby the dynamic range increases to match the physical PD FWC of 6000 e-.

Photodiode with negative ground

From an electric potential point of view, there are two problems if the reset level is lowered by V_{pix} reduction. First, as shown in Fig. 6 (a), it gives rise to a backflow from FD to PD when TG switches from a high state to a low state, because a charge splitting occurs according to the reduced FD level [4]. To suppress this, there was a way to lower the high-state level of TG to make the potential difference from the FD level larger. However, this causes insufficient charge transfer when the generated electrons by photons flow from PD to FD, especially if FWC is large, as shown in Fig. 6 (b). As a result, the problems in electric potential resulted in image lags due to the signal loss in FD.

As a way to overcome the above pixel potential limit according to the reduced V_{pix}, a negative voltage is applied to the ground in the pixel, as shown in Fig. 7. The silicon substrate in the pixel could be isolated from that in the logic circuit in a stacked CIS, thus a different ground voltage could be applied between the pixel and the circuit [5-6]. As depicted in Fig. 8, if a negative ground voltage (N_{GND}) is forced -0.6 V as much as the reduced V_{pix}, the electric potential is shifted because FD becomes a floating node after the RG is turned off. As PD potential moves low, PD-to-FD charge transfer became no problem even with the lowered TG voltage. Also, the backflow phenomenon was removed by obtaining a potential gap between TG and FD. In other words, if using N_{GND}, it had the advantage of securing pixel characteristics only with a small potential adjustment related to both FWC and charge transfer. Along with the PD potential profile shifted, it was possible to obtain 6000 e- FWC by lowering CG as mentioned above.

The backflow and transfer lags of the low-voltage pixel are measured compared to those of the conventional pixel, as shown in Fig. 9. As the TG voltage increases, the charge transfer lag was improved whereas the fixed pattern noise was degraded due to the backflow. Conversely, the lower the TG voltage, the worse the transfer lags and the better the backflow. In conclusion, the TG voltage for the CIS operation should be determined within the sweet spot where both the charge transfer and the backflow are minimized. This sweet spot was also moved as the V_{pix} is lowered, indicating that the PD potential was shifted low with the aforementioned N_{GND}.

Dark performances

By applying N_{GND} with low V_{pix}, both RG and SEL voltage could also be lowered considering low V_{FD} and V_{out}. Conversely, it was necessary to increase the absolute value of the low state of TG (N_{TG}), in order to improve the dark current from the defects. As shown in Fig. 10 (a), it is confirmed that the white spot is drastically increased when N_{GND} is more negatively applied. Once the voltage gap between N_{TG} and N_{GND} was decreased, accumulation of holes at the Si-SiO_2 interface on the TG channel was physically reduced, which increased the dark current and white spots. Therefore, to suppress this, N_{TG} should be more negatively applied as well. It is confirmed that white spots are significantly suppressed, as shown in Fig. 10 (b). This indicated that the accumulation of holes increased by widening the voltage gap between N_{TG} and N_{GND}.

The random telegraph signal (RTS), which is a blinking noise in dark conditions, increased as the pixel pitch decreased because the SF gate size became smaller. In addition, as shown in Fig. 11, it is worsened with the reduced V_{pix} in spite of the same SF gate size and process conditions with the conventional pixel. Actually, RTS was physically the same, but there was a difference according to ADC range due to criterion units. That is, it was the same in voltage units, but different in bit units. Through SF size and process optimizations, RTS in bit units was improved better than the conventional pixel.

Conclusion

A low-voltage pixel with 0.7 μm pitch was designed for a low-power CIS. By reducing V_{pix} from 2.8 V to 2.2 V, power consumption for pixel and analog circuits was reduced by 20%. Simultaneously, FWC of 6000 e- was achieved with the low CG in the reduced ADC range, along with applying a negative voltage to the ground of the pixel; thus the dynamic range was increased. Furthermore, since the electric potential of the pixel was merely moved to a low level, the charge transfer lag and the backflow noise were not degraded even with low V_{FD}. For dark performances, it was necessary to control the voltage of TG transistor in order to suppress white spots and dark current generated by N_{GND}. In mobile applications, low power for high resolution CIS is very important to reduce power consumption; therefore a trend is expected to decrease the driving voltage of pixels.

References

[1] H. Kim et al., "A 1/2.65in 44Mpixel CMOS Image Sensor with 0.7μm Pixels Fabricated in Advanced Full-Depth Deep-Trench Isolation Technology," ISSCC, pp. 104-106, 2020.

[2] D. Park et al., " A 0.8 μm Smart Dual Conversion Gain Pixel for 64 Megapixels CMOS Image Sensor with 12k e- Full-Well Capacitance and Low Dark Noise," IEDM, pp. 370-373, 2019.

[3] Y. Lee et al., "World first mass productive 0.8μm pixel size image sensor with new optical isolation technology to minimize optical loss for high sensitivity," IISW, pp. 12-15, 2019.

[4] V. Goiffon et al., "Pixel Level Characterization of Pinned Photodiode and Transfer Gate Physical Parameters in CMOS Image Sensors," JEDS, vol. 2, no. 4, pp. 65-76, 2014.

[5] S. Sukegawa et al., "A 1/4-inch 8Mpixel Back-Illuminated Stacked CMOS Image Sensor," ISSCC, 2013.

[6] C. C. Liu et al., "A 1.5V 33Mpixel 3D-Stacked CMOS Image Sensor with Negative Substrate Bias," ISSCC, 2016.

Author Biography

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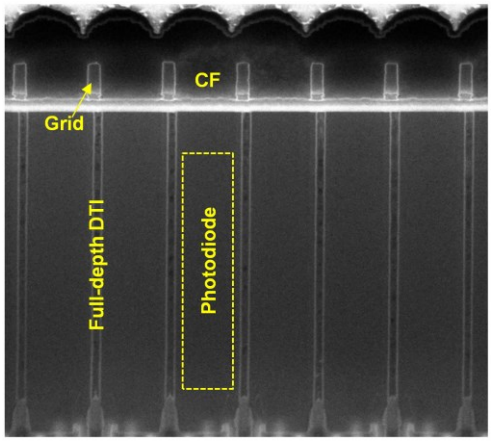

Figure 1. Cross-sectional scanning electron microscope image of low-voltage 0.7 μm pixels.

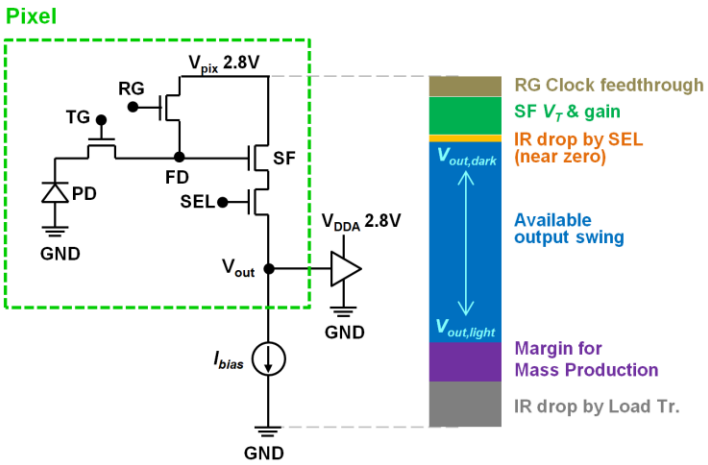

Figure 2. Pixel schematics and voltage budget for each portion.

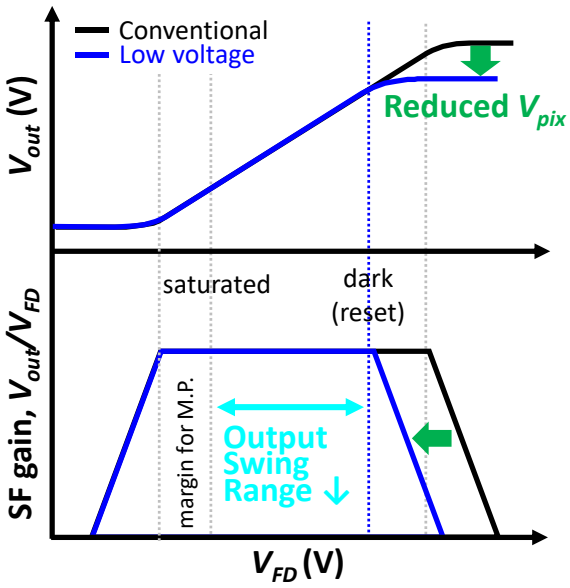

Figure 3. SF gain and possible output swing ranges in the conventional and the low-voltage pixel.

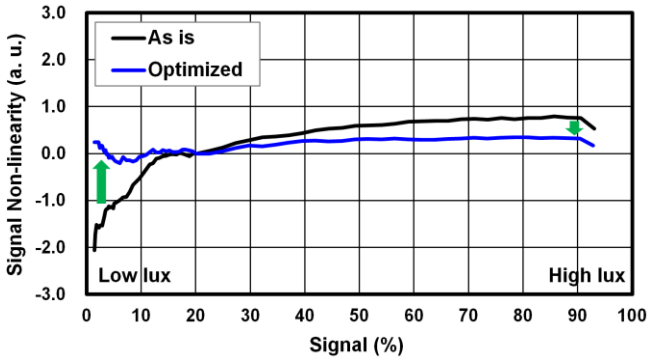

Figure 4. Signal non-linearity before and after optimizing SF transistors.

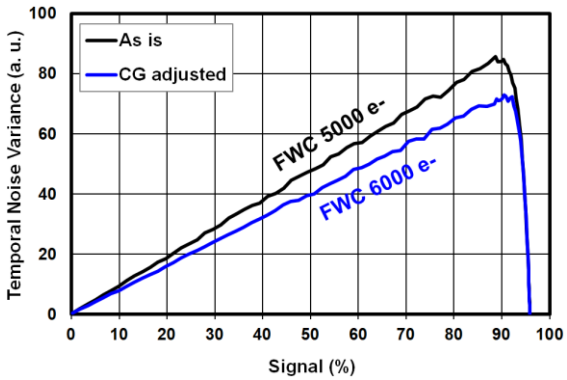

Figure 5. Photon transfer curve before and after adjusting the conversion gain with the reduced V_{pix}.

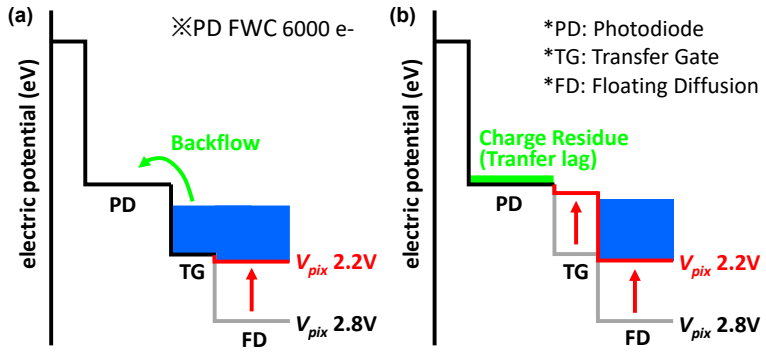

Figure 6. Electrical potential diagrams of (a) the backflow by the lowered V_{pix} and (b) the insufficient charge transfer by the lowered TG voltage.

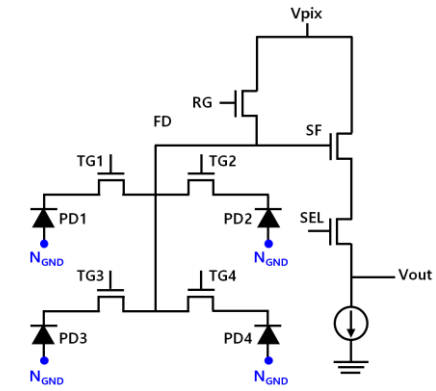

Figure 7. Schematics of the low-voltage pixel with negative ground.

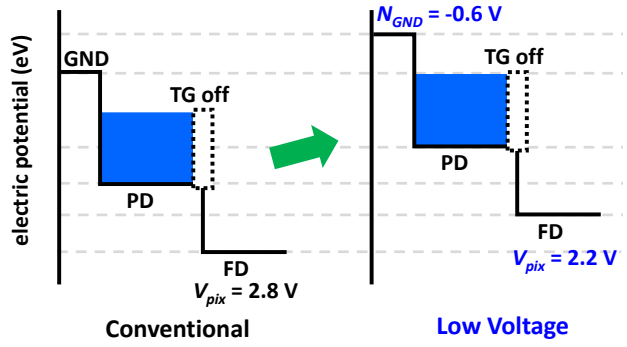

Figure 8. Electrical potential diagrams of low-voltage pixel when a negative voltage is applied to ground in pixel.

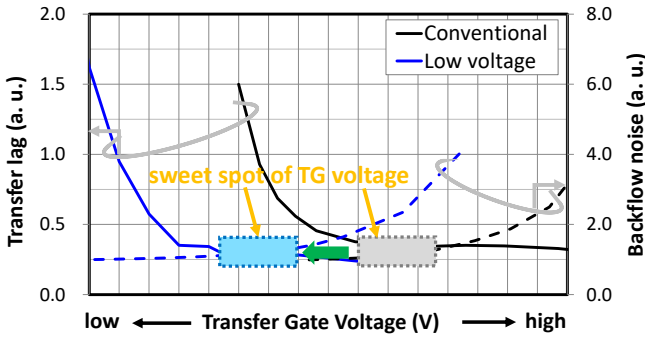

Figure 9. The transfer lags and backflow noise according to TG voltage comparing low-voltage pixel (blue) with the conventional (black). Box with dotted line represents the TG sweet spot for charge transfer operation.

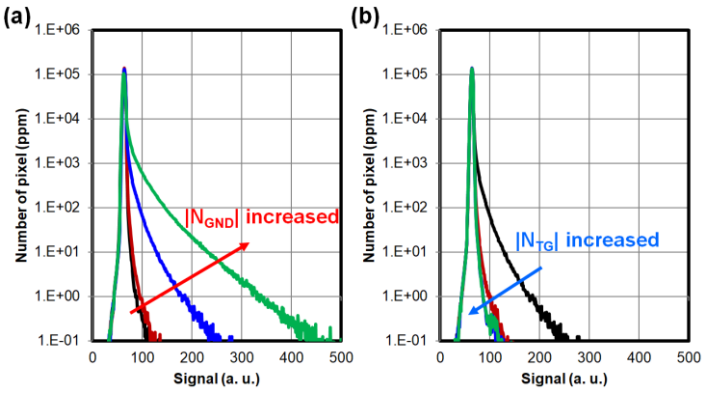

Figure 10. The histogram of dark fixed pattern noise at room temperature when (a) N_{GND} is increased and (b) N_{TG} is increased with applying the N_{GND}.

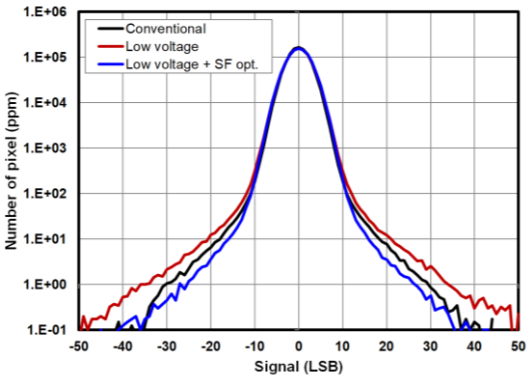

Figure 11. Random telegraph signal curve in bit units obtained by subtracting one frame from another frame in dark conditions.

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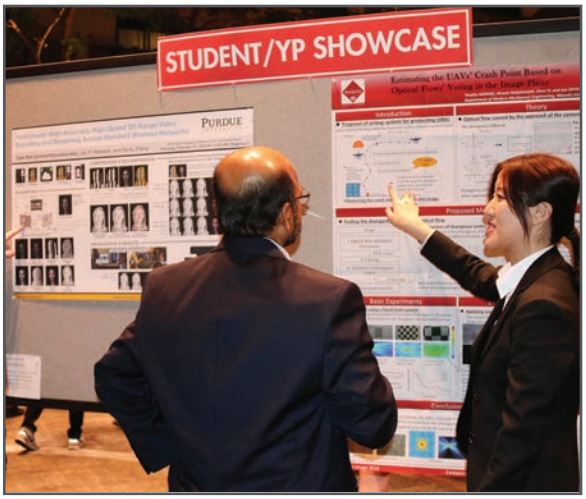

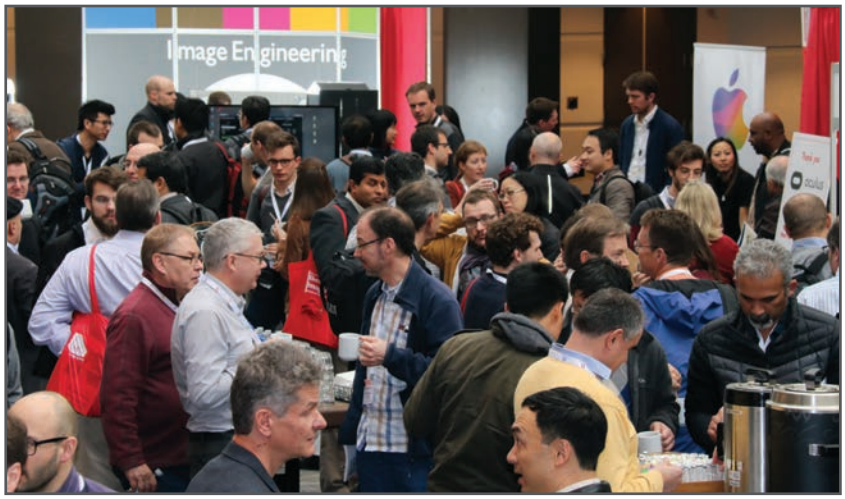

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