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CIS Band Noise Prediction Methodology Using Co-Simulation of Camera Module

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Abstract

This paper describes a CMOS image sensor (CIS) horizontal band noise reduction methodology considering on-chip and off-chip camera module PCB design parameters. The horizontal band noise is a crucial issue for high quality camera of modern smartphone applications. This paper discusses CIS horizontal band noise mechanism and proposes the solution by optimization of design factors in CIS and camera module. Analog ground impedance value and bias voltage condition of pixel array transfer gate have been found to be effective optimization parameters. Through the real experimental data, we proved that proposed solution is instrumental in reducing the horizontal band noise.

Introduction

CIS has been applied for various applications, including smart phones, medical, automobile, security and etc. [1], [2] In addition, as the applications of various fields are developed, the demand for low noise sensors is also increasing. [3], [4], [5] This paper describes the CIS band noise phenomenon, which is crucial in subjective image quality, shown as a band shape in the direction of horizontal in figure 1.

Figure 1. Example of a horizontal band noise. The pixel image at the top of picture shows the deterioration of the horizontal shape.

This paper presents the theoretical background of band noise, countermeasures, and simulation methodology. On the consideration of the module environment where the actual CIS chip is applied, a module design aspect has been experimented. Novelty of proposed approach is to consider both CIS internal circuitry and also module PCB design parameters. Conventional approach for CIS noise has been only focused on CIS design itself, however, our approach also considered the module assembly as it is the final devices applied on smartphones.

CIS Horizontal Band Noise Mechanism

Pixel Operation Principle

It is well known that each pixel consists of four transistors, so called 4-T APS (Active Pixel Sensor), as figure 2 exhibits. Each pixel consists of pinned photodiode, reset gate, transfer gate (TG), source follower (SF), and row select gate. Once photodiode receives light and generates electron and hole pair, TG moves electron to floating diffusion (FD) node. And source follower transfers those electrons as amplified voltage value which is pixel output. It is also input signal to comparator for the next stage, known as Correlated Double Sampling (CDS).

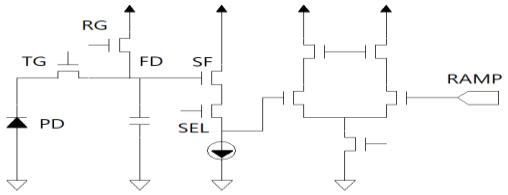


Figure 2. Basic 4-T APS and comparator circuit for A-D converting.

Root-Cause of Horizontal Band Noise

4-T APS Circuit

Horizontal band noise occurs when a quantity of light is highly applied to a pixel. As shown in figure 1, even though it's a dark background picture, the image of the partial row which is contacting a bright source, shows a brighter image than the surrounding area, and it looks like band-shaped noise. The situation of the APS circuit in the dark background column is shown in figure 3 (a), and the situation of the APS circuit in the column where band noise is generated is shown in figure 3 (b). As shown in Figure 3 (a), dark pixel outputs high value of the pixel output voltage (Vout) range. At this time, the load current of each column in that row has the same value (I).

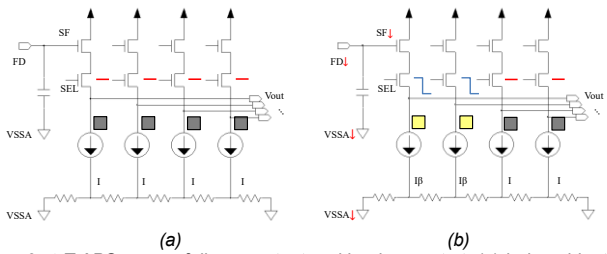


Figure 3. 4-T APS source follower output and load current at: (a)dark ambient light, (b) a high intensity light is incident in partial pixel.

On the other hand, in a circuit that is exposed to light in figure 2 (b), Vout level of the column pixel exposed to strong light source is lower than that exposed to a dark light source. And still the load current is expected to maintain the same value (I).

However, when the Vout level falls below a certain value, the drain-source voltage of the gate, which serves as the current source, is lowered. This means that the current source gate cannot maintain a saturation region, but operates in a linear region. In this region, the lower the drain-source voltage, the lower the drain current, and consequently the load current(Iβ). ($\beta < 1$) This is why the load current changes due to the pixel output exposed to strong light.

Also, the reference ground of the APS circuit, VSSA, ideally maintains the voltage level as 0V, but actually it has some arbitrary impedance value. This results in IR drop, which is proportional to the load current and VSSA impedance value. The important point is that the ground of the pixel load is common to the FD ground, which also affects the FD level. This effect eventually leads to a decrease in the Vout level.

Since the 4T APS circuit, located in the same row, belongs to the same ground line, which affects not only the pixels exposed to strong light, but also other pixel outputs in the same column. Therefore, the pixel output of the corresponding row is lower than the periphery and makes the phenomenon to be shaped as a band pattern which is brighter than the surroundings.

Regulator Characteristics for TG Driving

The other design factor on system is a NTG (Negative voltage Transfer Gate) regulator output capacitor's characteristic. There is a charge pump function inside the CIS to supply power of APS circuit. Since the TG driver requires a positive bias voltage of 4V and a negative bias voltage of -2V, the charge pump circuit must generate a further amplified voltage. [6] The voltage amplified from the charge pump is stabilized through the internal regulator and requires an output capacitor for a ripple rejection. Good load transient responses with small output-voltage is critical to prevent a system error. [7] The negative bias voltage for the TG driver is supplied by the VNTG regulator which is connected with the output capacitor (Cext), and the circuit is shown in figure 4.

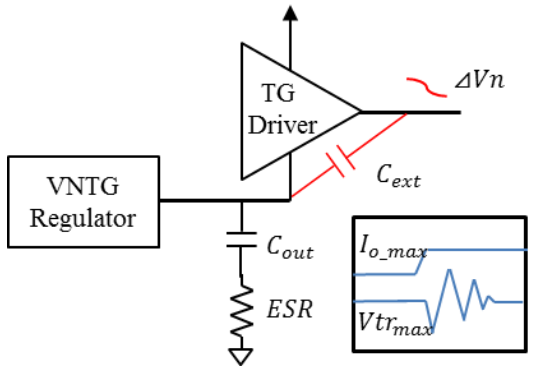


Figure 4. TG driver and regulator with output capacitor. Vtr response at a load current driving.

At this time, the output transient response of the regulator can be modelled by (1)

$$Vtr\_\max = \frac{Io\_\max}{Cout} x\Delta t + Vesr \quad (1)$$

Where Vtr_{max} is maximum transient voltage variation, Io_max is maximum load current, Δt corresponds to the closed loop bandwidth of a regulator. Vesr is the voltage variation resulting from the ESR (Effective Series Resistance) of the output capacitor. [5] Then, when a high intensity light enters, the TG output drops causing a fluctuation (ΔVn). This can be coupled with TG bias voltage. Considering the parasitic capacitor (Cext) between TG output and TG bias, this can be expressed by (2).

$$Vtr\_\max = \frac{(Io\_\max \Delta t + Cext\Delta Vn)}{(Cout + Cext)} + Vesr \quad (2)$$

Given that Cout is about one thousand times that of Cext, it can be observed that the method of lowering Vtr for noise reduction eventually depends on Cout, Io_max, and Vesr.

Modeling and Simulation

CIS Modeling

The standard module schematic of CIS module is shown in figure 5. The unit pixel model consists of the 4-T APS circuit model; photodiode, transfer gate, reset gate and source follower. The on-chip level model reflects the full pixel array information, 4032(H)*3024(V) in 2L8 (Samsung S.LSI 12Mega Pixel CIS). And it includes voltage doubler block for gate driver bias and row decoder driver block for driving main APS gate such as TG, RG, and SEL.

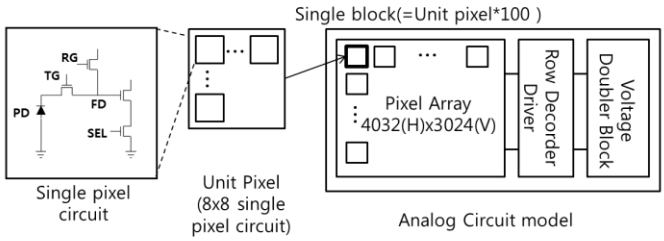


Figure 5. Proposed CIS modeling for horizontal band noise. Unit pixel consists of 8x8 single pixel circuits. A combination of 100 unit pixels constitutes a single block, and this block completes the final 4032x3024 array.

Module PCB Modeling

The module PCB model consists of wire bonding, rigid PCB, FPCB, and connector block, as shown in figure 6. It includes external power supply path and regulator output capacitor path. This model can provide a practical and realistic advantage in that it can reflect the design parameter such as RLC value of PCB pattern to which CIS can be applied. It is also adapted to the mutual parameters of the PCB pattern of the actual camera module in order to enhance its modeling suitability

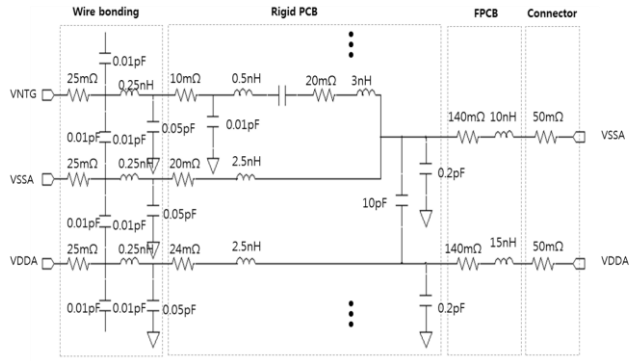


Figure 6. Proposed module PCB modeling for horizontal band noise.

Simulation Methodology

The CIS horizontal band noise simulation methodology, shown in figure 7, consists of on-chip part and module part. The on-chip part starts with CIS gate-level schematics which include 4-T APS, voltage doubler block and row driver block. Then, the physical RC parameters of the APS circuit path are added to the gate-level circuit information to create an on-chip level RC model. On the other hand, the PCB is designed based on the module circuit schematic. The PCB design file is converted to 3D modeling. The 3D modeling of the PCB can reflect not only the pattern information per layer but also mutual coefficient information such as mutual capacitance between patterns. Impedance simulation by frequency sweep is performed based on the 3D PCB modeling. The output can be extracted as a matrix form consisting of RLGC and coefficients. The next step is to combine the on-chip level model with the previously extracted module PCB information. When the input of the timing about switching operation of the entire gate is complete, the final module-level band noise simulation step is then finished.

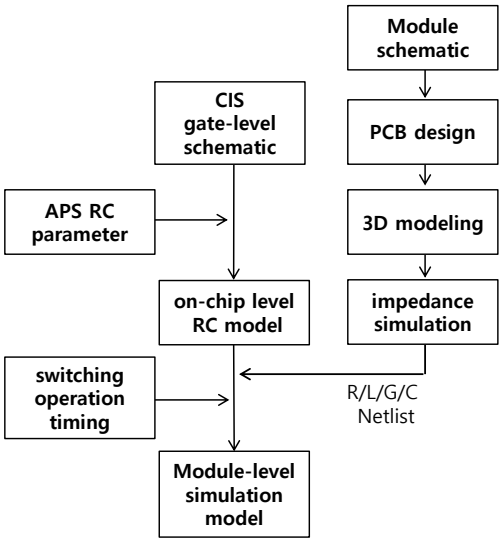


Figure 7. Proposed CIS horizontal band noise simulation methodology.

Experimental Results

Previously, most CIS noise has been experimented using dedicated test chips or using only small CMOS circuit. Our experimental CIS is a mass production sensor combined with a real module's printed circuit board, not a package test board, so it is equivalent to the actual assembled camera module measurement environment.

For the measurements of band noise, the horizontal LED light is exposed to only half of CIS and then the CIS column output is observed at the opposite side of LED light. The band noise is calculated as the difference in voltage output level between the band shape pixel area and the normal pixel area based on the band shape boundary line.

Analog Ground Impedance

Figure 8 shows the noise voltage value according to the VSSA impedance of the module PCB. This analog ground is the path shared by the APS 4-T of the CIS and the module PCB. It demonstrates the noise voltage reduction as the analog ground impedance decreases both measurement and simulation. An image of noise test with a change in analog ground impedance value is shown in Figure 9. In the image (b) of the CIS module with low impedance, the band noise shape is blurred.

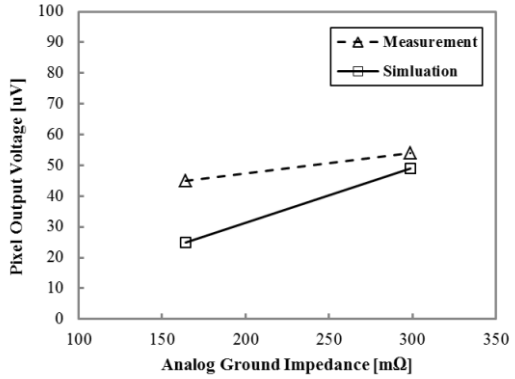


Figure 8. Comparison of measured and simulated horizontal band noise voltage with analog gain(x16) by VSSA impedance

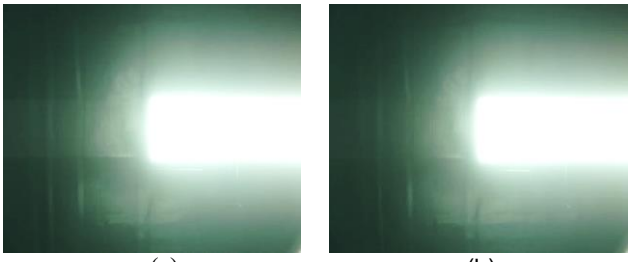


Figure 9. Horizontal band noise image when: (a) Analog ground impedance is 299mΩ, (b) Analog ground is 164mΩ

Regulator Output Capacitor Value

Next, the experimental results on the output capacitor value of the NTG regulator (Cout) has been discussed. The measurement noise is 56uV when the output capacitor value is 9.4uF, while it is lowered to 35uV when the capacitor value is 23.5uF. In the same situation, the simulation value decreases from 54uV to 21uV. Overall measurement and simulation values, and trends are shown in figure 10. Figure 11 shows a noise test image with 8.8uF and 23.5uF applied to the regulator output capacitor, respectively. The

noise shape is blurred in the image (b) of the module to which 23.5 uF is applied, rather than the image (a) of the module to which 8.8 uF is applied.

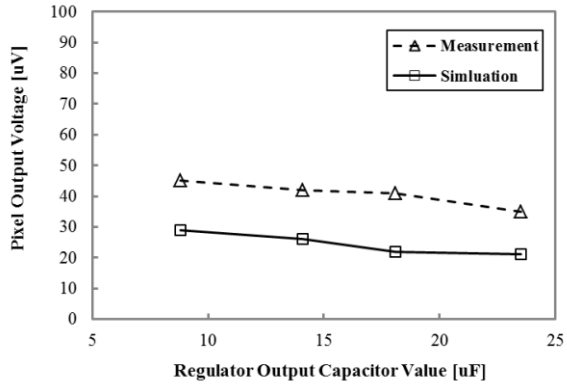
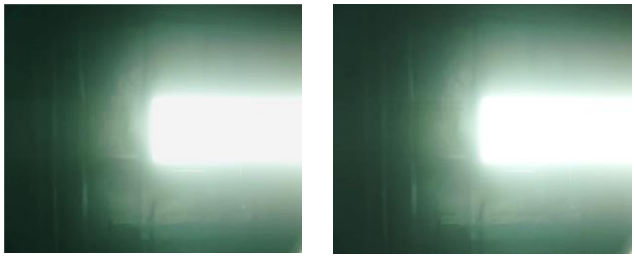


Figure 10. Comparison of measured and simulated horizontal band noise voltage with analog gain(x16) by NTG capacitor value.



(a) (b)

Figure11. Horizontal band noise image when: (a) NTG capacitor value is 8.8uF, (b) NTG capacitor value is 23.5uF

Conclusion

This paper proposed a realistic and effective module-level CIS noise-band simulation methodology. It is possible to reduce noise by optimizing design parameters of camera module PCB and CIS. This has been confirmed through both measurement and simulation. And the simulation implemented based on 12MP pixel sensor modeling, and this modeling can also be extended to image sensors of more than 100 million pixels.

The novelty of proposed methodology is that it can represent the actual operating environment of CIS by applying the simulation model combining CIS and camera module. While some of IC simulation includes the fixed package model, this methodology extended to the camera module model which considers the actual design parameter. In addition, considering the trend of increasing application of high-resolution cameras to high-end smartphones, consideration of NTG capacitor characteristics is an approach that can overcome the limitations of CIS's built-in regulator output performance. Moreover, high-resolution trend requests more pixel of CIS, a possibility of horizontal band noise occur increases due to a high TG driving current and coupling by intensive structure. Therefore, it is important to establish such a prediction modeling and simulation system environment.

This methodology is expected to be very useful in the perspective that it can be used for verification of the preliminary design ahead of the mass production. Also, it can be utilized for the study of on-chip sensor design in real product environment, as well as noise reduction effect of various host device model in research stage.

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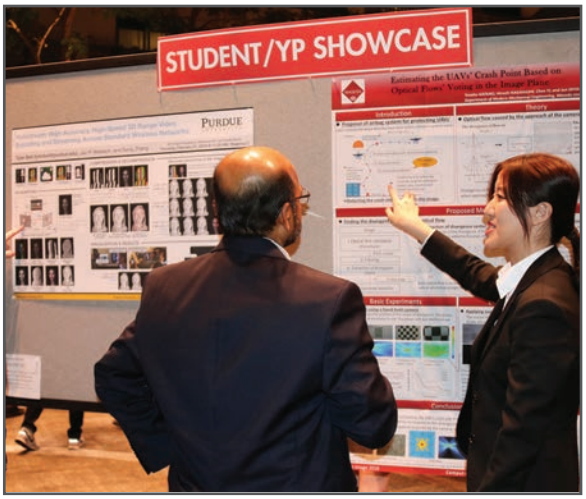

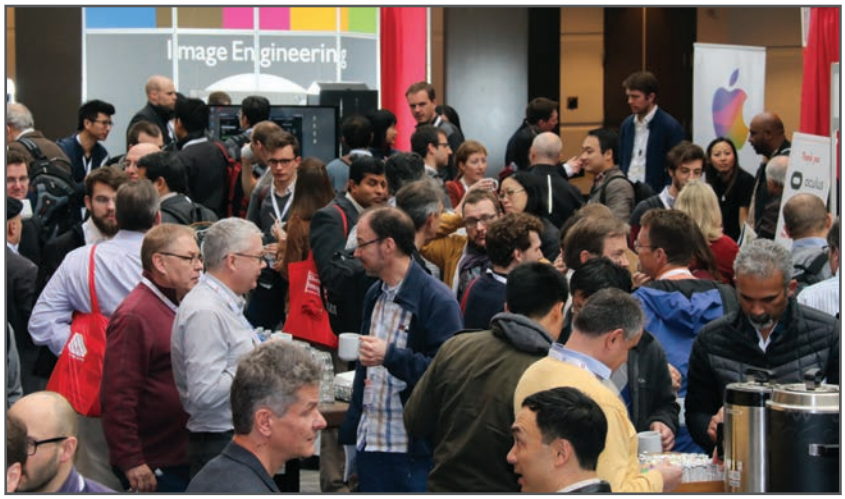

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