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An Over 120dB Dynamic Range Linear Response Single Exposure CMOS Image Sensor with Two-stage Lateral Overflow Integration Trench Capacitors

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Abstract

This paper presents a prototype linear response single exposure CMOS image sensor with two-stage lateral overflow integration trench capacitors (LOFITreCs) exhibiting over 120dB dynamic range with 11.4Me$^-$ full well capacity (FWC) and maximum signal-to-noise ratio (SNR) of 70dB. The measured SNR at all switching points were over 35dB thanks to the proposed two-stage LOFITreCs.

Introduction

In recent years, sensing technology using CMOS image sensor (CIS) has been widely used. Some sensing applications in automotive, medical, factory automation fields need to capture subjects with strong contrast of light illumination. For CIS in those usage, wide dynamic range (WDR) with linear response is highly required. In addition, for WDR image sensors types synthesizing multiple signals over different illuminances, in order to obtain a high-quality image, the signal-to-noise ratio (SNR) of over 32dB is needed at the switching point of signals [1].

Several WDR technologies have been reported so far; logarithmic compression [2-7], multiple exposure [8-15], combination of photodiodes (PDs) [16-19], dual conversion gain [20-22], lateral overflow integration capacitor (LOFIC) [1, 23-27] and lateral overflow integration trench capacitor (LOFITreC) [28], and combinations of above [29-32]. The logarithmic compression approach utilizes the logarithmically compressed photocurrent output by using the sub-threshold characteristic of MOSFET in high light condition. The multiple exposure approach captures some images with different exposure times. The approach with combination of PDs captures an image with multiple PDs with different size or light sensitivity in a single exposure. The dual conversion gain approach changes conversion gain (CG) by controlling a switch connected to a capacitor and floating diffusion (FD) in a pixel during horizontal blanking period. The LOFIC and LOFITreC approach accumulates overflow-electrons from PD and FD capacitor and reads out signals with different sensitivity in a single exposure. This approach allows independent design of CG and full well capacity (FWC). Previously reported LOFIC CIS achieved 100dB dynamic range (DR) and over 32dB SNR at switching point [24]. However, achieving both single exposure WDR over 120dB and over 32dB SNR at switching points is still challenging [16, 21, 31].

The purpose of this work is to develop a CIS with an over 120dB DR and over 32dB SNR at all switching points. In order to achieve high SNR at the switching points, two-stage LOFITreCs is newly developed. The structure and performances of the developed CIS are described as follows.

Developed image sensor

Figure 1 shows the circuit block diagram of the developed CIS. The pixel consists of a pinned PD, a transfer gate (T), a FD, a source follower driver (SF), a select switch (X), a first overflow switch (S1), a LOFITreC1, a second overflow switch (S2), a LOFITreC2, and a reset gate (R). In this work, the 67fF LOFITreC1 and 1.5pF LOFITreC2 are integrated adjacent to the PD. The values of the capacitances are designed to achieve sufficient SNR at signal switching points. The developed prototype chip has three pairs of parallel analog outputs and they are converted by differential analog-to-digital converters (ADCs) outside the chip. When column-parallel ADCs are introduced, its suitable circuit architecture needs to be examined.

Figures 2 and 3 show the operation timing diagram and the potential diagram of the two-stage LOFITreCs operation, respectively. After the PD reset, a reset signal for the highest FWC signal S3 converted at FD+LOFITreC1+LOFITreC2 is read out at t1. A reset signal for high FWC signal S2 converted at FD+LOFITreC1 is read out at t2. When a high intensity light is irradiated to the pixel during the integration period (t3), overflow photoelectrons from PD and FD are accumulated in the LOFITreC1 and overflow photoelectrons from LOFITreC1 are accumulated in the LOFITreC2. A reset signal for high sensitivity signal S1 converted at FD is read out at t4. Photoelectrons accumulated in the PD are transferred to the FD at t5. A high sensitivity signal converted at small capacitance FD (S1) at t6, a high FWC signal converted at FD+LOFITreC1 (S2) at t7 and a highest FWC signal converted at FD+LOFITreC1+LOFITreC2 (S3) at t8 are read out to achieve WDR under a single exposure.

Figure 4(a) shows the layout of the 16μm pitch pixel of the prototype CIS developed in this work and 4(b) shows the pixel cross sectional diagram. The trench capacitors were integrated inside each pixel as LOFITreCs to achieve high FWC and a sufficiently high fill factor (FF). The TEM images of LOFITreC are shown in Figure 4(c-d). A deep p-well (DPW) was formed around the LOFITreC in order to form a potential barrier between inversion layer of LOFITreC and the buried n-type layer of pinned PD. The concentration of DPW was optimized to obtain a uniform capacitance in the signal range of LOFITreC. To suppress leakage current of charge integration node of LOFITreC, overflown-photoelectrons from PD and FD capacitance are accumulated at the n^+-doped poly-Si buried electrode. The inversion layer induced at the Si substrate side interface and n^+ layer are connected to ground.

Chip measurement results

Figure 5 shows the micrograph of the fabricated chip with $128^H \times 128^V$ effective pixels. The number of pixels is easily extendable under the same design. The chip was fabricated by using a 0.18μm 1-Poly-Si 5-Metal layer CMOS image sensor technology

with 20μm thick p-epitaxial layer on n-type Si substrate. The die size is $3.65mm^{H} \times 4.64mm^{V}$.

Figure 6 shows the measured photoelectric conversion characteristics of the developed CIS. An over 120dB WDR with linear response was obtained by S1, S2 and S3 signals under a single exposure. The FWC of S1, S2 and S3 were 17.8ke$^-$, 50.9ke$^-$ and 11.4Me$^-$. And the spatial efficiency of the FWC were 69.5e$^-$/μm^2, 199e$^-$/μm^2 and 44.5ke$^-$/μm^2, respectively. The SNR at S1/S2 and S2/S3 switching points were 35dB and 47dB, respectively. The high SNR at two switching points were successfully achieved due to the introduced two-stage LOFICTreCs.

Figure 7 shows the sample images of a light bulb, a grayscale chart, printed paper and two stuffed animals captured at 285fps with F# 4.0 lens. The stuffed animal on the left was illuminated with high intensity lights from both its front and back to simulate the gray phenomenon. The other stuffed animal on the upper right was placed in a dark box. Figure 7(a), 7(b) and 7(c) were captured by the S1, S2 and S3 signals, respectively. The S1 signal captured the upper right stuffed animal under low light condition. The S2 signal captured the printed paper on the back and the grayscale chart under high light condition. The S3 signal captured the bulb filament and the stuffed animal on the left under very high light condition. The results show that the developed CIS exhibits a single exposure WDR performance.

The performances of the developed CIS are summarized in Table I.

The pixel pitch can be scaled while maintaining its high spatial efficiency of FWC thanks to the LOFITreC. In addition, backside illumination and stacking technologies can increase the spatial efficiency of FWC further even if decreasing the pixel pitch.

Conclusion

In this work, a CMOS image sensor with two-stage LOFITreCs was presented which achieved over 120dB WDR with linear response and over 35dB SNR at all switching points in a single exposure. The developed CMOS image sensor is highly adaptive to many applications with strong contrast of light illumination.

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Author Biography

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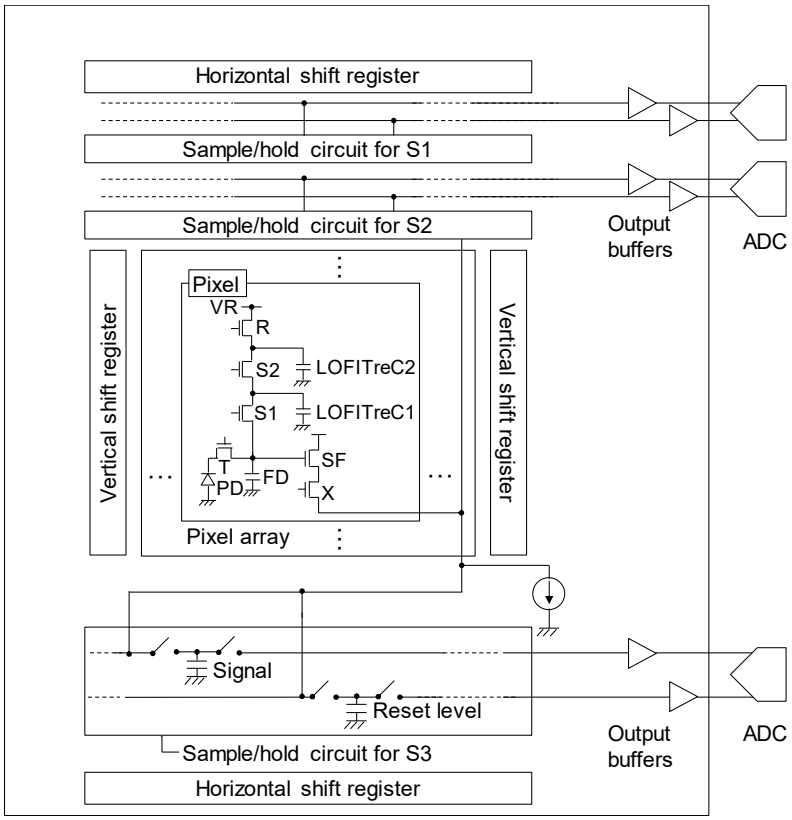


Figure 1. Circuit block diagram of the developed CMOS image sensor with two-stage LOFITreCs

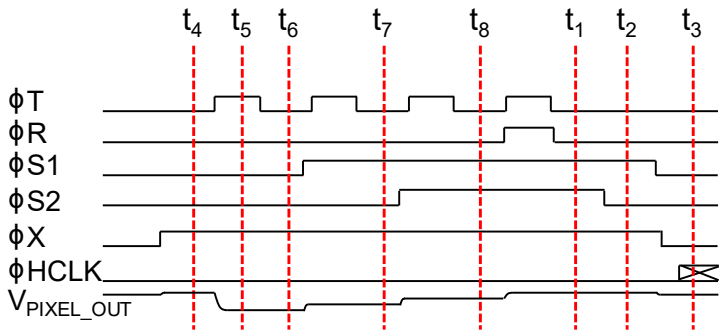


Figure 2. Timing diagrams of two-stage LOFITreCs operation

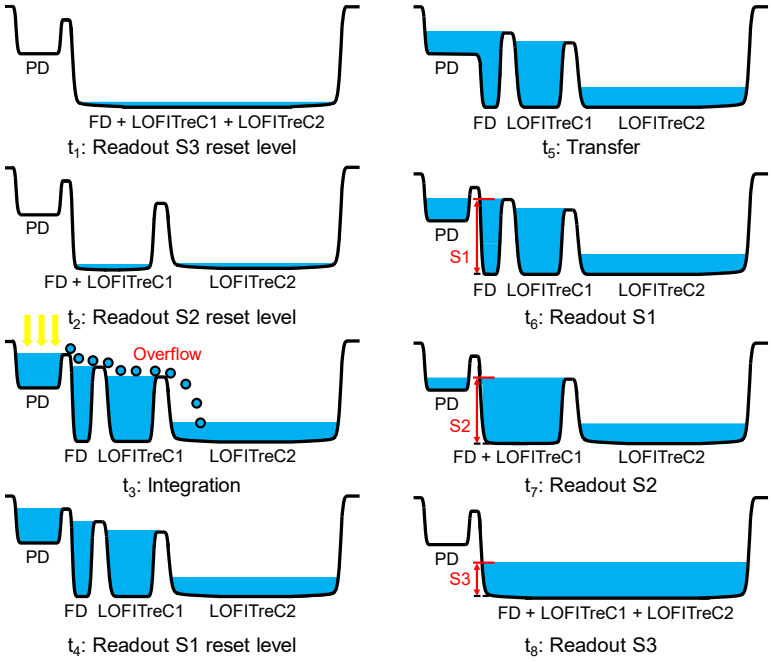


Figure 3. Potential diagrams of a two-stage LOFITreCs operation

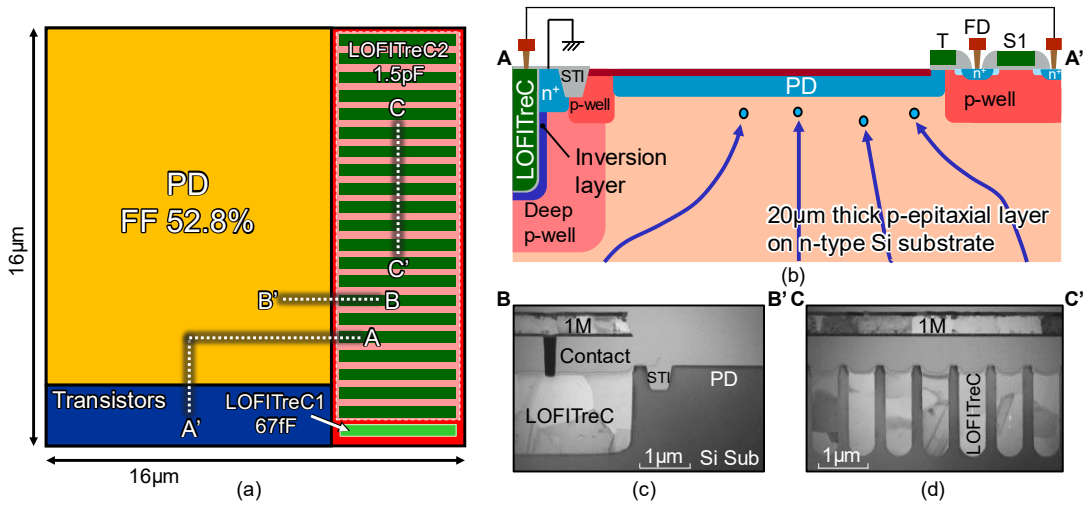


Figure 4. (a) Pixel layout and (b) pixel cross sectional diagram of line A-A', and cross sectional TEM images of (c) line B-B', (d) line C-C'

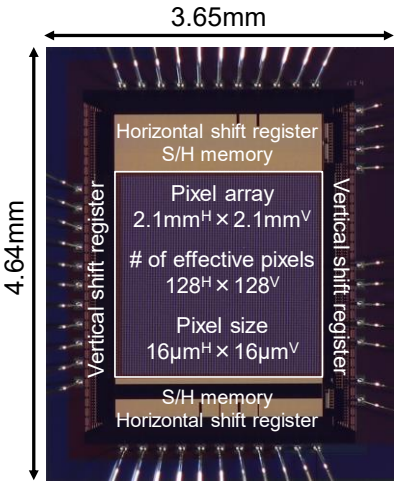


Figure 5. Micrograph of the developed CMOS image sensor chip

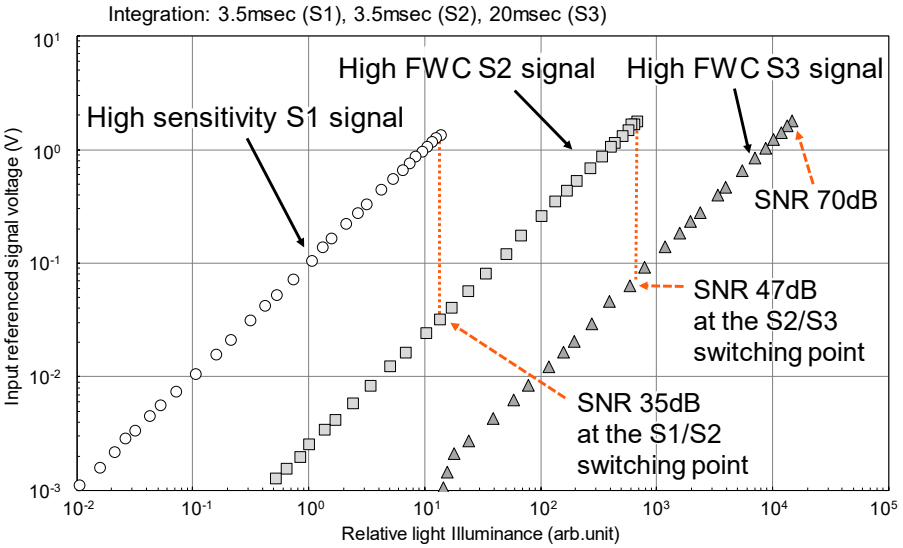
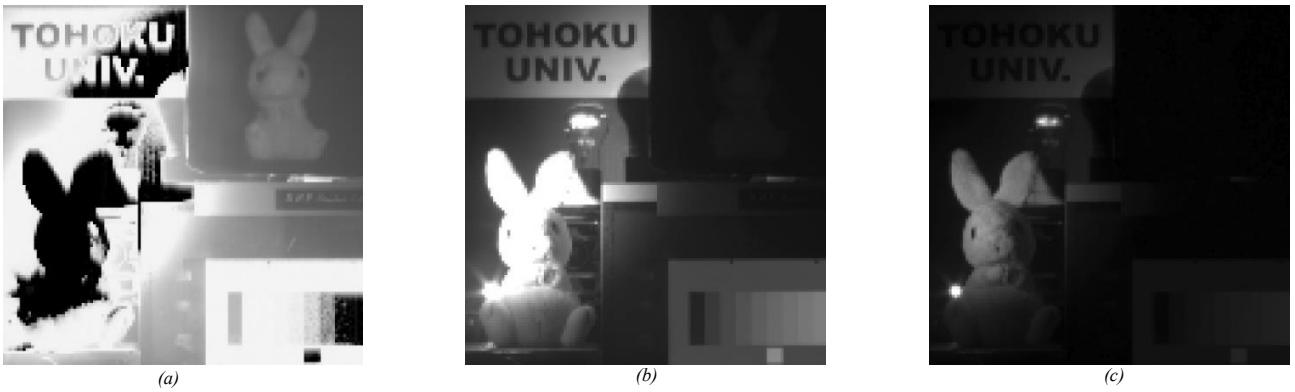


Figure 6. Measured photoelectric conversion characteristics



(a) *(b)* *(c)*

Figure 7. Sample images by (a) S1, (b) S2 and (c) S3 signals captured at 285fps with F# 4.0 lens

Table 1. Performance summary of the developed CMOS image sensor

Process technology		0.18μm 1-poly-Si 5-Metal CMOS with pinned PD
Power supply voltage		3.3V
Die size		3.65mm^{H} × 4.64mm^{V}
# of effective pixels		128^{H} × 128^{V}
Pixel size		16μm^{H} × 16μm^{V}
Fill factor		52.8%
Maximum frame rate		685fps @ 20MHz
Capacitance	FD	2.1fF
	LOFITreC1	67fF
	LOFITreC2	1.5pF
FWC (Spacial Efficiency)	High sensitivity S1	17.8ke^{-} (69.5e^{-}/μm^{2})
	High saturation S2	50.9ke^{-} (199e^{-}/μm^{2})
	High saturation S3	11.4Me^{-} (44.5ke^{-}/μm^{2})
SNR	S1/S2 switching point	35dB
	S2/S3 switching point	47dB
	Maximum S3	70dB
Dynamic range		>120dB
Spectral sensitivity range		200nm-1100nm

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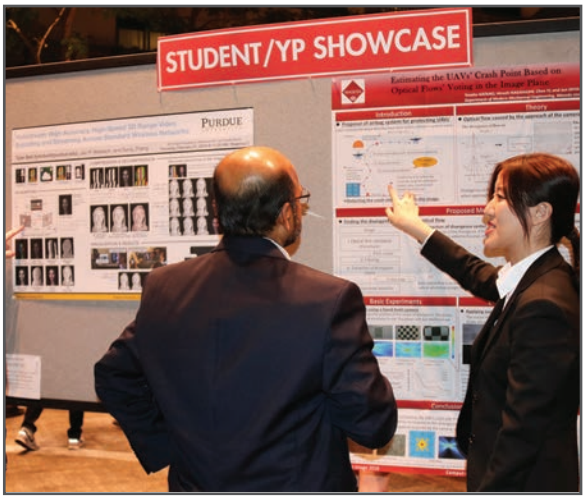

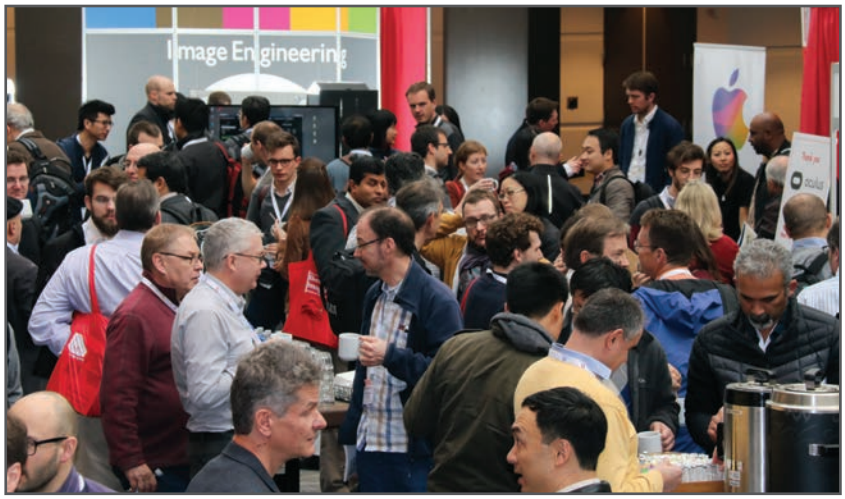

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