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A 4-tap global shutter pixel with enhanced IR sensitivity for VGA time-of-flight CMOS image sensors

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Abstract

An indirect time-of-flight (ToF) CMOS image sensor has been designed with 4-tap 7 µm global shutter pixel in back-side illumination process. 15000 e- of high full-well capacity (FWC) per a tap of 3.5 µm pitch and 3.6 e- of read-noise has been realized by employing true correlated double sampling (CDS) structure with storage gates (SGs). Noble characteristics such as 86 % of demodulation contrast (DC) at 100MHz operation, 37 % of higher quantum efficiency (QE) and lower parasitic light sensitivity (PLS) at 940 nm have been achieved. As a result, the proposed ToF sensor shows depth noise less than 0.3 % with 940 nm illuminator in even long distance.

Introduction

Depth sensors are used for numerous applications such as augmented reality (AR), 3D scanning and automotive [1]. Time-of-flight (ToF) is a method to measure the round-trip time of flight has been used in light detection. Indirect ToF sensor which is implemented on a standard CMOS process with low operating voltage can be more suitable for mobile devices.

Recently, due to strong demands for high resolution of ToF sensors in consumer electronic market, development of high performances of small size ToF pixel has been required. Especially, since low read-out noise and high infra-red (IR) sensitivity are directly related to depth error characteristics as shown in (1) [2], low noise pixel design having enhanced IR sensitivity is highly recommended.

$$\sigma_{\text{depth}} = \frac{c}{4\sqrt{2}\pi f_m} \cdot \frac{1}{DC \times SNR_{light}} \qquad (1)$$

In addition, optimizations of pixel layout and doping conditions are required to obtain high demodulation contrast (DC) with low power consumption and low parasitic light sensitivity (PLS) which makes it possible to offer stable depth information under strong sunlight. In this paper, we introduce VGA ToF sensor with 7 µm pitch pixel containing suitable structures for improving 940 nm wavelength depth performances.

Electrical engineering

Pixel architecture for 4-tap global shutter

We introduce four in-pixel charge storages individually corresponding to 4-taps in a pixel for high performance depth sensing. As shown in Fig. 1, four photo-gates (PGA, PGB, PGC and PGD) represent 0º, 90º, 180º and 270º sampling, respectively [3]. A 4-tap pixel has four taps in a pixel so that 4-phase sampling can be performed in one frame. The PGs are rotationally arranged to suppress a tap asymmetry by minimizing transfer path of charges, because electrons with low mobility could be irregularly added on taps during high frequency modulation of PGs.

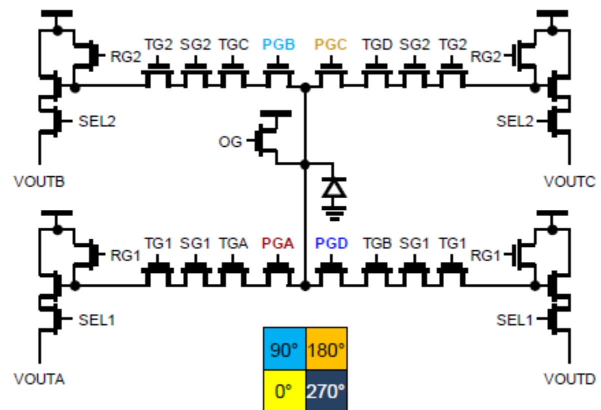

Figure 1. Schematic of 4-tap pixel with 4-PGs and 4-SGs for 4-phase sampling.

Fig. 2 shows schematic of pixel structure with optimized optical structure and doping conditions for improving depth noise performance. In this ToF sensor, photo-generated electrons are collected through a photodiode (PD) enhanced by a PG at first. High and low voltage biased PGs with modulation frequencies guide them into corresponding storage diodes (SDs). Particularly, these SDs are in the form of a pinned diode by a biasing on MOS storage gate (SG) to enable global shutter operations for the modulation of the entire pixel array.

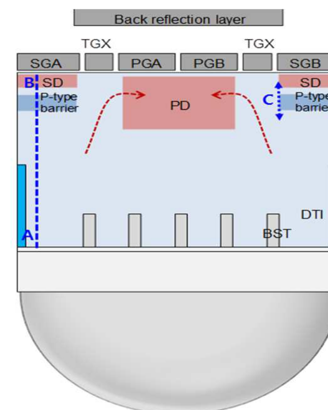

Figure 2. Pixel structure with optimized optical structures and doping conditions for improving QE, PLS and DC.

Pixel design for low read-noise and high saturation

Fig. 3 shows potential diagrams during the operation. In this ToF sensor, charge transfer and its storage for global shutter is possible with true correlated double sampling (CDS) operations. For global reset, charges in PDs and SDs are drained through overflow gates (OGs) and transfer gates (TGs), respectively. SG has low voltage during global reset since it helps charge transfer from SD to floating-diffusion (FD). On the contrary, during the integration, high voltage is applied to SG for proper signal transfer from PDs to SDs, as shown in (2) of Fig. 3. After the integration, conventional rolling readout operation is employed. The stored charges at each SD are transferred to FD node during readout time. To achieve the enhanced transfer characteristics from SD to FD, low voltage level is applied to SGs as same with global reset. SD structure using these read-out operations in ToF sensor allows true CDS operation which effectively reduces the read-noise to about 3.6 e-. With this SG voltage operation and high doping structures, large full well capacity (FWC) of SD has been realized. The proposed structure with 3.5 µm pitch of taps achieved 15000 e-/tap (60000 e-/pixel) while simultaneously transferring electrons perfectly.

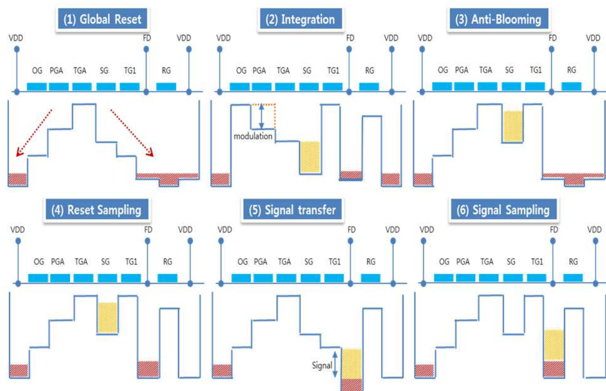

Figure 3. Potential diagrams of charge storing and transferring operations with true CDS operations for global shutter.

Optimization of doping structure for DC and PLS

Considering power consumption, the PG voltage range is designed to be low and depletion region is also limited. PD with low-dose doping conditions is used for fast charge transfer with expanding depletion region in deep silicon. Fig. 4 (a) shows simulated potential profile of the PD having optimized doping conditions. As expected, it is found that drift field affects electrons in deep silicon region. Moreover, Fig. 4(b) is experimental results that DC and PLS could be improved by formation of sufficient drift field in PD.

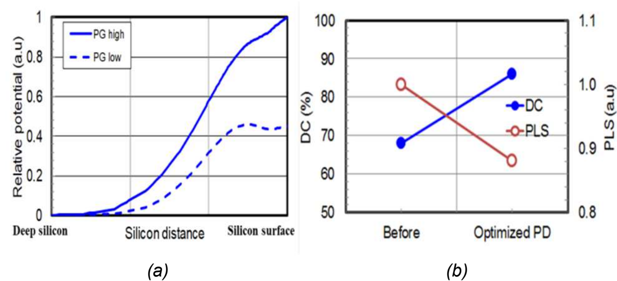

Figure 4. (a) Potential profile in vertical direction of pixel with optimized PD and (b) measurement results for PLS and DC.

Therefore, 86 % of DC is realized while PLS is suppressed. Fig. 5 (a) shows the changes in simulated potential profile according to energy of implantation for p-type barrier. Fig. 5 (b) is experimental results of PLS at each condition of implantation. These results indicate that PLS could be reduced by controlling of potential barrier near SDs (C in Fig. 2). It is considered that reduced size of SDs and increased potential barrier from PDs to SDs induce decreases in components of PLS. As a result, we achieved 24 % relatively reduced PLS with low implantation of p-type near SD.

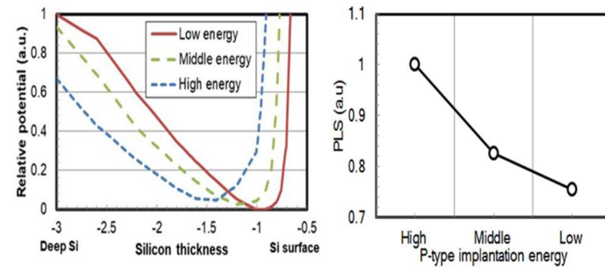

Figure 5. (a) Potential profiles (A-B in Fig. 2) according to energy of implantation for p-type barrier and (b) experimental results of PLS at each condition of implantation.

Measurement results

Fig. 6 shows simulated and measured result of depth noise according to distance and table is for summary of electrical performances. 15000 e- of high FWC and 86% of DC have been achieved with low noise structures. Depth noise for 90 % reflectivity chart is measured as < 0.3 %. This indicates that low read-noise is useful to achieve good depth performance in low-light conditions corresponding to long distance usages in indoor environment. As the larger read-noise, the depth noise at long distance deteriorates. Depth noise of the designed ToF sensor with true CDS isn't increased even at long distance due to low read-noise of 3.6 e-.

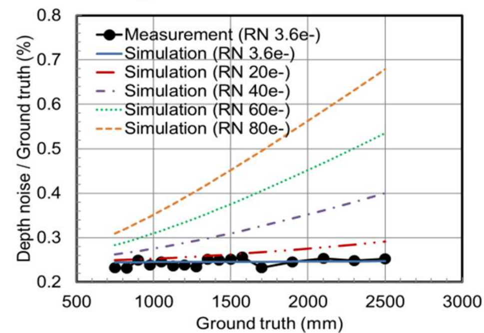

Figure 6. Effect of read-noise on depth noise at long distance.

Optical engineering

IR sensitivity Enhancement pixel structures

Although 940 nm vertical cavity surface emitting laser is used for low ambient light, quantum efficiencies (QEs) of typical CMOS image sensors are very low about 10~20 % at that wavelength. Thus, IR sensitivity enhancement structures are required in small pixel sensors. Thus, we employed several pixel process technologies such as anti-reflection layer (ARL) modification, backside scattering technology (BST) and silicon thickness increment.

First, modification of ARL has been investigated for enhancement of transmittance at IR region. Generally, ARL is comprised of multiple composition layers and its transmittance is determined by thickness of each layer. In this study, 99 % of transmittance at 940 nm has been achieved by controlling thickness of individual layer in ARL structure (shown in Fig. 7).

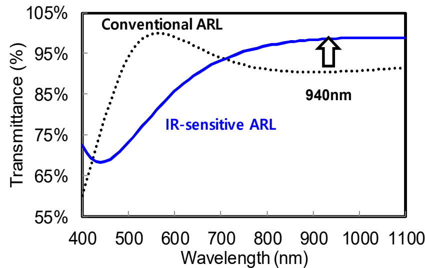

Figure 7. Enhanced transmittance of ARL at 940nm compared to conventional ARL.

Second, in order to increase IR QE with constant silicon thickness, we introduce light scattering structures such as BST on the center of pixel, which increase the light traveling path in silicon. The enhancement of IR sensitivity comes from the increase of effective silicon thickness. Light scattering and multiple reflections are generated by deep trench isolation (DTI) and BST structures with lower refractive index than that of silicon. The scattered beam by BST is illustrated in Fig. 8. IR QE is relatively increased by about 57 % in practice, compared to conventional structures. A deterioration of crosstalk by scattering light has been mitigated by applying DTI structures between pixels and lowering the depth of BST. However, scattering also contributes on the PLS deterioration because of increases in direct penetration into SD node.

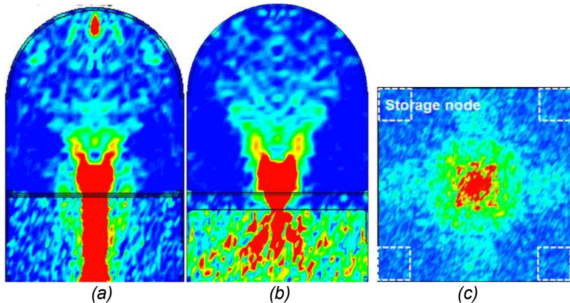

Figure 8. IR beam profile of pixel (a) without BST (b) with BST using finite difference time domain optical simulation tool. (c) Location of SD node considering of PLS due to diffraction pattern of light.

To deal with PLS deterioration by scattering light due to BST, increasing silicon thickness can be a good approach. Thicker silicon make PLS smaller because of the increase of distance for light to reach SD node while absorption in PD for IR QE is increased. In addition, considering the PLS, four SGs should be placed in the pixel corners, as shown in Fig. 8. Conventionally, increasing silicon thickness causes degradation of DC due to insufficient field by low voltage of PGs [4]. However, optimized PD doping enables advanced DC performance even in thick silicon.

Measurement results

Consequently, 37 % of QE having lower PLS at 940 nm has been achieved by optimized ARL, employed BST and increased silicon thickness (shown in Fig. 9). Fig. 10 shows the QE data for designed pixel. The depth noise of the ToF sensor with thick silicon has been improved in proportion to square root of IR sensitivity without a deterioration of DC as shown in Fig. 11. Fig. 12 shows measured depth data and depth accuracy according to ground truth.

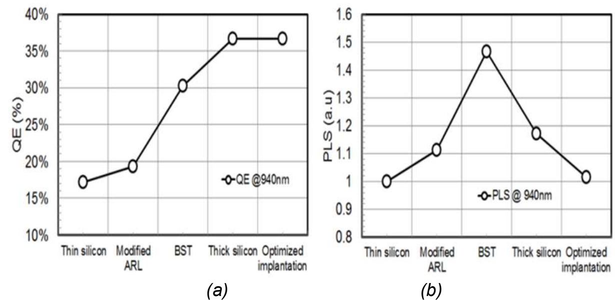

Figure 9. Pixel structure dependence of (a) QE and (b) PLS at 940 nm.

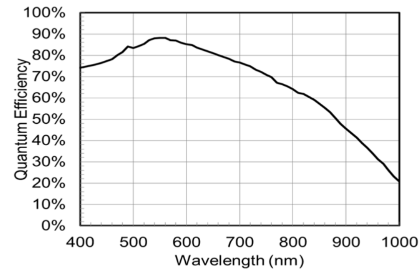

Figure 10.Measured QE curve of IR sensitivity enhanced pixel.

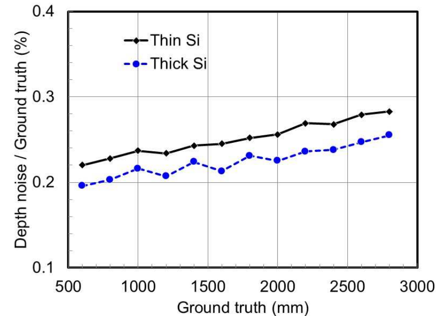

Figure 11. Comparison of measured depth noise between structures with thin and thick silicon.

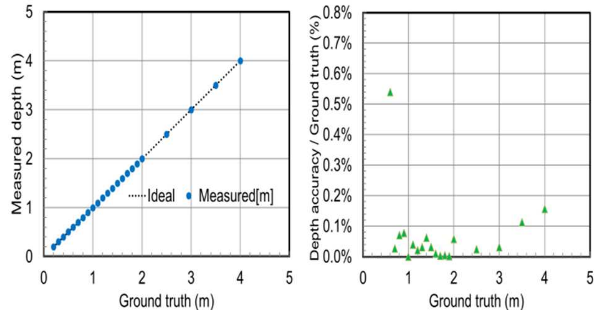

Figure 12. (a) Measured depth versus ground truth and (b) depth accuracy, with 50% reflectivity chart.

Conclusion

To sum up, the ToF CMOS image sensor with 4-tap and 7 µm global shutter pixel has been developed. 4-tap operations are beneficial for motion blur, because they have 4-phase information in one frame compared to the 2-tap operations as shown in Fig. 13 [5]. The 2-tap pixel need two consecutive frames to generate one depth image which causes delays in time and makes motion blur. In order to improve depth performance of 7 µm-ToF pixels, we reduced read-noise with true CDS readout scheme. The doping structures have been optimized to improve DC and PLS performances at a thick silicon. We achieved QE of 57.4 % at 850 nm and 37 % at 940 nm with IR sensitivity enhancement structures of BST, ARL modifications and silicon thickness increment. Overall, depth noise for 90 % reflectivity chart is measured as < 0.3 % without denoise-filtering. The performance of the designed ToF sensor is summarized in Table 1. This work has the largest responsivity and high DC performance with relatively low power consumption. VGA depth map and point cloud images for designed pixel are given in Fig. 14.

Furthermore, for higher resolution and small pixel size of ToF, increasing IR sensitivity and low read-noise with high DC have to be investigated consistently.

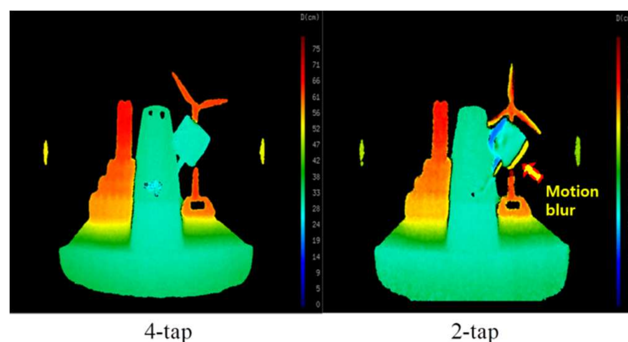

Figure 13. Motion artifact comparison: 4-tap operations are beneficial for motion blur.

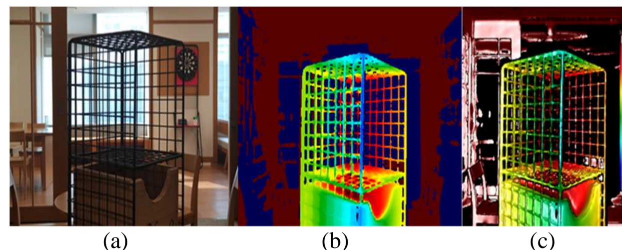

Figure 14. VGA (640x480) (a) RGB, (b) depth map and (c) point cloud images.

Table 1. Performance summary and comparison.

	This work	VLSI'17 [4]	JSSC'15 [6]	ISSCC'18 [7]
Process	65 nm BSI	90 nm BSI	130 nm FSI	65 nm BSI
Pixel pitch	7 µm	10 µm	10 µm	3.5 µm
Number of tap	4	2	2	2
Pixel array	640x480	320x240	512x424	1024x1024
Modulation frequency	10 to 150 MHz	-	10 to 130 MHz	10 to 320 MHz
Responsivity	0.39 A/W @ 850 nm, 0.28 A/W @ 940 nm	0.343 A/W @ 850 nm	0.144 A/W @ 860 nm	0.305 A/W @ 860 nm
Read-noise	3.6 e-	87 e-	(320 µV)	3 e-
Chip power	197 mW	-	2.1 W	650 mW
Depth noise	< 0.3 % @ 0.4-4.0m	0.59% @ 1 m	< 0.5 %@ 0.8-4.2 m	< 0.2% @ 0.4-4.2 m

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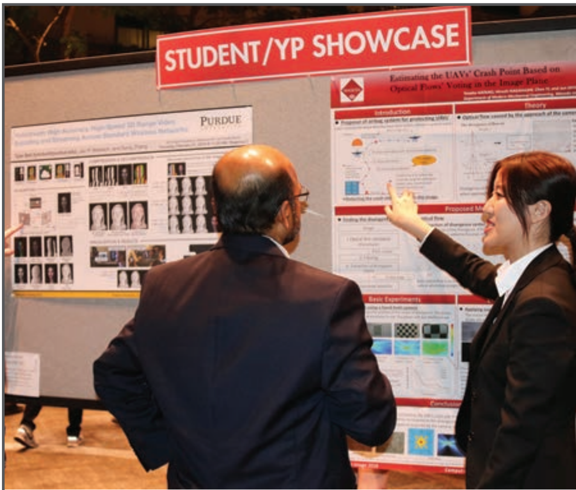

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