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Noise Suppression Effect of Folding-Integration Applied to a column-parallel 3-stage pipeline ADC in a 2.1 μm 33-megapixel CMOS Image sensor

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Abstract

This study investigated the noise suppression effect of multiple sampling applied to a 3-stage pipeline analog-to-digital converter (ADC) in a 33-megapixel, 120-fps 1.25-in CMOS image sensor. The 3-stage pipeline ADC is composed of folding-integration (FI), cyclic, and successive approximation register ADCs, and the multiple sampling for noise suppression is implemented in the FI ADC. The sampling number M is limited by the conversion interval of the FI ADC and the maximum sampling number is M=6 at the 120-fps operation. To investigate the noise suppression effect of 120-fps operation, we measured the random noise of the pixel readout circuit to the sampling number M and compared with theoretical calculations. As a result, we confirmed that the measurement result corresponds reasonably well with the calculated result and the sampling number M = 6 is effective for noise suppression. Furthermore, the calculations revealed that the influence of 1/f noise of the source follower is dominant on the noise performance.

Introduction

The ultra-high-definition television (UHDTV) is a next generation broadcasting system that provides viewers with an extremely high sense of presence and reality. The image parameters for UHDTVs are standardized in Recommendation ITU-R BT.2020 and ITU-R BT.2100 [1, 2], which specify a high pixel count of 33-megapixel, high frame frequency of up to 120-fps, wide color gamut, and high dynamic range (HDR).

We are presently developing a practical 8K camera that satisfies the superior parameters listed, specifically, a resolution of 7,680 (H) × 4,320 (V) pixels, 120-fps, 12-bit, wide color gamut and HDR. From the perspective of usability, the size of the image sensor is a key factor since it dominantly affects the camera size and weight, the variety of lens, and the depth of field. Our first generation 8K 120-fps camera involves a 1.7-in optical format and uses three 33-megapixel CMOS image sensors with a pixel pitch of 3.2 μm [3, 4]. As a next generation device, we are developing an image sensor with a pixel pitch of 2.1 μm for constructing an 8K camera with a 1.25-in optical format.

The signal-to-noise ratio (S/N) of an image sensor tends to deteriorate as the pixel size is reduced, owing to the reduction in the number of photons in a pixel. Therefore, we installed a 3-stage pipelined analog-to-digital converter (ADC) having a folding-integration (FI) ADC [5] as the first stage to alleviate the S/N degradation. The FI ADC utilizes multiple sampling method, and the developed image sensor achieved a random noise of 3.2 e^- by 6 times multiple sampling [6].

However, the sampling number, which is 6, was determined by operation speed restrictions, and we have not clarified yet how multiple sampling affects the noise characteristic. In this study, we examined the random noise characteristics corresponding to the sampling number and compared the measurement results with theoretical calculations to clarify the contribution of the multiple sampling method to an 8K image sensor,

Pixel readout architecture of the image sensor

Figure 1 shows the block diagram of the 8K image sensor [6] employed in the experiment, and Table 1 lists the specifications of this image sensor. The sensor includes a 7,680 (H) ×4,320 (V) pixel array and column parallel ADCs. Further, it includes 480-fps, 240-fps, and 120-fps operation modes and has been already installed in our 8K high-speed camera [7]. The multiple sampling method is not activated in the 240-fps and 480-fps operation mode. Therefore, only the 120-fps mode is considered in this paper.

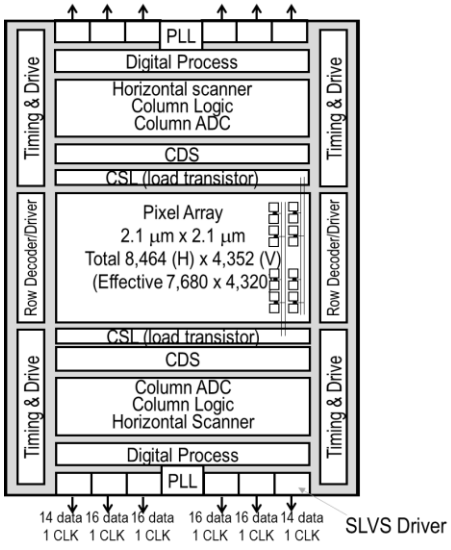

Figure 1. Block diagram of the image sensor [6]

The following section details the pixel readout and A/D conversion architecture of the image sensor. The setup for the measurement is described in the subsequent section.

Figure 2 shows a simplified diagram of the pixel readout circuit. For the detailed structure, readers can refer to our previous paper [6].

Each pixel uses an FSI 4-transistor structure. In the photodiode, the incident light generates signal electrons. These electrons accumulate and are converted to voltage in the floating diffusion amplifier (FDA). This voltage is read out by using an NMOS source follower, and the output voltage of the source follower is input to the CDS circuit, which executes level adjustment and amplification of the input signal. The gain value of the CDS circuit can be modified by changing the ratio of the two capacitors. In the 120-fps operation, the gain value is set to 2x.

Table 1: Specifications of the image sensor

Process	110 nm 1P4M CIS (FSI)
Chip size	22.3 mm (H) x 30.9 mm (V)
Pixel size	2.1 μm x 2.1 μm
Active Pixel count	7,680 x 4,320
Frame Freq.	120 Hz RS
ADC bit depth	14 bit
FWC	7,600 e^- (linear max)
Power	12.5 W

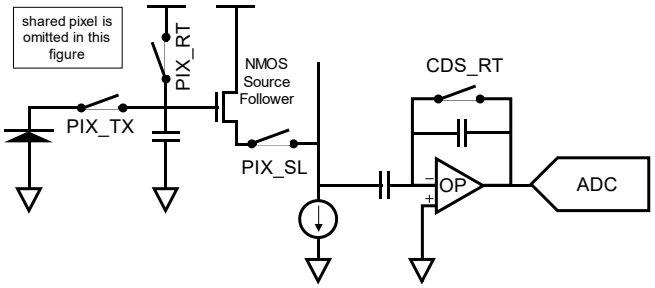

Figure 2. Simplified diagram between pixel and ADC

The operation timings for pixel and CDS circuit are shown in Figure 3. This diagram is also simplified for explanation. Since 4,500 pixels in a column are read out sequentially in a period of 1/120 s, 1.85 μs is the time available to readout one pixel. To execute digital CDS processing, two A/D conversions are operated for one pixel. Therefore, one multiple sampling A/D conversion can use 0.93 μs. Intervals of 0.93 μs exist between reset level and signal level conversions. In this interval, the ADC is processing another pixel. The converted digital value of the reset level is subtracted from that of the signal level to remove the pixel reset noise and offset (digital CDS).

Figure 4 describes the architecture of the 3-stage pipelined ADC. The ADC consist of three sub-ADCs. For the first, second, and third stages, we use an FI ADC, a cyclic ADC, and a successive approximation register (SAR) ADC, respectively. In normal operation with six samplings, the FI ADC outputs a 3-bit (0 to 6) digital code and residual voltage (V_{res1}). The cyclic ADC samples V_{res1} and converts them into a 6-bit digital code. The cyclic ADC also outputs residue voltage (V_{res2}). Finally, the SAR ADC samples V_{res2} and converts it to a 6-bit digital code. The digital codes output from these three sub-ADCs are sent to the logic circuit, and they are combined to form a 14-bit code. Figure 5 shows the timing diagram of the pipeline operation of the three sub-ADCs.

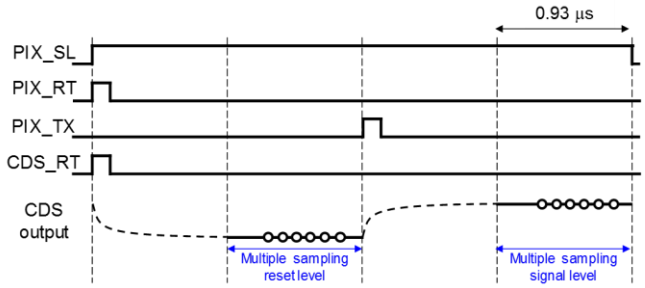

Figure 3. Pixel operation timing and behavior of output voltage of CDS

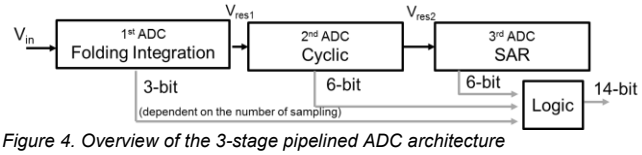

Figure 4. Overview of the 3-stage pipelined ADC architecture

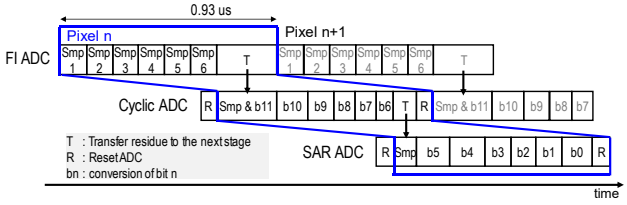

Figure 5. Timing diagram of ADC pipeline operation with M=6

The basic architecture of the FI ADC is shown in Figure 6. The FI ADC consists of a switched capacitor integrator and a 1-bit feedback path. Therefore, its basic structure resembles that of an incremental delta-sigma modulator.

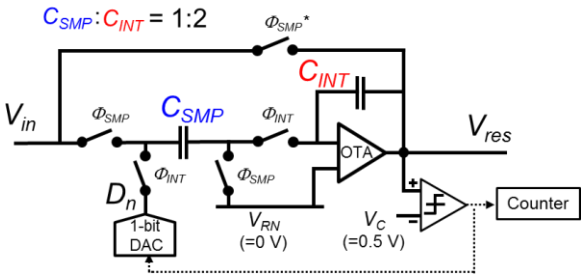

Figure 6. Simplified diagram of FI ADC (simplified for explanation)

The behavior of the residual voltage of an FI ADC (V_{res1}) can be described as follows. In the discussion, we assume that the input range of the ADC is from 0 to 1 V, and the initial V_{res1} value is 0 V. A combination of the $\emptyset_{SMP}$ phase and the successive $\emptyset_{INT}$ phase is corresponds to one sampling, and $\emptyset_{SMP}^*$ works only at the first sampling.

At the first sampling, both the sampling capacitor (C_{SMP}) and the integrating capacitor (C_{INT}) are charged by the input voltage. The capacitance ratio of C_{SMP} to the C_{INT} is 1:2. Therefore, the amount of charge at this phase is equivalent to the amount charged by three sampling capacitors. The residual voltage is expressed as

$$V_{res1}^{1} = \frac{3}{2}V_{in} - \frac{1}{2}D^{1} \quad (1)$$

where $D^1 = 1$ when $V_{in} > 0.5$, otherwise $D^1 = 0$

From the second sampling, the input voltage is sampled by the C_{SMP} and integrated in the C_{INT}. For the n-th sampling, the residual voltage is expressed as

$$V_{res1}^{n} = V_{res1}^{n-1} + \frac{1}{2}V_{in} - \frac{1}{2}D^{n} \quad (2)$$

where $D^n = 1$ when $V_{res1}^{n} > 0.5$, otherwise $D^n = 0$

Consequently, after M samplings, the residual voltage can be described as

$$V_{res1}^{M} = \frac{3}{2}V_{in} + \sum_{n=2}^{M}\frac{1}{2}V_{in} - \sum_{n=1}^{M}D^{n} = \frac{(M+2)}{2}V_{in} - \frac{1}{2}DOUT \quad (3)$$

where $DOUT = \sum_{n=1}^{M} D^{n}$

As shown in this equation, the input voltage V_{in} is amplified by a gain of $\frac{(M+2)}{2}\times$, while V_{res1} is fit into the voltage range from 0 to 1 V by subtracting the $DOUT$, which ranges from 0 to M after M samplings. The residual voltage is converted to digital code via the second and third stage ADCs. The converted digital value of the reset level is subtracted from the converted digital value of the signal level in the digital CDS circuit. This column ADC using multiple samplings and the digital CDS has almost the same noise reduction effect as correlated multiple sampling (CMS) does [9].

Figure 7 shows the relationship between the input voltage and output residue voltage for the case of M = 6. The input voltage is amplified by a gain of 4× (noted as "slope" in the figure) and folded by $DOUT$, which ranges from 0 to 6.

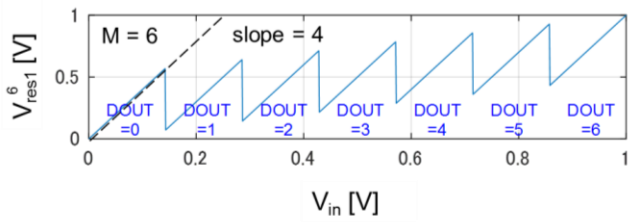

Figure 7. Relationship between V_{in} and V_{res1} for the case of M = 6.

Experimental

Measurement method:

To clarify the noise suppression effect of the multiple sampling utilized by the FI ADC, we measured the dark random noise of the image sensor to the sampling number. The image sensor was operated at room temperature, and all 33-megapixels are read out with 120-fps shooting operation. The extracted 100 × 100 pixels are used to analyze the random noise; the root mean square noise values are calculated for each pixel; and the median value of the pixels is treated as random noise.

A block diagram of the pixel readout circuit is shown in Figure 8. An image sensor is placed in a dark environment, and signal electrons generated in a photodiode are converted to a voltage in the pixel. The voltage is transmitted to the CDS using a source follower amplifier. The conversion gain of the pixel is 85.4 μV/e⁻, which includes the gain of the source follower amplifier. Typically, the gain of the source follower amplifier ranges between 0.8× to 0.9×. The gain value of the CDS is set to 2×. Owing to their limited bandwidth, the source follower and the CDS also work as low pass filters (LPF) and higher frequency noises are eliminated. The cut-off frequency of the CDS is designed to be approximately on the order of tens of megahertz.

The sampling timing used for the measurement is shown in Figure 9. Although the total time for A/D conversion is 0.93 μs, the available time span for multiple sampling is 0.67 μs, because 0.26 μs is required for sampling the residue voltage to the next cyclic ADC. As shown in Figure 9, we divide 0.67 μs equally by the sampling number. Therefore, the sampling frequency becomes higher as the sampling number increases. Further, there are intervals between the reset level conversion and the signal level conversion.

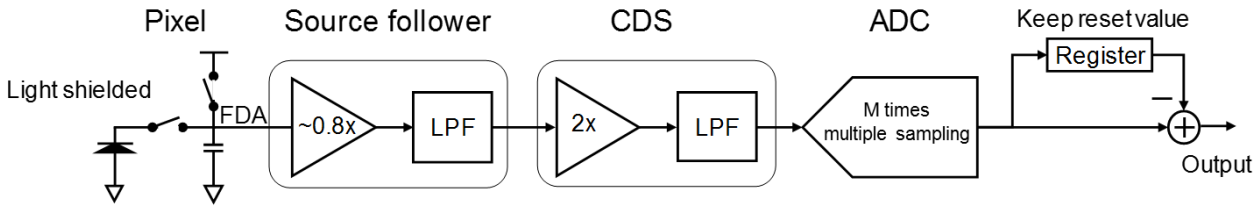

Figure 8. Block diagram of experimental setting.

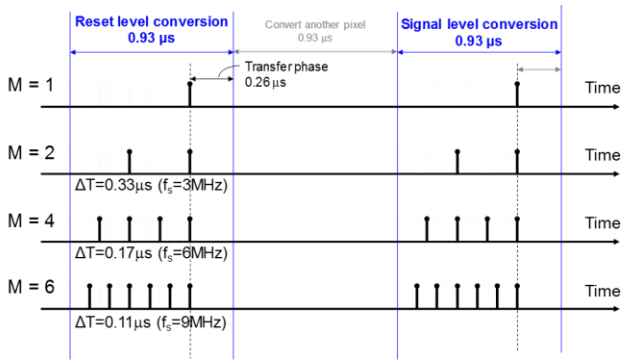

Figure 9. Sampling timing in examined sampling number

A lower sampling frequency can effectively limit the bandwidth of noise and a shorter interval can achieve higher correlation between noise values in the reset and signal levels; therefore, in general, a lower multiple sampling frequency and shorter interval time between the reset and signal conversions are optimal to reduce noise [8]. Consequently, the sampling diagram is not the ideal one; however, it can be expected that the multiple sampling method has a considerable effect on random noise because the sampling frequency is much slower than the cut-off frequency of the LPF characteristics of the source follower and the CDS.

Comparison with theoretical calculations:

The measured dark random noise power $P_{n,total}$ is divided into three components generated by the source follower ($P_{n,SF}$), CDS ($P_{n,CDS}$), and ADC ($P_{n,ADC}$); they are expressed by

$$P_{n,total} = P_{n,SF} + P_{n,CDS} + P_{n,ADC} \tag{4}$$

The noise components generated by the source follower $P_{n,SF}$ can be calculated by

$$P_{n,SF} = \int_0^\infty S_{n,SF}(f) \frac{1}{1+\left(\frac{f}{f_c}\right)^2} \left|H_{CMS}\left(e^{j\omega T_0}\right)\right|^2 df \tag{5}$$

where $S_{n,SF}(f)$ is the noise power spectrum of the source follower, $H_{CMS}(\omega)$ is the transfer function of the CMS, and f_c is the cut-off frequency of the readout circuit. The noise power spectrum $S_{n,SF}(f)$ measured at the source follower output, including the thermal and $1/f$ noise sources, is expressed as [9]

$$S_{n,SF}(f) = \frac{4k_B T \xi_{SF}}{g_{mSF}} + \frac{N_{fSF}}{f} \varsigma_{SF} \tag{6}$$

where k_B is the Boltzmann constant, T is the absolute temperature, f is the frequency. ξ_{SF}, ς_{SF}, and g_{mSF} are the excess thermal noise factor of the source follower, the flicker noise factor to include the influence of the current-source load, and the trance conductance of the transistor used for the source follower, respectively. The transfer function of the CMS can be determined using the timing of the multiple sampling [8, 9]. Figure 10 shows the timing diagram of the multiple sampling for the sampling number M. N_s is the sampling period of the multiple sampling, and N_g is the interval of the reset and signal multiple sampling. N_s and N_g are integers normalized by clock period T_0. Note that the values sampled at the first sampling is three times the amount of the others, because the charge of the first sampling is equivalent to the charge of the three sampling capacitors as described before. The transfer function of the CMS is obtained with the z -transform, and it is expressed in the z domain as

$$H_{CMS}(z) = \left(1 - z^{-(MN_s+N_g)}\right)\left\{\frac{(1-z^{-N_s M})}{1-z^{-N_s}} + 2z^{-(M-1)N_s}\right\} \tag{7}$$

From equation (7) with $z = e^{j\omega T_0}$, the noise power transfer function for the CMS is given by

$$\left|H_{CMS}\left(e^{j\omega T_0}\right)\right|^2 = 4\sin^2\left\{\frac{\omega\left(MN_s + N_g\right)T_0}{2}\right\} \cdot$$

$$\left\{\frac{\sin^2(\omega M N_s T_0/2)}{\sin^2(\omega N_s T_0/2)} + 4\frac{\sin(\omega M N_s T_0/2)\cos\{\omega(M-1)N_s T_0/2\}}{\sin(\omega N_s T_0/2)} + 4\right\} \tag{8}$$

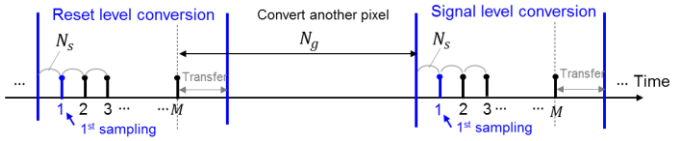

Figure 10. Timing diagram of the multiple sampling for the sampling number M

The noise component generated by ADC ($P_{n,ADC}$) is difficult to calculate owing to the complicated architecture of the ADC and the noise generation due to the high-speed digital signal readout [10]. Therefore, we set a constant voltage input to the ADC to measure the random noise to the sampling number; we regard this measured noise as the ADC noise component. Further, we assumed the noise component generated by the CDS to be much smaller than $P_{n,total}$ and $P_{n,ADC}$. From equation (4), the value expected by subtracting the measured ADC noise from the measured dark random noise ($P_{n,total} - P_{n,ADC}$) should be equal to the calculated source follower noise ($P_{n,SF}$). We compared these values to verify the noise suppression effect of multiple sampling.

Results and discussion

Figure 11 shows the measured input-referred noise to the sampling number M. The measured total noise decreased with an increasing sampling number until it is finally down to 3.2 e^- at M = 6. The same trend can be observed for the measured ADC noise. The value plotted in blue square is obtained by subtracting the measured ADC noise from the measured total noise, which is used for comparison with the calculated source follower noise.

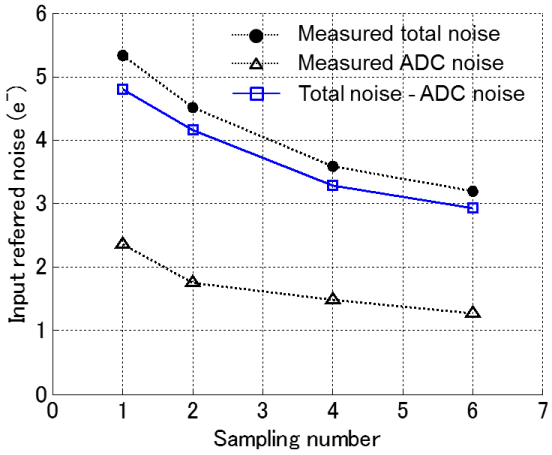

Figure 11. Measured input-referred noise to the sampling number M

Figure 12 shows the comparison of the measurement results with the theoretical calculations. The value plotted in the blue square (Total noise – ADC noise) is the same value plotted in Figure 11. The value plotted in the red circle is the calculated source follower noise. The calculation corresponds reasonably well with the measured result, which indicates that the multiple sampling of FI ADC effectively reduce the source follower noise. Furthermore, the sampling number $M = 6$ is effective for noise suppression, because the calculation indicates that when the sampling number is greater than 6, it leads to a saturated noise suppression effect.

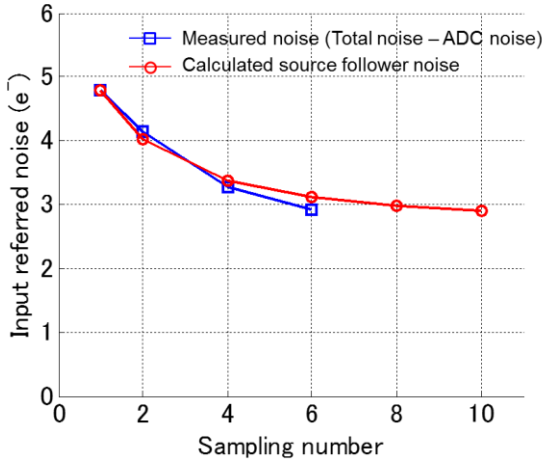

Figure 12. Measured input-referred noise to the sampling number M

Figure 13 shows the noise components of the calculated source follower noise. As shown in equation (6), we assume that the noise of the source follower consists of the thermal noise and the $1/f$ noise. The $1/f$ noise exhibits a dominant effect on the calculated source follower noise, which results in the saturated noise reduction effects when $M > 8$.

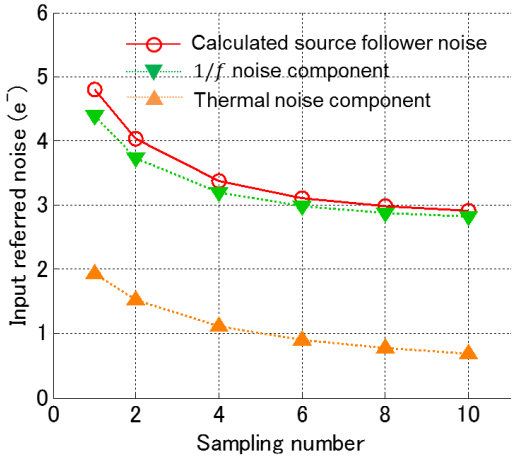

Figure 13. Noise component of the calculated source follower noise

Conclusion

In this paper, we examined the noise suppression effect of the FI ADC applied to a 2.1 µm 33-megapixel 120-fps CMOS image sensor with a column-parallel three-stage pipeline ADC. The measured input-referred noise to the sampling number clearly demonstrated the noise suppression effect of multiple sampling. The comparison with the theoretical calculation showed good correspondence between the measured and calculated results, which indicates that $M = 6$ is effective for noise suppression. Furthermore, the calculations revealed that the influence of the $1/f$ noise of the source follower is dominant on the input-referred noise. We confirmed the effectiveness of the three-stage pipelined ADC with FI for noise suppression in an 8K image sensor.

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Author Biography

Kohei Tomioka received his BE and ME degrees in engineering science from the Kyoto University, Kyoto, Japan, in 2011 and 2013, respectively. In 2013, he joined NHK. He worked as a broadcasting engineer from 2013 to 2016. Since 2016, he has been with NHK Science & Technology Research Laboratories, where he has been engaged in research and development of image sensors and cameras for the 8K Super Hi-vision. He is a member of the Institute of Image Information and Television Engineers of Japan (ITE).

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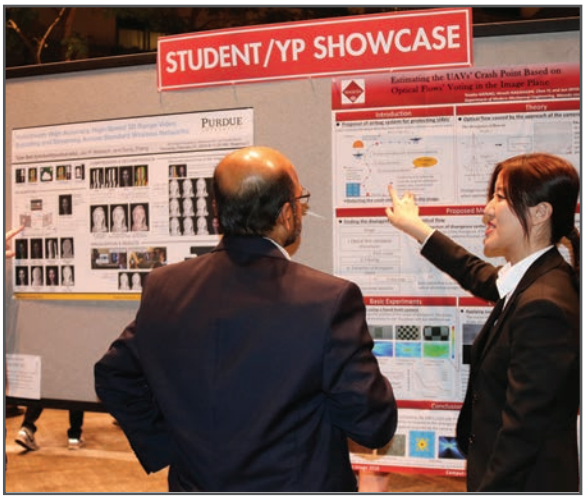

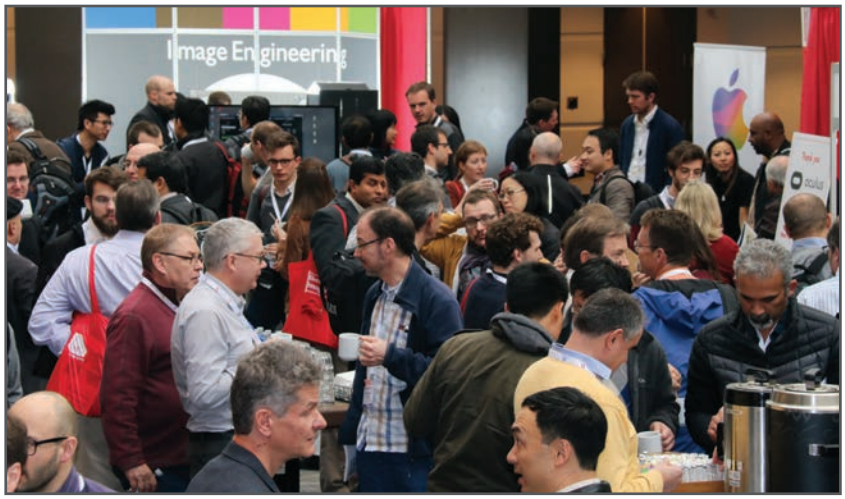

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