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Two calibration methods to improve the linearity of a CMOS image sensor

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Abstract

This paper presents two on-chip calibration methods for improving the linearity of a CMOS image sensor (CIS). A prototype 128 × 128 pixel sensor with a size of 10 μm×12 μm is fabricated using a 0.18 μm 1P4M CIS process. Both calibration methods show obvious improvement on the linearity of the CIS. Compared with the voltage mode (VM) calibration, the pixel mode (PM) calibration method achieves better linearity results by improving the nonlinearity of the CIS 26×. This results in a minimum nonlinearity of 0.026%, which is a 2× better than the state-of-the-art.

I. Introduction

A linear digital output response towards the input luminance intensity is mandatory for an image sensor in many applications where the image performances rely on the absolutely signal values, such as machine vision and quantitative imaging [1].

Different approaches are developed to linearize the radiance response of a CIS. Off-chip processing usually uses polynomials or a look-up table (LUT) to improve the imaging systems' linearity [2].

To improve the circuit efficiency and reduce the following calculation tasks on soft-level, many linearity optimization efforts have also been spent on chip-level, either from the pixel or the circuit standpoint [3]-[4]. Most of the inherent pixel's nonlinearity is caused by the nonlinear gain of the source follower (SF) and by the voltage dependency of the integration capacitor on the floating diffusion region(C_{FD}) [5]. A novel pixel design is proposed in [3], which uses a single stage operational amplifier (OPA) instead of the conventional source follower, to drive the load circuits. This type of pixel structure can avoid the introduction of the SF's nonlinearity. In [4], a type of capacitive transimpedance amplifier (CTIA) pixel is adopted to realize a highly linear CIS by conveying the electrons into a constant Metal-Insulator-Metal (MIM) capacitor, instead of the nonlinear integration capacitor C_{FD}. Compared with C_{FD}, the MIM capacitor has a small voltage coefficient. This structure can further reduce the nonlinearity caused by the nonlinear integration capacitor. Both designs achieve better linearity performance at the expense of noise performance and fill factor.

In [3], we also developed an on-chip digital calibration method to improve the linearity of the CIS from the system level. By calibrating the ramp signal of the ADC, the pixels can achieve a nonlinearity less than 0.06% after calibration. However, the calibrated ramp signal of the image sensor should be captured in a constant illumination condition, which is not always easy to realize.

In this paper, based on the previously proposed calibration method, we increase the resolution of the ADC and propose another type of calibration method to improve the linearity of a prototyped CMOS image sensor. This new calibration method has the advantage of being independent of any illumination to capture the calibrated ramp signal. An image sensor array consisting of 128 × 128 pixels is fabricated in a 0.18μm 1P4M CIS process. Experimental results show a 96% improvement on the linearity of the proposed standard 4T pixel in the pixel mode and 33% improvement in the voltage mode.

This paper is organized as follows. Section II describes the sensor architecture. In Section III, the principle and the operation of the pixel mode and voltage mode calibration are introduced. Measurement results are discussed in Section IV. Finally, Section V states the conclusion.

II. Sensor architecture

The overall block diagram of the prototype image sensor is shown in Figure 1. The column-parallel architecture is chosen due to its excellent trade-off among readout speed, silicon area and power consumption.

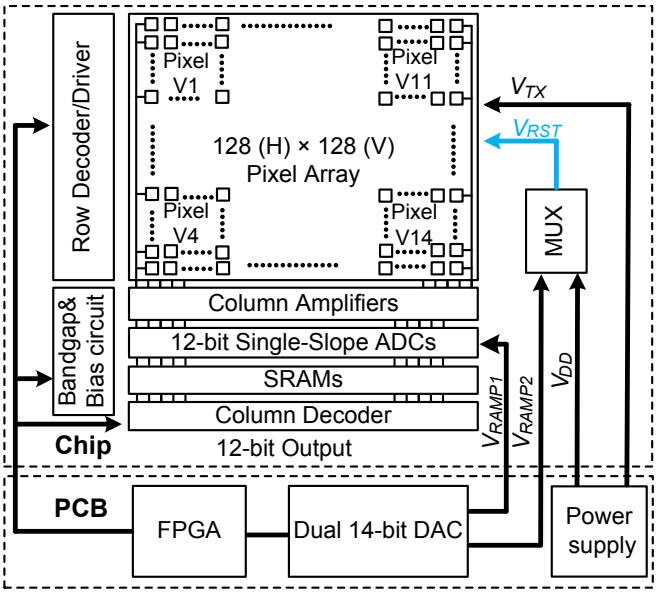

Figure 1. *The proposed CIS system diagram.*

The pixel array consists of 128 × 128 pixels with a size of 10 μm × 12 μm. The array is divided into 16 subgroups with a different pixel design, each subgroup containing 32 × 32 pixels. Each column contains a column amplifier, a 12-bit Single-Slope Analog-to-Digital Converter (SS-ADC), and a SRAM array. The column amplifier provides a programmable gain and realizes correlated double sampling (CDS). The single-slope structure is employed considering its simplicity and the calibration method used. The ADC digitizes the analog signals, and transfers the data into the SRAM. During the next row's A/D conversion, the data in the SRAM is read out through sense amplifiers. Finally, the data will be further processed by an off-chip FPGA. The pixel's reset voltage (V_{RST}) can be either provided by the on-board power supply or by a periodic ramp signal V_{RAMP2}.

Figure 2 shows the schematic of the readout chain. A conventional pMOS transistor featuring a low 1/f noise level, works as the source follower (SF) in the pixel. The value of the C_{IN} is 1pF. By switching the value of the feedback capacitor array from 0.125pF to 1pF, the

column amplifier can provide a programmable gain from 1× to 8× under different light conditions. In the SS-ADC, an off-chip ramp signal is used and compared with the output signal of the column amplifier.

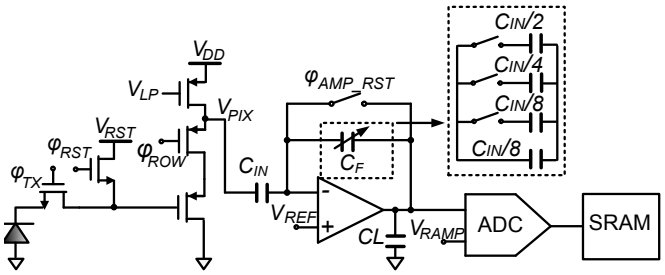

Figure 2. *The schematic of the readout chain.*

The performance of the ramp generator determines the accuracy and linearity of the ADC [6]. For the SS-ADC, the ramp signal can be realized by a high-resolution digital-to-analog converter (DAC) or an integrator. In this paper, combined with the calibration method, a dual 14-bit on-board current steering DAC (CS-DAC) clocked at 100MHz is adopted to create an initial ramp signal V_{RAMP1} for the 12-bit ADC, and the DAC also provides a periodic ramp signal V_{RAMP2} as the pixel's reset voltage in the voltage mode calibration.

As shown in Figure 3, the 14-bit CS-DAC converts the digital signals from the FPGA into two groups of differential current outputs. The load resistors R_{RAMP1} and R_{RAMP2} convey the current outputs to two differential voltage outputs. Then a high bandwidth OPA, combining with R_1~R_4, converts the differential input voltage to the single-ended ramp signal V_{RAMP1}. V_{RAMP2} is generated in the same way.

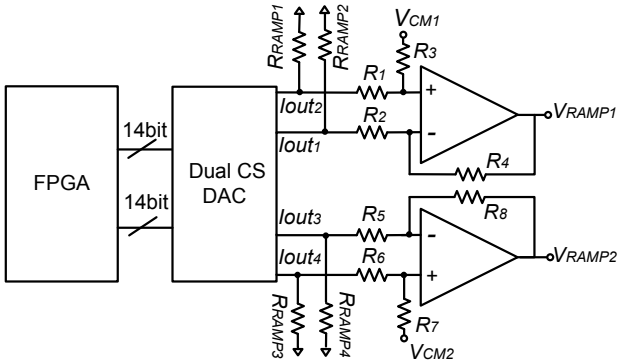

Figure 3. *The schematic of ramp generator.*

III. The calibration algorithm

To improve the linearity of the proposed CIS, two calibration methods are explored. The operating principle of the pixel mode (PM) calibration method is illustrated in Figure 4, in which the pixel is read out conventionally; V_{RST} is a constant DC voltage and the time period between the two adjacent falling edges of φ_{TX} defines the exposure time. The nonlinear transfer function between the number of incoming photons and the final digital output (D_O) of the ADC is stored in the SRAM. The SRAM data is then used to pre-distort the ADC's ramp in such a way that the resulting ADC nonlinearity compensates for the nonlinear behavior of the CIS [3].

During the PM calibration, the number of photons accumulated by the sensor is changed by increasing the exposure time from a unit T_{EXP} to 4096 × T_{EXP} under constant light intensity. M_{IN} is the input digital code of the DAC without calibration, which increases from 0 to 16383(2^{14}-1) evenly. So the DAC generates a linear ramp signal V_{RAMP1}. The digital output of the 12-bit ADC is captured within each exposure time. N_{IN} is the exposure sequence, which increases equally from 0 to 4095. $M_{IN\_C\_PM}$ is the corresponding output sequence after mapping and interpolation. The mapping process removes the offset and the gain errors of the data collected from the SRAMs. The calibrated ramp signal $V_{RAMP1\_C\_PM}$ generated by the DAC, which contains the information of the nonlinearities of the pixel and the readout circuit, is employed to cancel out the latter nonlinearities.

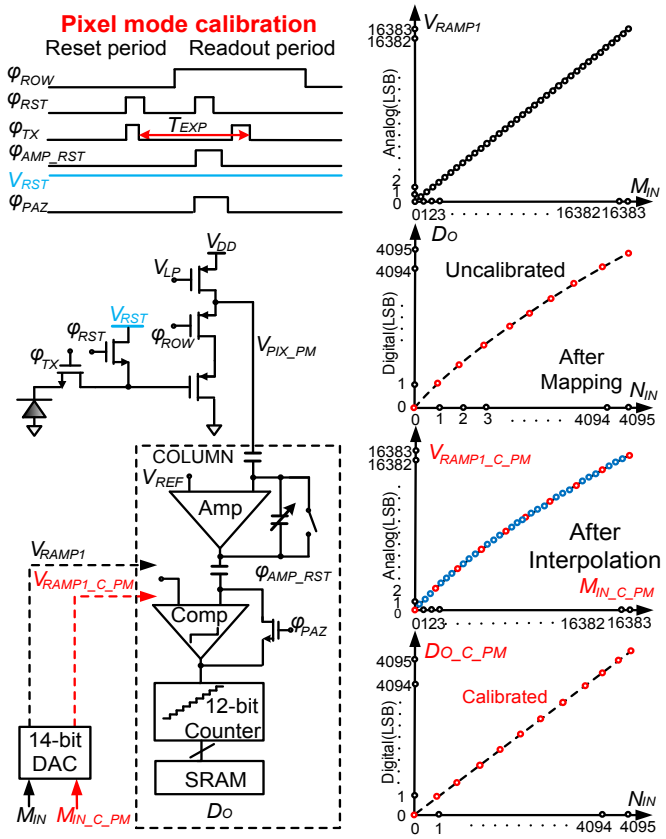

Figure 4. *Pixel mode calibration operation and its timing diagram.*

Figure 5 introduces the voltage mode (VM) calibration method, where the photodiode is disabled by turning off the TX transistor and a decremental periodic ramp signal V_{RAMP2} is added to the drain of the RST transistor. V_{RAMP2} imitates the output signal on the floating diffusion region of the pixel in the pixel mode. It has two values, referring to the two different phases of a conventional pixel. A monotonic increasing output signal is obtained through the following CDS circuit. Digitized by the ADC, the final digital output contains the information of the nonlinearities of the SF and readout circuit.

Similarly, the voltage mode calibration is based on the voltage transfer function between the input ramp signal V_{RAMP2} and the final digital output, starting from the SF. After mapping and interpolation, the incremental sequence $M_{IN\_C\_VM}$ is converted by the DAC into a new ramp signal $V_{RAMP1\_C\_VM}$, with which, the nonlinearities of the SF and readout circuit can be compensated for. Although the VM calibration cannot cancel the nonlinearities caused by the photodiode and the integration capacitor in the pixel, it has the advantage of being independent of any illumination to capture the calibrated ramp signal. Other calibration methods that combine the advantage of the voltage

mode method with the accuracy of the pixel mode method, are under investigation.

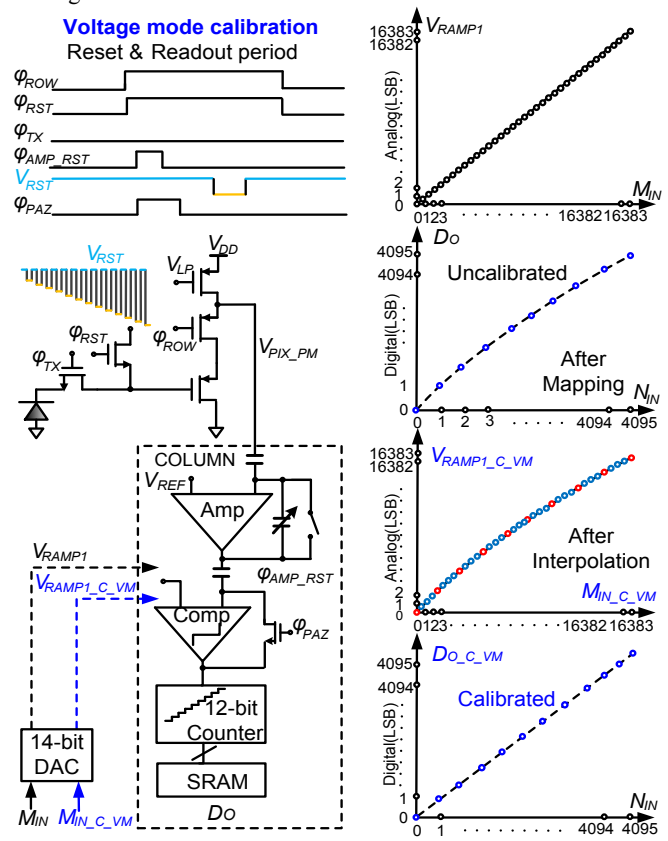

Figure 5. *Voltage mode calibration operation and its timing diagram.*

VI. Measurement results

Figure 6 shows the chip photo and the camera system. The chip in this paper has been fabricated with a commercial 0.18 μm CIS process. The chip size is 5mm × 3mm.The supply voltage is 3.3V. The sensor has an effective resolution of 16384 pixels at 40fps, progressively scanned. An Altera Cyclone II FPGA is used to provide digital control signals.

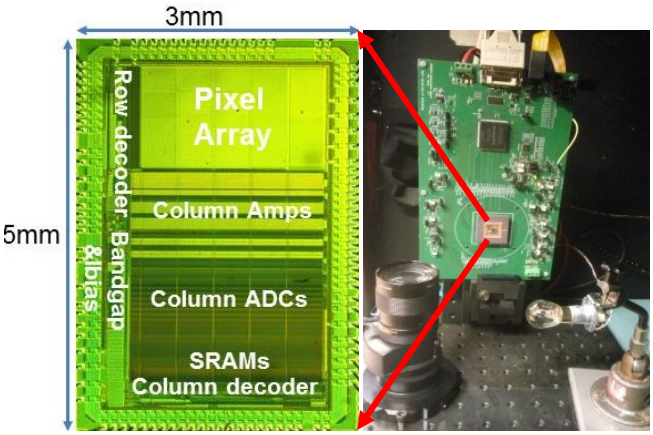

Figure 6. *Chip microphotograph and test camera system.*

The input range of the ADC is 1V. The differential nonlinearity (DNL) and integral nonlinearity (INL) of the ADC can be measured by applying to the input either a voltage ramp generated by a higher resolution DAC or a low-frequency sine wave. In this design, considering the calibration method we use, a voltage ramp generated by the same DAC is used to measure the nonlinearity of the ADC. The nonlinearity measurement results contain the nonlinearity of the ADC as well as that of the DAC. The measured DNL and INL of the ADC in a column are shown in Figure 7. The A/D conversion time is 163.84 µs with 25 MHz clock frequency and consumes only 120 µW per column. From the measured results, the DNL errors are -0.357/+0.368 LSB and the INL errors are -0.88/+1.963 LSB, which corresponds to a nonlinearity of 0.034%.

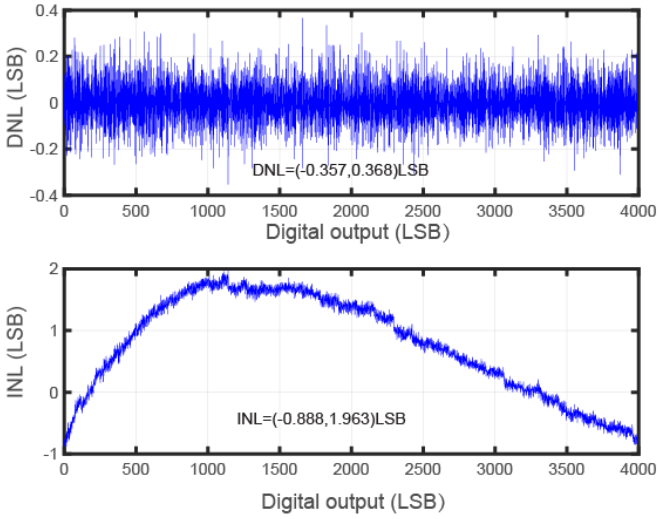

Figure 7. *Measured nonlinearity performance of one channel SS-ADC.*

The nonlinearity performances of all ADCs in the array are plotted in Figure 8. All channels have a nonlinearity less than 0.052%.

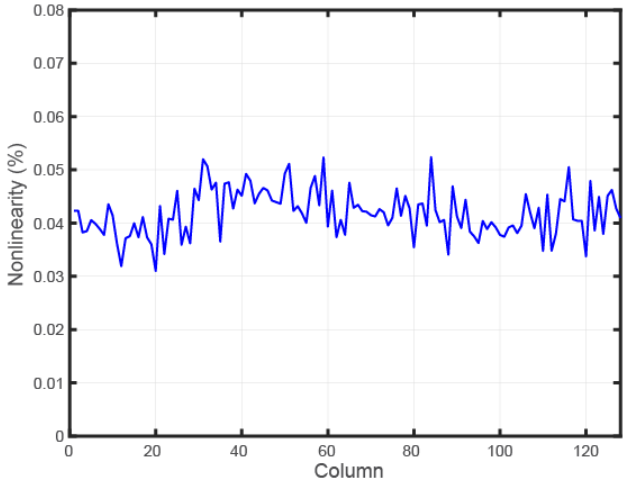

Figure 8. *Measured nonlinearity performance of SS-ADC array.*

Among dozens of pixel designs, one type of pixel V4 featuring low noise design, is selected to demonstrate the effectiveness of the proposed calibration methods. All measurements are carried out with unity gain for the column amplifier. A tungsten lamp provides a stable and constant illumination. The number of photons coming to the sensor is changed by linearly increasing the exposure time. All linearity evaluations are done with a window containing 8×30 pixels averaged over the 100 frames captured. Figure 9. (a) shows the DNL

results of Pixel V4 array. The black line plots the measurement results without calibration while the red and the blue lines represent the results with the PM and VM calibrations, respectively. Figure 9. (b) and (c) show the INL results. With these two calibration methods, the nonlinearity of the pixel V4 is improved from 0.68% to 0.46%, and 0.026% respectively. Compared with VM calibration, we achieve better linearity with the assistance of the PM calibration method since it can fully calibrate the nonlinearity caused by the pixel, especially the nonlinear integration capacitor. These two calibration methods are also valid for the other types of pixels.

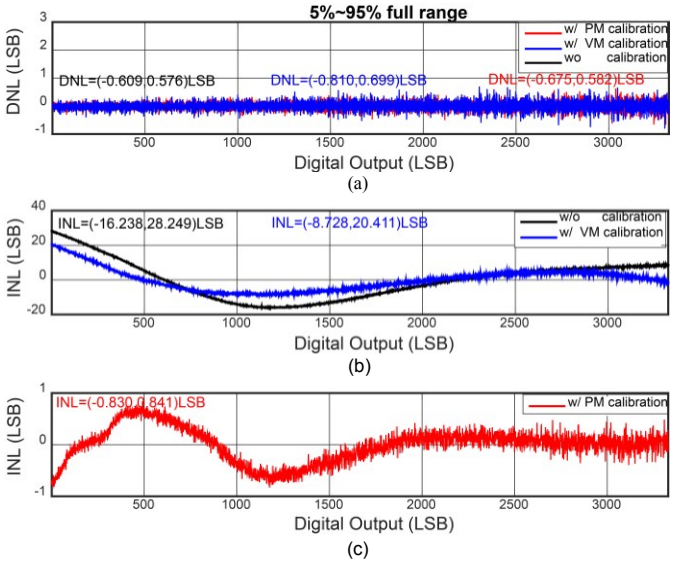

Figure 9. *The nonlinearity of Pixel V4 array (notice the difference in scale on the vertical axis). (a) DNL (b) INL w/o & w/ VM calibration (c) INL w/ PM calibration.*

Figure 10 shows the linearity improvement for each pixel with the proposed calibration methods. We can conclude that the calibration methods are effective for each pixel.

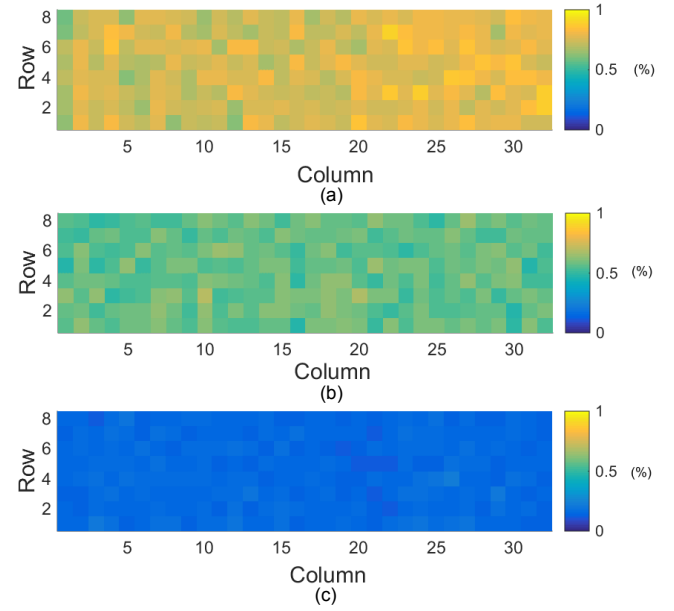

Figure 10. *The nonlinearity of Pixel V4 (for each pixel). (a) w/o calibration (b) w/ VM calibration (c) w/ PM calibration.*

The input referred noise of the pixel V4 as a function of the column amplifier's gain is plotted in Figure 11. With the high gain of the column amplifier, the input referred noise of the pixel V4 is 145 μV at an analog gain of 18 dB.

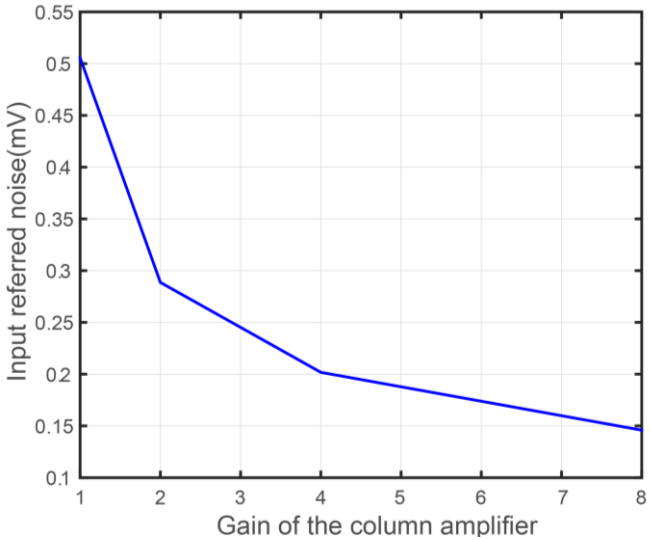

Figure 11. *The noise performance of Pixel V4.*

Figure 12 shows a captured picture of a test chart taken by this design. There are 14 groups of different pixel designs with various conversion gain and noise performances, which makes the photon response non-uniform.

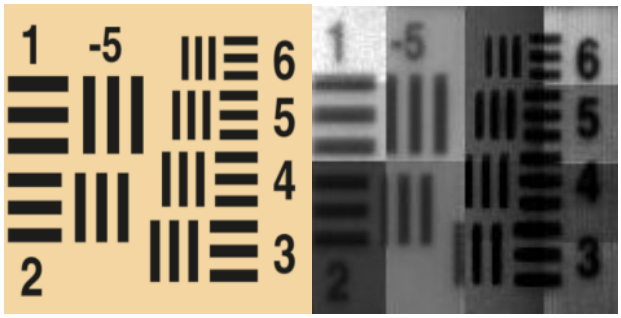

Figure 12. *Original ISO test Chart and the captured picture.*

Table I summarizes the performance of the proposed CIS and compares it with prior art in terms of linearity [3]-[9]. The nonlinearity of this CIS is 2× better than the state-of-the-art.

V. Conclusion

In this paper, we have proposed two different calibration methods to improve the linearity of the CIS implemented in a 0.18μm CIS process. With calibration, the CIS can achieve a nonlinearity less than 0.026%, which is a 2× better than the state-of-the-art.

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TABLE I

PERFORMANCE COMPARISON

		This Work	[3] IISW'17	[4] WIS'17	[7] VLSI'16	[8] ISSCC'15	[9] TED'09
Process	nm	**180**	180	180	90	90/65	350
Array Size		**128 × 128**	128 × 128	160 × 128	4624 × 2296	5246 × 3934	320× 240
Global /Rolling shutter		**RS**	RS	RS	GS	RS	RS
Pixel structure		**4T**	Buffer	CTIA	4.5T	NA	4T
Pitch	μm	**12**	10	12	5.86	1.43	5.6
Fill factor	%	**59.5**	47	36.3	NA	NA	NA
ADC Architecture		**12-bit SS**	10-bit SS	12-bit SS	14-bit SS	12-bit SS	10-bit SS
Frame rate	fps	**40**	60	40	480	30	700
Conversion gain	μV/e-	**40**	56.8	40	30.3	76.6	46
Read Noise	μV	**145**	234	656	140	100	490
Full well capacity	e-	**23100**	17270	30613	30450	9700	18500
Nonlinearity	w/o calibration	**0.68%**	0.26%	0.095%	0.18%	0.16%	0.37%
	w/ VM calibration	**0.46%**	NA				
	w/ PM calibration	**0.026%**	0.058%				

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