https://doi.org/10.2352/ISSN.2470-1173.2018.11.IMSE-398

A Preliminary Chip Evaluation toward Over 50Mfps Burst Global Shutter Stacked CMOS Image Sensor

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Abstract

A preliminary chip evaluation targeting a development of over 50Mfps burst global shutter stacked CMOS image sensor is reported in this work. A two dimensional CMOS image sensor chip with 34.56μm^{H} ×34.56μm^{V} equivalent pitch 25^{H} ×100^{V} pixels with ultra-high speed charge collection capability and in-pixel 80 analog memories was designed and fabricated using a 0.18μm 1-Poly-Si 5-Metal layer CMOS image sensor technology. The operation of the fabricated chip was confirmed to work with two modes: in-pixel correlated double sampling (CDS) mode with 80 frames up to 50 Mfps and direct readout mode with 40 frames up to 71.4 Mfps. Based on the developed architecture, over 50 Mfps with about 400 consecutive frames with 100% fill factor will be achieved using backside illumination 3D stacking technology with high-density analog memory.

Introduction

Ultra-high speed (UHS) imaging over 1 Mfps frame rate is a key technology for visualization of UHS phenomena in scientific, engineering, biomedical fields. We have previously developed UHS global shutter CMOS image sensors with on-chip analog memories for each pixel [1-2]. These sensors have achieved 10 Mfps, 100 kpixels and 128 frames by the full pixel mode and 20 Mfps, 50 kpixels and 256 frames by the checkered-pattern half pixel mode. Demands for higher frame rate, higher light sensitivity and longer record length motivate researchers including us for further development of UHS CMOS image sensors targeting the unreached performance region shown in Figure 1 [1-7].

Technologies that utilize three dimensional (3D) capability of semiconductors such as 3D stacking [8], deep trench isolation [9] and so on, have become strong driving force to improve performance and add more functions to image sensors. A theoretical study of UHS CMOS image sensor utilizing 3D stacking technology revealed that a higher frame rate is to be obtained due to the shorter wire length between pixels to the designated analog memories [10]. We have recently presented a 10 Mfps 960 frames video capturing using a UHS CMOS image sensor with newly developed high-density trench-type analog memory with 30 fF/μm^2 areal capacitance density [7]. A 3D stacked global shutter CMOS image sensor with high-density analog memory is promising architecture to further improve the performance of UHS CMOS image sensors.

In this paper, we conducted a preliminary evaluation of newly fabricated chip toward a development of over 50 Mfps burst global shutter stacked CMOS image sensor. A two dimensional CMOS image sensor chip with 80 in-pixel analog memories mimicking the 3D stacked image sensor structure was designed and fabricated. And the measurement results of the developed sensor chip are presented.

Developed preliminary image sensor chip

The targeted 3D stacked global shutter UHS CMOS image sensor with pixel-width connection is schematically shown in Figure 2 (b). Here, the speed and light sensitivity improvements from our previous work (Figure 2(a)) are to be achieved by three means; shortening delay of pixel driving pulses due to flexible wiring layout and multiple number of metal layers not sacrificing the fill factor, shortening pixel signal readout time to analog memory due to the minimized signal wire distance, and 100% fill factor by back side illumination. In addition, the chip size becomes almost the same as the pixel area in the 3D stacked case. This structure is beneficial to increase the number of pixels for higher resolution. Moreover, in this architecture, it is unnecessary to put relay source follower (SF) buffer between pixel and memory array. This is beneficial to reduce power consumption.

In this work, as preliminary experiment to evaluate the speed improvement, a two dimensional CMOS image sensor chip shown in Figure 2(c) with 34.56μm^{H} × 34.56μm^{V} equivalent pitch 25^{H} × 100^{V} pixels with UHS charge collection capability [11] and in-pixel 80 analog memories per pixel was designed and fabricated.

Figure 3 shows the circuit and pixel layout diagrams of the developed chip. In order to mimic the 3D stacked image sensor chip, 4^{H}×20^{V} analog memory bank is placed closely to the pixel. In this work, a planer poly-Si/SiO$_2$/Si capacitor was employed as analog memory. The number of analog memory will be increased by a factor of four if the developed high-density trench-type analog memory is utilized [7]. ϕSS is an analog memory select pulse, and ϕMC is a memory column select pulse. The pixel has a photodiode (PD), a charge transfer switch (T), a reset switch (R), SF amplifiers (SF1, SF2), SF select switches (X1, X2, X2'), current source

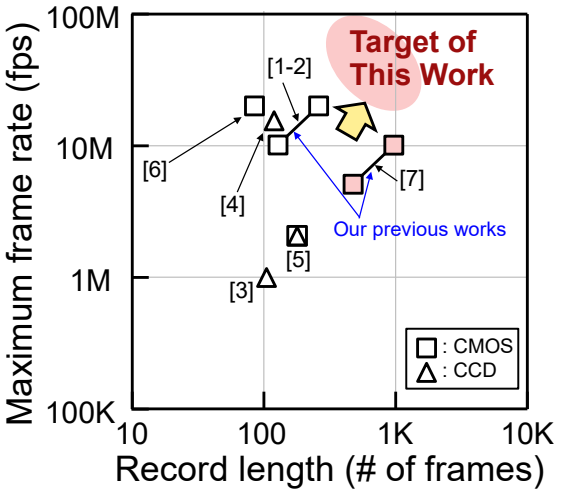


Figure 1. Relationship between maximum frame rate and record length of burst UHS image sensor and target performance region of this work.

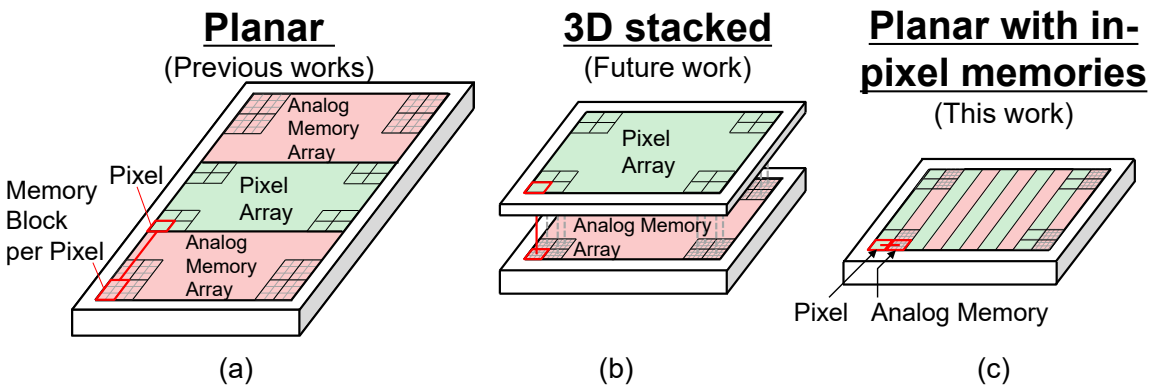


Figure 2. Structures of UHS global shutter CMOS image sensors. (a) planar type achieved by previous works[1-2], (b) 3D stacked type as future work and (c) planer type mimicking the 3D structure for preliminary experiment in this work.

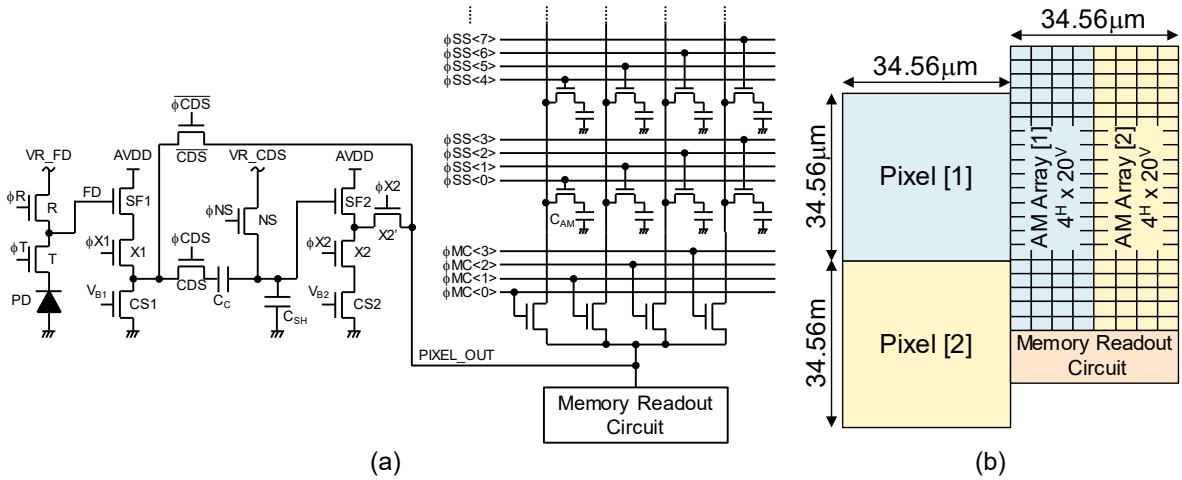


Figure 3. (a) Circuit and (b) pixel layout diagrams of the developed CMOS image sensor in this work.

transistors (CS1, CS2), a noise reduction circuit, and newly added switches (CDS, $\overline{CDS}$) to the circuits of previous works[1-2, 7]. A noise reduction consists of capacitors (C_C, C_{SH}), and noise sampling switch (NS). The photodiode has the same structure and size as the previous works[2, 7, 11]. In order the reduce the RC delay of pixel driving pulses, the width and spacing of pixel pulse wires were by about two times and six times wider than from the previous works [2, 7] respectively. The wiring length of pixel output line was shortened from about 8 mm of the previous works[1,2] to about 40 µm.

Two operation modes were implemented in the developed chip due to the additional switches in the pixel circuit. The first one is the in-pixel correlated double sampling (CDS) mode with consecutive 80 frames up to 50 Mfps. Here, the pixel signal after CDS operation is outputted to the analog memory, like demonstrated in the previous works [1-2]. The second one is the direct readout mode with consecutive 40 frames up to 71.4 Mfps (14nsec period). In this operation mode, in-pixel SF output is bypassed to the analog memory inputs to shorten the frame period by eliminating the in-pixel CDS operation. In this mode, both reset signal and light signal are readout to the analog memory to take CDS off-chip, the record length becomes half the analog memory number per pixel.

Chip measurement results

Figure 4 shows the micrograph of fabricated chip. The chip was fabricated by using a 0.18µm 1-Poly-Si 5-Metal layer CMOS image sensor technology. The die size is 4.8 mm^H × 2.8 mm^V. The chip has two parallel analog outputs.

Figure 5 shows the simulation results of the developed chip for (a) the in-pixel CDS mode and (b) the direct readout mode, respectively. During the in-pixel CDS mode, analog memory is selected simultaneously with the in-pixel CDS operation. In the previous works[1-2, 7], analog memory was selected after in-pixel CDS operation because multiple pixels shared one output line. Compare to the previous works, the operation in this work can reduce the signal readout time. Furthermore, the pulse width and signal readout time are significantly shortened from previous planar types with separated pixel and memory regions because the delay of pixel driving pulse are shortened and the pixel readout time to analog memory is shortened. During the direct readout mode, in-pixel CDS operation is omitted to further improve the speed. Up to 50 Mfps is to be achieved by the in-pixel CDS mode and 71.4 Mfps is to be achieved by the direct readout mode, respectively.

The chip measurement system is shown in Figure 6. The prototype camera consists of FPGA board that generate timing pulse, sensor head board, and analog front end board. The maximum

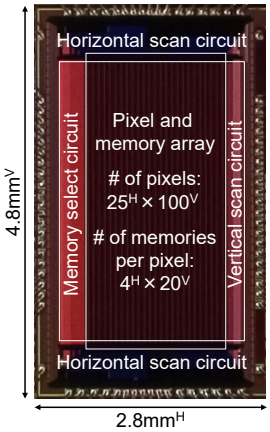
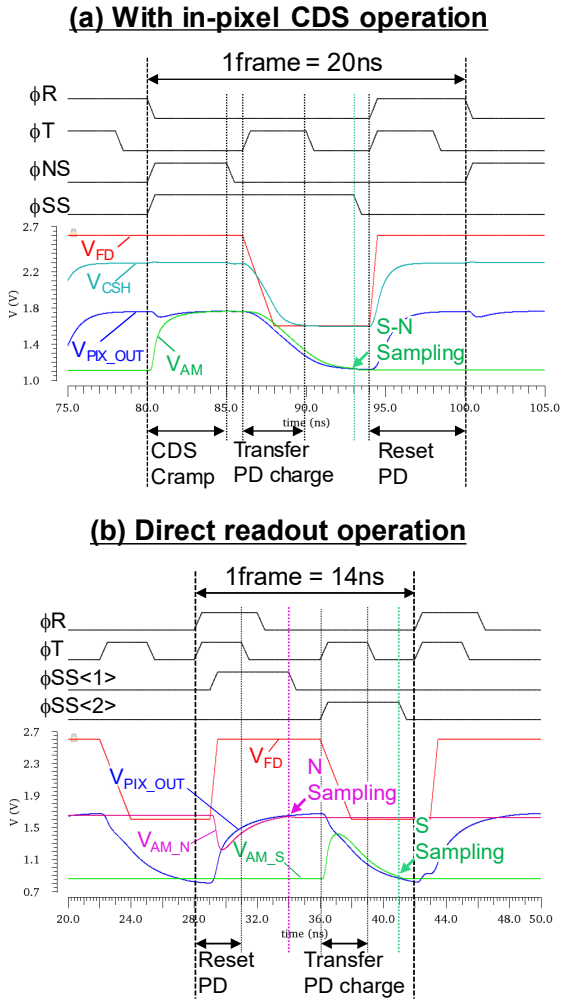


Figure 4. Micrograph of the fabricated chip.



ϕR: Reset pulse, ϕT: Transfer pulse
ϕNS: Noise Sampling pulse ϕSS: Analog memory select pulse

V_{FD}: Voltage of FD, V_{CSH}: Voltage of C_{SH},
V_{PIX_OUT}: Voltage of pixel output, $V_{AM:}$ Voltage of analog memory

Figure 5. Circuit simulation results for (a) the in-pixel CDS operation at 50 MHz and (b) the direct readout operation without in-pixel CDS at 71.4 MHz, respectively.

operation frequency for driving pulse is 1 GHz. The sensor chip has no cooling system at all.

Sample images captured by the in-pixel CDS mode and the direct readout mode are shown in Figure 7, 8 respectively. The captured object was attached to the tip of a motor rotating at 18 krpm in counterclockwise direction. Video capturing at 50 Mfps with 80 frames by the in-pixel CDS mode, and at 71.4 Mfps with 40 frames by the direct readout mode were successfully confirmed respectively. The performance of the developed UHS CMOS image sensor are summarized in Table I.

Conclusion

In this work, Over 50 Mfps video capturing with maximum 80 frames was successfully demonstrated by evaluating a planar-type preliminary UHS burst global shutter CMOS image sensor chip with $25^H \times 100^V$ pixels with 80 analog memories placed close to the pixels, mimicking the 3D stacked structure. The circuit simulation and evaluation results of the preliminary designed chip are promising to the 3D stacked chip with pixel-wise connection that achieves 100% fill factor due to back side illumination, over 50 Mfps frame rate and about 400 frame record length due to the combination with high density analog memory.

References

[1] Y. Tochigi et al., "A Global-Shutter CMOS Image Sensor With Readout Speed of 1-Tpixel/s Burst and 780-Mpixel/s Continuous," IEEE JSSC, Vol.48, pp.329-338, 2013.

[2] R. Kuroda et al., "A 20Mfps Global Shutter CMOS Image Sensor with Improved Light Sensitivity and Power Consumption Performances," ITE Trans. Media Tech. and Applications, Vol.4, pp.149-154, 2016.

[3] T. G. Etoh et al., "A CCD Image Sensor of 1Mframes/s for Continuous Image Capturing of 103 Frames," ISSCC Dig. Tech. Papers, pp.46-47, 2002.

[4] T. G. Etoh et al., "A 16 Mfps 165 kpixel backside-illuminated CCD," ISSCC Dig. Tech. Papers, pp.406-407, 2011.

[5] J. Crooks et al., "Kirana: a solid-state megapixel uCMOS image sensor for ultra-high speed imaging," in Proc. IS&T/SPIE Electronic Imaging, Vol.8659, pp.865903-1-14, 2013.

[6] L. Wu et al., "A 20 Mfps high frame-depth CMOS burst-mode imager with low power in-pixel NMOS-only passive amplifier," in Proc. The 31st International Congress on High-speed Imaging and Photonics, pp.96-101, 2016.

[7] M. Suzuki et al., "10Mfps 960 Frames Video Capturing Using a UHS Global Shutter CMOS Image Sensor with High Density Analog Memories," Proc. Intl. Image Sensor Workshop, pp.308-311, 2015.

[8] S. Sukegawa et al., "A 1/4-inch 8Mpixel back-illuminated stacked CMOS image sensor," ISSCC Dig. Tech. Papers, pp.484-485, 2013.

[9] Y. Kitamura et al., "Suppression of Crosstalk by Using Backside Deep Trench Isolation for 1.12μm Backside Illuminated CMOS Image Sensor," IEDM Tech. Dig., pp.537-560, 2012.

[10] M. Gonthier et al., "High-density 3D interconnects Technology: The key for burst-mode very high speed imaging?," Proc. Intl. Image Sensor Workshop, pp.142-145, 2015.

[11] K. Miyauchi et al., "Pixel Structure with 10 nsec Fully Charge Transfer Time for the 20M Frame Per Second Burst CMOS Image Sensor," in Proc. IS&T/SPIE Electronic Imaging, Vol.9022, pp.902203-1-12, 2014.

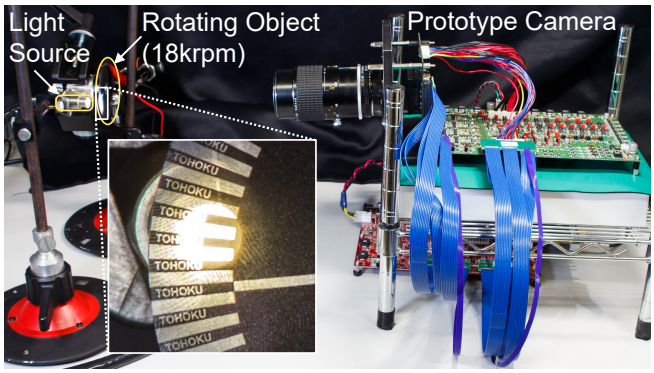


Figure 6. Measurement system of the developed UHS CMOS image sensor chip.

Table I. Summary of the performance of the developed UHS CMOS image sensor chip.

Technology	1P5M 0.18 μm CMOS image sensor	
Pixel pitch (3D stacking equivalent)	69.12 $\mu m^H \times 34.56\ \mu m^V$ ($34.56\ \mu m^H \times 34.56\ \mu m^V$)	
Photodiode size	$30.00\ \mu m^H \times 21.34\ \mu m^V$	
# of pixels	$25^H \times 100^V$	
# of analog memory per pixel	80	
Maximum frame rate	In-pixel CDS mode	Direct readout mode
	50 Mfps	71.4 Mfps
# of consequtive frame	80	40

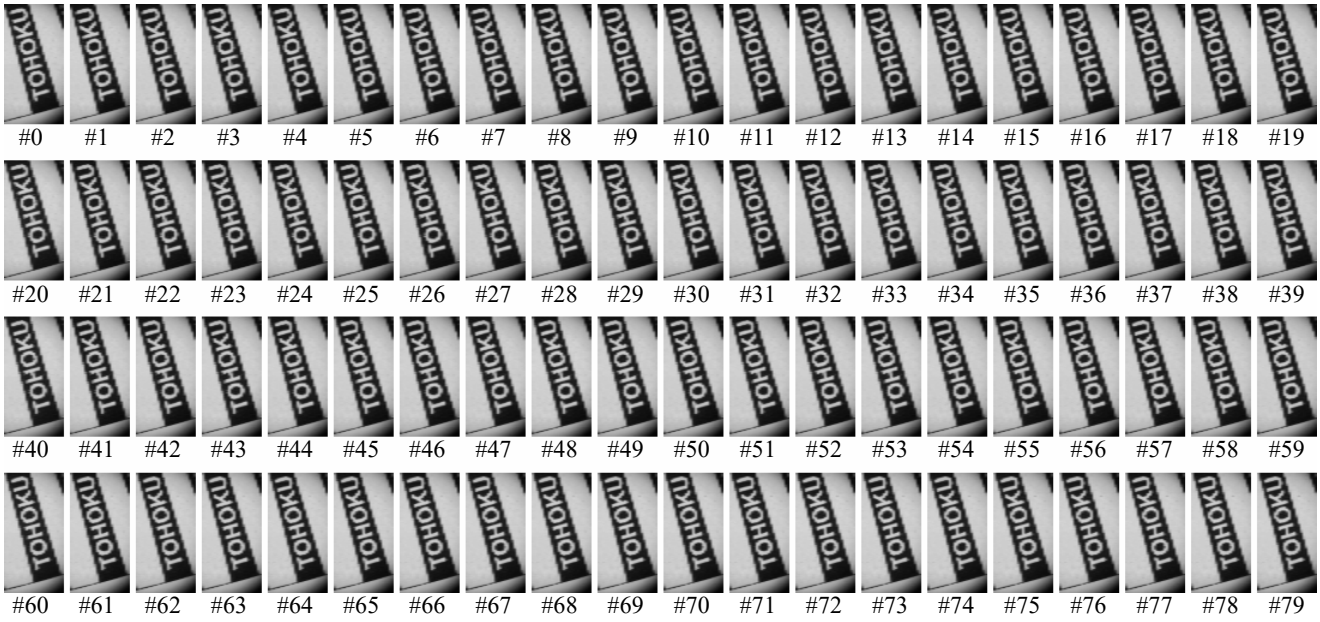


Figure 7. Sample images of the rotating object (18 krpm) captured at 50 Mfps 80 frames by the in-pixel CDS mode.

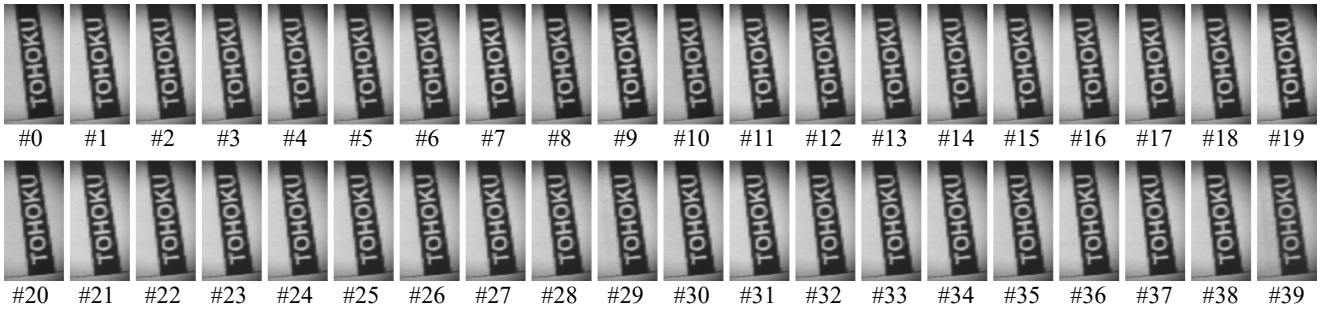


Figure 8. Sample images of the rotating object (18 krpm) captured at 71.4 Mfps 40 frames by the direct readout mode.