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Dark Current Limiting Mechanisms in CMOS Image Sensors

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Abstract

The presence of dark current, signal charge which is not due to photons, has been a performance limiter for image sensors. There has been a 5000x decrease over 40 years and there is the assumption that this trend will continue. However, the decrease has been accompanied by a change of the nature of the generation mechanism as is seen in characterization data related to voltages and temperature. The present limiting root cause of dark current needs to be determined to guide further improvement. It is also interesting to speculate on the ultimate limitation of dark current in defect-free silicon.

Introduction:

Dark current limits performance in image sensors, producing false signal and resulting noise. The understanding of the nature of dark current and resulting technology improvements have had a significant impact on lowering dark current. The technology has successfully eliminated the defects and contamination that has been the cause of dark current, leaving a new performance level whose mechanism is not understood. As other sources of sensitivity-limiting noise drop, it is important that dark current, with its contribution of shot noise, continue to drop. For this to happen, there is a need for CMOS Image Sensors (CIS) to find actionable root cause for the present technology and to understand the eventual limit that can be achieved in defect-free silicon.

What is dark current?

Dark current in an image sensor is the signal that is generated in a typical pixel that is not due to the absorption of a photon. The basic principle for image sensor operation is based around creating a pixel that has a collection area that is isolated and out of equilibrium. Then the photon- generated carriers can collect here, returning this volume back toward equilibrium. Unfortunately carriers created by thermal process or high field effects can do the same, producing dark current. Dark current is physical charge that adds to any photon-generated charge.

Dark current occurs in every pixel, but varies from pixel-to-pixel because of variation in the number of process-related defects and because of the shot noise from the generation process. The result, as seen in an image seen in the dark is varying degrees of "grainy" (Figure 1).

Dark current for a given technology tends to be dominated by a single critical mechanism that overshadows lesser sources. Reducing dark current has been a continual "peeling of the onion", conquering one source only to reveal the next dominant one. The sources need to be of a physical density that probability leads to their being several occurrences per pixel. Dark current differs from "bright defects" which result from sources where probability only produces events in a small fraction of the pixels (Teranishi, 2013). "Bright pixels" can be ignored or corrected while dark current impacts performance in all pixels. This paper will concentrate on dark current only.

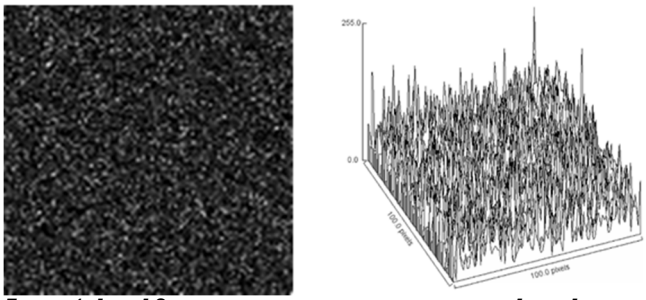


Figure 1: [left] Synthetic dark image appears grainy; [right] dark image is combination of "grainy" and "snow"

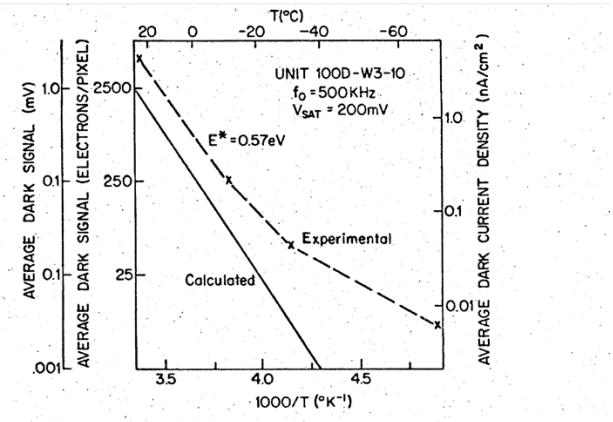
Historic perspective

The reduction in dark current as image sensor technology has progressed has been dramatic. In 1974, published dark current was 2 nA/cm2 at room temperature (Figure 2) (Dyke & Jack, 1974). By 2015, published values had dropped to 0.4 pA/cm2, a 5000x improvement (Kobayashi, 2015).

Along with this reduction, the nature of the temperature dependence also changed, going for a Shockley-Read-Hall-like mechanism with a temperature dependence dominated by traps in the middle of the silicon band-gap (Eg/2) to one consistent with generation across the full silicon band gap (Eg).

The upshot is that technology improvement has been able to reduce the dark current nominally 10x per technology node (Figure 3). After initial efforts driven by scientific imaging, this has been the result of commercial applications pushing for and expecting constant improvement. The expectation is that this will continue, but it the solutions being proposed by foundries (e.g., improved equipment) seem aimed at solving an "Eg/2" problem, not the "Eg" nature that is now dominant.

It is also interesting to understand when dark current stops being driven by defects in silicon, but is dominated by the silicon itself. At this point in technology development, there will be no further improvement due to process and manufacturing and any progress will have to shift to design, working from an understanding of the dark current mechanisms in silicon itself.



EXPERIMENTAL AND CALCULATED CURVES OF DARK CURRENT VS. TEMPERATURE. THE EXPERIMENTAL DATA WAS TAKEN WITH A UNIT EXHIBITING AN AVERAGE DARK CURRENT OF 2 nA/cm^2 AT ROOM TEMPERATURE. THE TWO ORDINATES ON THE LEFT GIVE THE DARK OUTPUT AND THE CORRESPONDING DARK CHARGE PER PIXEL. THE ORDINATE ON THE RIGHT GIVES THE CALCULATED DARK CURRENT DENSITY.

FIGURE 2: DARK CURRENT PUBLISHED IN 1974.

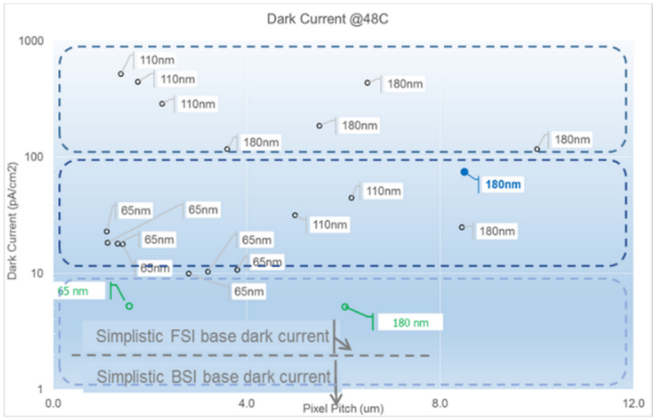
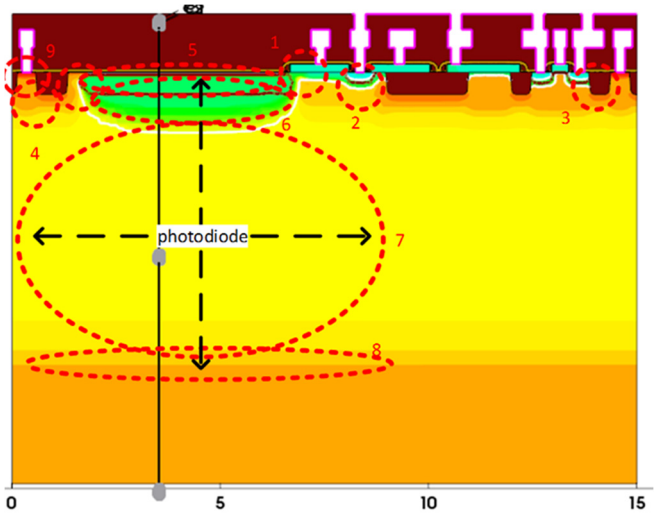


FIGURE 3: DARK CURRENT TRENDS BY TECHNOLOGY & PIXEL SIZE

Possible causes

There are a number of possible dark current sources in the pixel (Figure 4). These variously are related to defect-related traps in the band gap, direct or field assisted jumping the band gap, field=assisted tunneling or diffusive transfer. One means of distinguishing these is through there different temperature dependence based on whether or not the process is thermionic or not and, if so, what the limiting energy barrier is (Table 1).



Dark current sites within pixel:

1. **TX edge: diffusion from interface (E_g); lucky drift from interface ($E_g/2$); interface stress (E_g);**
2. FD injection: blooming forward bias;
3. Other junction: forward bias or carrier injection;
4. STI interface: diffusion from interface (E_g); interface stress (E_g);
5. Pinning layer: diffusion from interface (E_g); interface stress (E_g); doping-based SRH (E_g);
6. **Deep depletion: SRH from contamination ($E_g/2$);**
7. Lightly doped region: diffusion from weak SRH ($E_g/2$ or E_g);
8. **Back interface: diffusion from weak interface SRH (E_g);**
9. Contact substrate current (Eg)

FIGURE 4: POSSIBLE LOCATIONS OF DARK CURRENT GENERATION IN A PIXEL

Cross band-gap thermionic emission

The classic sources of dark current relate to a "lucky" carrier moving in a population of carriers finds itself in the high energy tail of the distribution with enough energy to jump to a state at a higher energy level. This is a Boltzmann process with an exponential function, ~exp(-Et/kT). For dark current the controlling barrier height is either the defect energies in the band-gap or it is the band-gap energy itself.

The physics of silicon dark current has several twists. There is a material-dependent capture cross-section for a carrier to interact with a defect state. Since silicon is an indirect band-gap material there is requirement of conserving momentum by sharing some energy with a phonon or other carrier. The dark current carrier can pick up energy, thermalizing to the lattice, while in the defect so it does not have to have the total band-gap energy. This contributes to a mid-band-gap defect generating more dark current than one near the band edge. Various thermionic processes including ones that are defect mediated and the possibility of enhancing generation by band-gap narrowing (e.g., due to stress) are possible (Figure 5).

Source	Location	Dependence	Comments
Metallics	Photodiode depletion region	• "$E_g/2$" temperature dependence (~10C doubling); • Photodiode depletion area & volume	• Reduced by bulk gettering, use of screen oxides, cleaning & implant contamination control
Interface states	TX-gate-edge depletion region	• "$E_g/2$" temperature dependence (~10C doubling); • TX gate width dependence	• Should be isolated from photodiode by bulk barrier
Substrate diffusion current	Bulk silicon (depleted & un-depleted)	• "E_g" temperature dependence (~6C doubling); • Pixel area dependence • Presence of un-depleted substrate	• Minority carrier diffusion • *Should be reduced by BSI thinning*
Pinning layer diffusion current	Photodiode pinning layer	• "E_g" temperature dependence (~6C doubling); • Pixel area dependence	• Sensitive to dielectric-induced stress
STI diffusion current	STI edge	• "E_g" temperature dependence (~6C doubling); • STI length • STI depth	• Sensitive to STI corner stress • Impact of STI engineering & depth has reduced
Back surface diffusion current	Back interface for thinned device	• "E_g" or "$E_g/2$" temperature dependence • Pixel area dependence	• Mitigated by accumulation in present BSI
Contact diffusion current	Contact	• "E_g" temperature dependence (~6C doubling)	• Diffusion through substrate from contact
Gate injection	TX edge	• Weak temperature dependence • Gate voltage dependence	• Should be isolated from photodiode by bulk barrier
Gate-induced diode leakage	TX edge	• Weak temperature dependence • Non-linear TX gate voltage dependence	• Due to high fields • Isolated from photodiode by bulk barrier
Spill back dark current	TX edge	• "E_g" or "$E_g/2$" temperature dependence • TX gate width dependence	• Should be isolated from photodiode by bulk barrier
Dopants	Bulk silicon	• "E_g" temperature dependence	• SRH with shallow traps
Auger / Impact ionization	Bulk silicon	• "E_g" temperature dependence	• Requires valence band momentum transfer • Possible photon generation

TABLE 1: POSSIBLE ROOT CAUSES FOR DARK CURRENT WITH PROPERTIES

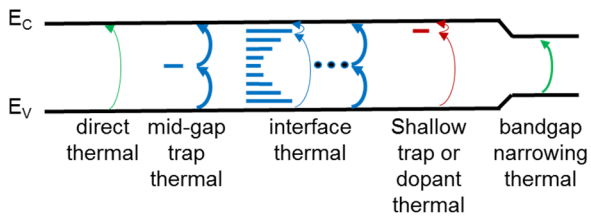


FIGURE 5: THERMIONIC MECHANISMS FOR DARK CURRENT

Mid-band-gap traps: metallics, dislocations & dangling bonds

Dark current mediated by a defect-generated trap in the band-gap is well described by Shockley-Read-Hall theory (Shockley & Reed, 1952), (Hall, 1952). Metallics readily substitute into the silicon lattice to create traps with well-defined energies and capture cross-sections leading to identifiable signatures. The generation rate is highest for traps located near the middle of the band-gap where the energy gap from the valence band and to the conduction band are nearly equal. The energy of the trap can be determined by measuring the temperature dependence with this be stronger for traps near the band edge. These defects were predominate contributors to dark current in early image sensors as cited above.

The silicon-silicon-oxide, even when optimally created, has dangling bonds with a range of configurations leading to a U-shaped trap distribution across the band gap. The density of trap states increases from those at the middle of the band but the higher generation rate of the dangling bond traps near band middle is a stronger effect and dominates the dark current generation where the interface is depleted.

The major advance in reducing dark current has been to eliminate or getter metallic to eliminate them from the collection volume in the image sensor and to improve and passivate the interfaces to reduce or turn off the related dark current generation. This effort has been very successful as shown by the shift in temperature dependence to that consistent with near band-gap transitions.

Near band-edge: doping & band-to-band

The Shockley-Read-Hall mechanism still holds for trap levels away from the middle of the band-gap. One the metallic defects are eliminated, these could become a significant source of dark current. These could be due to other defects or to dopant states. The nature of such dark current generation can be modeled in Technology Computer-Aided Design (TCAD) simulations where it is seen that the temperature dependence is the same as is commonly attributed to "diffusion current" (Figure 6). This temperature dependence is consistent with that seen in state-of-the art image sensors.

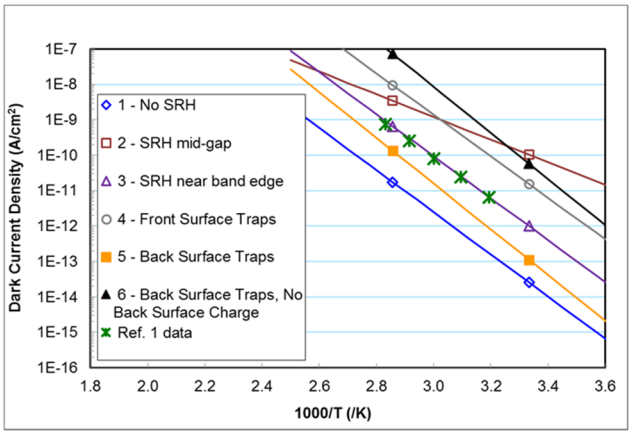


FIGURE 6: SIMULATION OF TEMPERATURE DEPENDENCE OF DARK CURRENT WITH COMMERCIAL DATA (RHODES & ET AL, 2011)

Tunneling: gate leakage

Dark current can be enhanced by high electric fields. This can be due to biasing a silicon junction so that the conduction band is pulled below the valence band across the junction to allow direct injection (Figure 7), field enhanced tunneling through the dielectric from a gate (Figure 8), gate induced drain leakage where the gate edge depletes the highly-doped diode at its edge leading to hot electron effects that create carrier multiplication and dielectric interface damage (Figure 9), and electric field enhanced defects (i.e., Poole-Frenkel effect) (Figure 10). A feature of tunneling effects is that they do not involve thermal excitation and have weak or no temperature dependent.

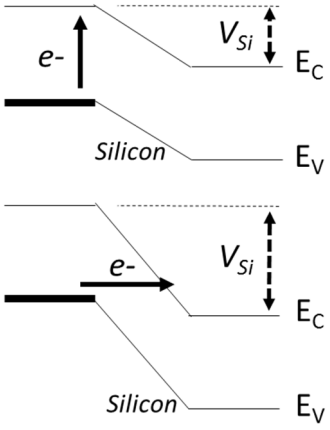


FIGURE 7: HIGH E-FIELD TUNNELING IN SILICON

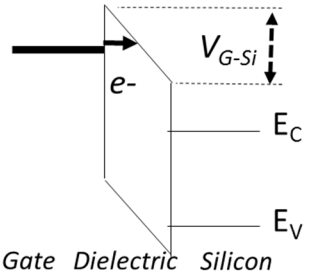


FIGURE 8: HIGH FIELD DIELECTRIC TUNNELING IN MOS

Impact of transport

Diffusion current through undepleted volumes in the silicon has a temperature dependence that is the same as that due to generation across the band-gap, Eg. This can be explained because in normal field-free transport, diffusion involves both charge random motion and equilibrium balance of generation and recombination across the band-gap. There is a question of whether this applies for image sensors where the materials are very pure yielding very long lifetimes and the charge concentration is much less than one minority carrier per pixel so that effective lifetime of a minority carrier, either dark current or photo-generated, before it falls into a depletion region and is swept away as drift current.

Un-depleted silicon has a very small, but non-zero, equilibrium concentration of minority carriers with negligible recombination probability. Collection of a carrier into a photodiode as dark current makes system non-equilibrium. Equilibrium can be restored by charge transfer from the ohmic contact so a plausible mechanism is that the junctions replenish the equilibrium concentration controlled by the transport details of the path from contact to photo-collection well.

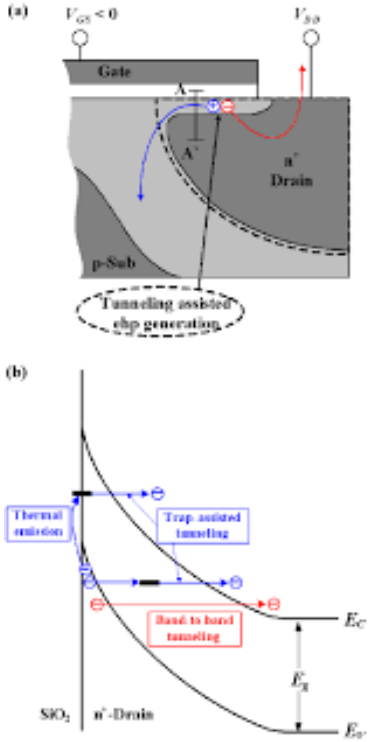


FIGURE 9: GATE-INDUCED DIELECTRIC LEAKAGE (GIDL) (CHOI, 2006)

Energy diagram in equilibrium (1) and in the presence of an electric field (2) showing field-enhanced electron emission: (a) pool-Frenkel emission, (b) phonon-assisted tunneling.

$$\tau_e = \frac{\exp((E_i - E_T)/kT)}{\sigma_n v_{th} n_i} = \frac{\exp((E_c - E_T)/kT)}{\sigma_n v_{th} N_c}$$

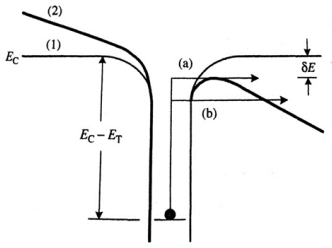


FIGURE 10: FIELD ENHANCED GENERATION (SCHROEDER, 2015)

Other mechanisms

Band-gap narrowing due to stress will decrease the barrier for thermionic dark current generation. Both compressive and tensile stress in silicon causes band gap narrowing. Result would be enhanced dark current with changed temperature dependence.

Impact ionization due to an electron gaining more than the energy of the band-gap has a finite probability of creating a photon rather than an additional electron. The result could be optical mediated dark current with the photons being in the near infrared. Temperature dependence should be weak.

Observed behavior

Characterization: probing the pixel

The starting point for understanding dark current is to gather characterization data. To get the sensitivity required to impact performance, the best vehicle is a pixel. Analysis assisted by TCAD for understanding and building a new round of pixels completes the classic experimental loop.

The voltage dependence of the dark current for a pixel can provide information on the location of the dark current source by shaping the depletion regions. This changes the volume, creates inversion and accumulation layers and moves potential barriers. It can also modulate the electric fields to look for their impact. For example, sweeping the transfer gate can show regions that depend on this voltage indicating proximity and regions that don't (Figure 11[top]). The figure shows data that, in conjunction with measurement of full well capacity (FWC) indicates that the photodiode is isolated below 0V and has a strong dependence above 0V.

The temperature variation help to narrow down the nature of the dark current source. Mechanisms with mid band-gap mechanisms have dark current increasing at a doubling rate of ~11C near 60C while mechanisms with full band-gap doubling is faster at a rate of ~ 6 C. The figure shows that for transfer gate voltages below 0V have the increase temperature dependence while for voltages above 0V there is the lower dependence (Figure 11 [bottom]). These results can be interpreted as the photodiode being isolated for below 0V and being free of metallic contamination and the influence of interface defects. Above 0V the dark current increases with the likely cause being interface states from near the transfer gate.

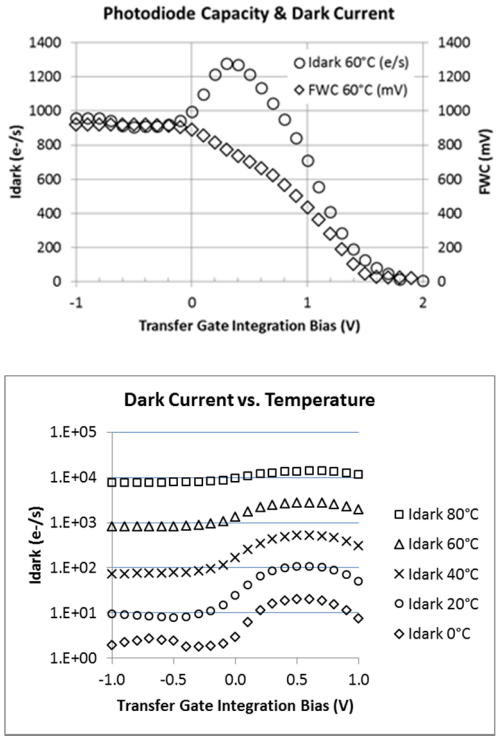


FIGURE 11: [TOP] TRANSFER GATE DEPENDENCE; [BOTTOM] TEMPERATURE DEPENDENCE

Another way to understand dark current and bright defects is to perform dark current spectroscopy (DCS) by creating a histogram of a dark frame (McGrath, Dory, Lupino, Ricker, & Vallerga, 1987). From the histogram, pixel dark current can be separated into a dark current peak at low dark current, interface states in the high dark current semi- logarithmic tail and defects such as metallic contamination in additional high dark current peaks (Figure 12 [top]).

This technique can be extended by measuring a series of dark images at a range of temperatures, pixel by pixel calculating the SRH trap energy from each pixels temperature dependence and then plotting this against the dark current on a pixel-by-pixel basis. This results provide a 2-d plot that shows that the low dark current peak is near the band edge, that the interface states produce a smooth curve that approaches the mid band-gap energy with increasing dark current and that contamination defects show up as nebulae (Figure 12 [bottom]). Note in this technique the trap energy for a SRH defect is for the larger of the two energy differences from trap to band edge so all of the data is folded into the top half of the band gap in the plot.

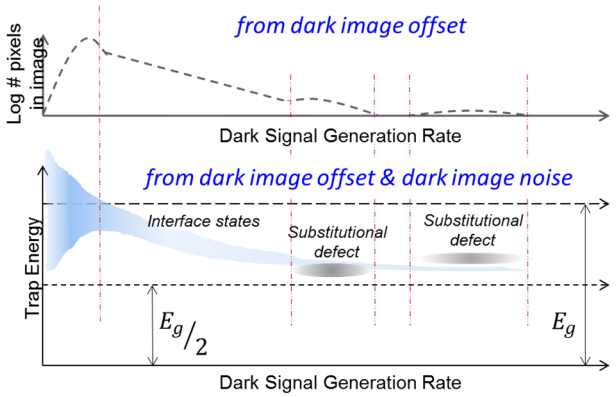


FIGURE 12: [TOP] 1-D DARK CURRENT SPECTROSCOPY (DCS); [BOTTOM] 2-D DCS

2-d DCS: voltage dependence

The 2-d DCS can be used to study the voltage dependence. Decreasing the transfer gate below 0V reduces the interface state feature that dominates so the more detailed features, including contamination clouds, become evident (Figure 13).

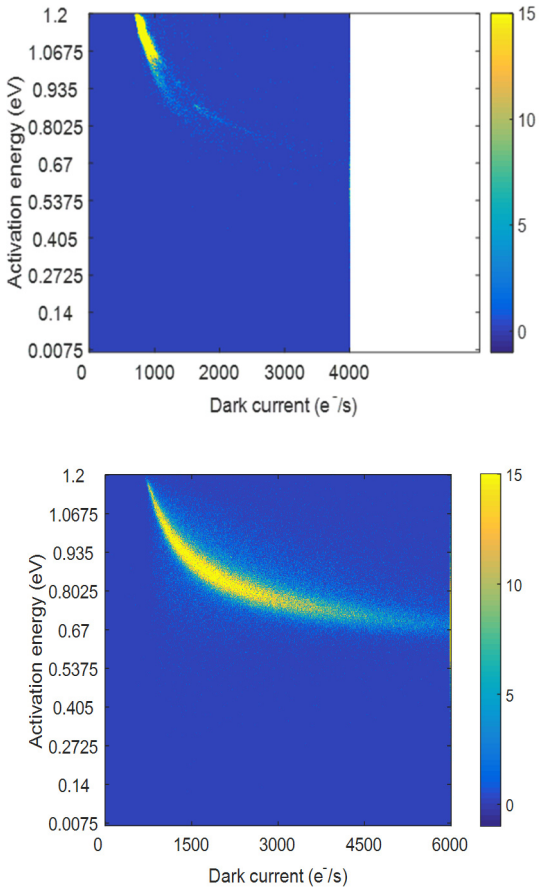


FIGURE 13: GATE VOLTAGE DEPENDENCE IN 2-D DCS [TOP] VTG < 0V; [BOTTOM] VTG = 0V

2-d DCS: temperature dependence

The 2-d DCS can be used to study the temperature dependence. Populations can be classified and tracked. Increasing temperature can add detail to the analysis (Figure 14). It should be noted that consistent with the methodology for calculating trap energy, that the charge generated by a defect near mid band gap increases at a significantly lower rate than one near the band edge.

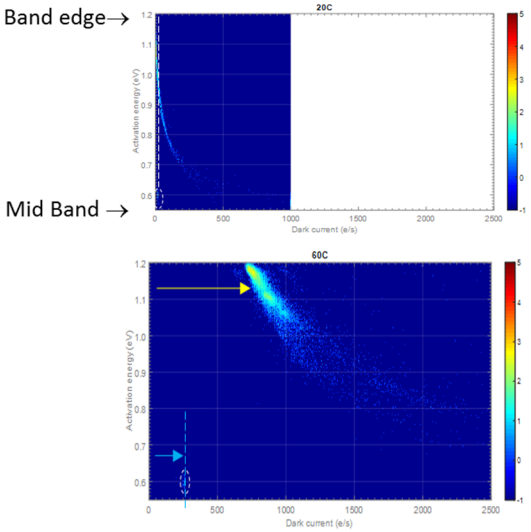


FIGURE 14: TEMPERATURE DEPENDENCE IN 2-D DCS

Discussion

Past progress & present trends in dark current

In the past dark current was primarily due to interface states. These were eliminated by use of inversion, accumulation and pinning layers. This led to the development of the CCD and CIS pinned photodiodes. Once this was understood by using DCS as a tool, "grainy "dark current was reduced by decreasing the concentration of metallics to become "bright pixels" through contamination control and gettering. This also resulted in the shift of temperature dependence shifted from ~11 C/doubling to ~6 C/doubling.

The present conundrum is that there is an assumption that dark current will continue to improve with technology modes and, while the nature of dark current seems to have changed, manufacturing improvements are still aimed at contamination that is related to ~6 C/doubling. An assumption that ~6 C/doubling as "diffusion current" does not provide an "actionable" root cause. There is no identified root cause connecting dark current to process for manufacturers or for designers.

Key attributes of the present state of dark current include that the dark current is collected from a finite volume, that the present advanced state of the technology leads to long lifetime and short transit time resulting in no significant recombination, and that all charge created, photocharge or dark current whether minority charge in undepleted volumes or majority charge in depleted volumes, are collected.

There are the Interesting questions related to the ultimate limit for decreasing dark current: What is the lower limit for dark current in "defect free silicon" and how far away is it from the present levels? Will this limit mean process is "as good as it will get"? Will knowledge of this lead to design opportunities.

Limits of dark current in silicon

As an example of what the limit of dark current could be in silicon, a simple model based on the assumption it will be dominated by an Auger process and that the photodiode structure is made up of a pinning layer, a depleted photodiode volume and an undepleted volume below the photodiode. The Auger process is necessary because of the indirect band-gap in silicon and the need for a photon or phonon in addition to the dark current carrier in order to conserve momentum. The assumption is this model is that the dark current generation is driven by how far the silicon in each volume is from its equilibrium state (Figure 15). The lifetime used in the model is that for measured for the Auger process (Figure 16).

The model calculates a generation rate for each of the three regions based on doping concentration and volume. The results when comparing a backside illuminated (BSI) pixel (Figure 17) and a frontside illuminated (FSI) pixel (Figure 18), that the BSI pixel should have higher dark current contributed by its deeper depletion volume, but that it has much lower total dark current because of the removal of the undepleted collection volume. The result of this simple model is that the limit for FSI pixels may be close at hand, but that the limit for BSI is significantly below the present measured values.

a. Model is for deep-depletion photodiode, undepleted pinning layer & undepleted substrate
b. E_g = 1.12eV
c. Lifetime is limited by Auger process:
    a. electron promoted into conduction band
    b. hole created in valence band
    c. electron or hole that conserves momentum
d. Generation lifetime equals equilibrium recombination lifetime: $\tau_{1/2} = 2.5 \cdot 10^{-3}\ s$
e. No recombination occurs because electrons generated are swept away due to electric fields
f. Charge generation depends on Δn, the concentration difference from equilibrium

FIGURE 15: MODEL FOR DEFECT-FREE SILICON DARK CURRENT

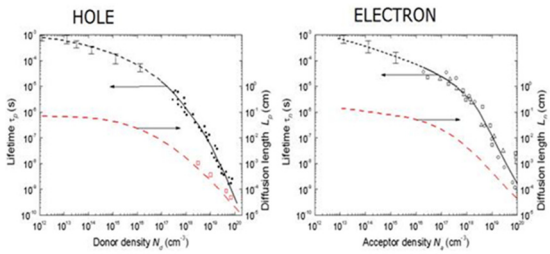


Figure 1. Hole and Electron Bulk Lifetime for different Silicon Doping [3-4]

M. S. Tyagi and R. Van Overstraeten, Minority carrier recombination in heavily-doped silicon, Solid-State Electron.,vol. 26, pp. 577 1983.

FIGURE 16: AUGER PROCESS IN SILICON

$$G^{BSI} = G^{dd}_{BSI\,(2.5\,\mu m)} + G^{pin}_{(0.1\,\mu m)} + G^{collect}_{BSI\,(0\,\mu m)}$$
$$= 1.5 \cdot 10^{-8}\,{}^{pA}/_{cm^2} + 6 \cdot 10^{-5}\,{}^{pA}/_{cm^2} + 0\,{}^{pA}/_{cm^2}$$
$$= \mathbf{6 \cdot 10^{-5}\,{}^{pA}/_{cm^2}}$$

FIGURE 17: DARK CURRENT GENERATION MODEL FOR BSI (27C)

$$G^{FSI} = G^{dd}_{FSI\,(1.5\,\mu m)} + G^{pin}_{(0.1\,\mu m)} + G^{collect}_{FSI\,(6.5\,\mu m)}$$
$$= 9 \cdot 10^{-9}\,{}^{pA}/_{cm^2} + 6 \cdot 10^{-5}\,{}^{pA}/_{cm^2} + 1.4 \cdot 10^{-1}\,{}^{pA}/_{cm^2}$$
$$= \mathbf{1.4 \cdot 10^{-1}\,{}^{pA}/_{cm^2}}$$

FIGURE 18: DARK CURRENT GENERATION MODEL FOR FSI (27C)

Conclusions

In summary, the nature of the dark current has gone from "gray" background to quantized snow and back to "gray" background. It is about to again be quantized, this time in space & in time. A significant part of this advance is based on the Shockley-Read-Hall mechanism which provided understanding to eliminate the predominant sources of dark current. But the present state of dark current is no longer explained by this mechanism and there is no root cause at present to understand how to proceed. When there is an identified root cause then there is the possibility for improvement through design. There is a need for data & analysis.

Commercial pressures will continue to push to reduce dark current. While there is a general view that improvement is natural fallout from advancing technology nodes, this improvement will require identifying root causes of the dominant defect different than those in the past. This understanding will provide the opportunity for design-driven improvement.

It is unclear when dark current will hit the limit of pure silicon where process improvements will no longer help and further advances will have to come from device design. There will be a point when silicon rather than defects becomes the limitation and when only design-driven improvements will be possible.

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Author Biography

Dan McGrath has worked for 38 years specializing in the device physics of silicon-based pixels, CCD and CIS, and in the integration of image-sensor process enhancements in the manufacturing flow. He chose his first job because it offered that "studying defects in image sensors means doing physics" and has kept this passion front-and-center in his work. He has pursued this work at Texas Instruments, Polaroid, Atmel, Eastman Kodak, Aptina and BAE Systems and has worked with manufacturing facilities in France, Italy, Taiwan, and the USA. His publications include the first megapixel CCD and the basis for dark current spectroscopy (DCS).