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A Lateral Electric Field charge Modulator with Bipolar-gates for Time-resolved Imaging

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Abstract

This paper reports high time-resolved imaging technique using a lateral electric field charge modulator with bipolar-gates. The proposed pixel structure achieved high time-resolved signal detection by using negative bias effect by work function difference between the p-type gate and p-substrate. The test chip fabricated in 0.11 um CIS technology demonstrates the high-speed charge modulation, and the modulation contrast is measured to be 97%.

Introduction

Time-resolved image sensors have wide range of applications such as time-of-flight (TOF) range imaging [1], [2] and a biological imaging like fluorescence lifetime imaging microscopy (FLIM) [3], [4]. There are two kind of methods in time-resolved imaging. One is a direct measurement of photon arrival time using single-photon avalanche diodes (SPADs) and a time-to-digital converters (TDCs) [5]. SPAD-based time-resolved imagers have a relatively high time resolution. However, typical SPAD-based imagers need a complicated and a large amount of in-pixel circuitry for TDCs. The spatial resolution of the SPAD-based time-resolved imagers is limited on this account. The other method is a mechanism of time-dependent photo charge modulation. Sinusoidal or pulsed light modulations are used for phase or delay measurements by demodulating it in the lock-in pixels. This charge modulation method enables compact in-pixel circuit and a high fill factor. In this method, it is very important to develop lock-in pixels with high-speed charge modulation, high modulation contrast and loss-less accumulation because it is necessary to modulate photo charge which occur in a very short period of time. To satisfy these requirements, a lateral-electric-field charge modulator (LEFM) have been proposed [6]. Since the LEFM pixel does not have any transfer gates in a signal path, high-speed charge modulation and loss-less charge accumulation can be achieved.

Conventional LEFMs, however, requires a negative gate bias to enhance a potential change in the channel. A negative power supply with low impedance is necessary in the camera system. In addition, the requirement of negative bias becomes a big problem to introduce an in-pixel buffer, which is effective to attain high-speed charge modulation in a two-dimensional pixel array [7]. Negative drive pulses lead to a forward bias in a p-n junction between the substrate and a source of NMOS transistor in the in-pixel buffer. For this reason, an isolation layer (Deep N-well) is required, and this leads to significant reduction of fill factor.

This paper presents a LEFM with bipolar-gates. The proposed pixel structure uses negative bias effect by work function difference between the p-type polysilicon gate and the p-substrate. By using this structure, the negative power supply is unnecessary, and the isolation layer also can be removed to implement the in-pixel buffer. Thus, it is possible to obtain a high-speed charge modulation while maintaining a high fill factor.

Conventional Lateral Electric Field charge Modulator

Figure 1 shows the structure of two-tap LEFM with a drain, in which two sets of gates (G1 and G2) creating a lateral electric field are used. The gates are not used for transferring charge through the gate, but for controlling electric field of X-X' direction by changing the hole concentration of the pinned photo diode surface. To do this, a positive voltage (HIGH=2.0V) and negative voltage (LOW=-1.0V) are used for the operation. For example, when G1 is HIGH and the others are LOW, photo electrons generated in the aperture region is transferred to FD1 within a short time. The direction of electron flow in a pinned photodiode is controlled by the gates, and time-resolved signal detection and accumulation are carried out in the two floating diffusions (FD1 and FD2). Since the LEFM pixel does not have any transfer gates in a signal path, high-speed charge modulation and loss-less charge accumulation can be achieved. These characteristics of LEFM are very suitable for indirect TOF method and biological time-resolved imaging like FLIM. During signal readout, GD is ON and other gates are OFF for preventing the influence of background light.

A challenge of the conventional LEFM structure is the requirement of negative gate bias. In the LEFM, doping concentration of surface p+ layer in pinned photodiode is designed to be relatively low. The gates (G1 and G2) modulate hole concentration of the surface, which creates channel potential modulation. For a large potential change on the channel by the gates and reduced dark current, negative drive pulses are necessary in the conventional LEFMs. Due to the necessity of negative bias, there are some limitations on implementation. For example, the image sensor should have a negative supply with low impedance because the impedance of negative power supply influence to modulation speed of the LEFMs. The other limitation from the negative gate bias is on an implementation of a buffer or pulse generation circuits in pixel. To use negative driving pulses for the in-pixel driver, an isolation layer like Deep N-well is needed because the negative driving pulses lead to a forward bias in a p-n junction between the substrate and a source of NMOS transistor in the in-pixel buffer. The isolation leads to a significant reduction of fill factor.

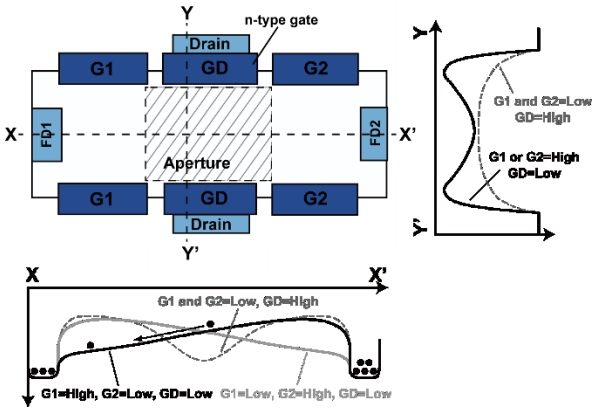

Figure 1. The structure of two-tap LEFM with a drain

Lateral Electric Field charge Modulator with Bipolar-gate

To develop a LEFM without negative gate bias, we fucus the work function of the polysilicon in this study. Figure 2 shows a band-enegry diagram of a n-type polysilicon and a p-type polysilicon. The work function of the polysilicon is changed by the dose of polysilicon. In standard CMOS image sensors, n-type polysilicon heavily doped by N+ layer is widely used as a gate material, and the N+ layer is also used for doping of NMOS source/drain. The fermi level of p-type polysilicon is close to valence band while that of n-type polysilicon to conduction band, and the work function difference between the polysilicon gate and the silicon substrate causes a band-bending even at zero bias. Due to the work function difference, the potential of the p-type gate shifts to negative, while that of n-type polysilicon shifts to positive. Therefore, when the gate materital is changed from n-type to p-type, a negative bias effect by the difference of those work functions (nearly equal to the bandgap potential) is obtained.

To investigate the negative bias effect of p-type gate, simple LEFM structures with n and/or p-type gates are simulated by a 3D device simulator, as shown in Figure 3. Figure 4 shows a simulated channel potential as a function of the gate voltage for various widths of the p-type gate and n-type gate. From this result, as the width of p-type gate is wider, the onset of "pinning" at the channel shifts to higher gate voltage. The channel potential of all n-type gate is pinned at -1.0V, while that of all p-type gate is pinned at 0V. In other words, all p-type LEFM with 0V bias is equivalent to all n-type gate with -1.0V bias.

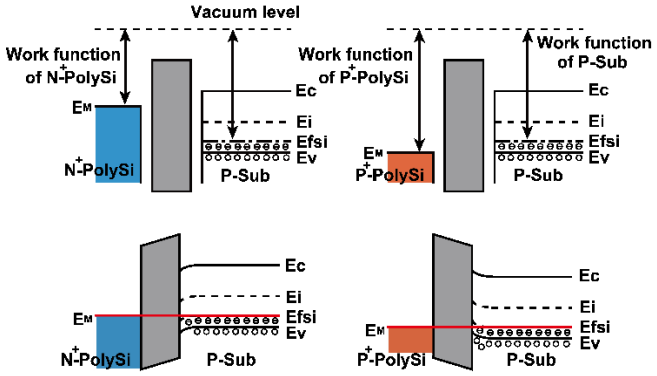

Figure 2. The band-enegry diagram of the n-type polysilicon and the p-type polysilicon

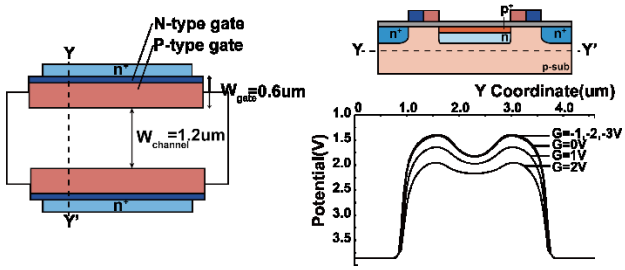

Figure 3. The simulated structure

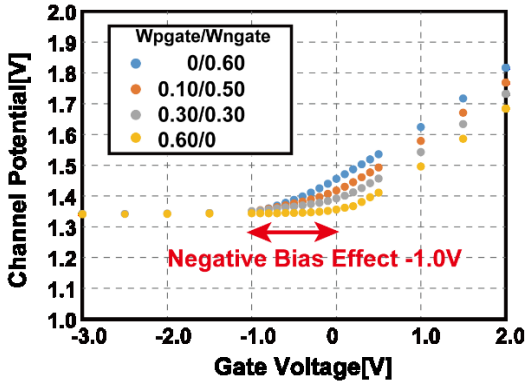

Figure 4. Channel potential versus Gate voltage

Figure 5 shows the structure and potential of the three-tap LEFM with the bipolar-gates. The proposed pixel structure employs p-type gates as well as n-type gates unlike the conventional structure in which the only n-type gates is used. Since the bipolar-gates structure helps to modulate lower potential at zero bias by work function difference between the p-type gate and p-substrate, the negative gate bias is not required in the modulation pulses. Only a positive voltage (HIGH=2.5V) is used. A low voltage is connected a ground voltage (LOW=0V). The bipolar-gates structure has a larger potential modulation compared to the n-type gates structure by work function difference between the p-type gate and p-substrate. In this design, the n-type gate is necessary to form a drain which is along with the modulation gates. The n-type gates is necessary to form drains along the each gate, which plays a role for reducation of unwanted charge accumulated under the gates.

Figure 6 shows the simulated potential and a trace of a generated electron when GD is HIGH and the others are LOW. The black dot indicates an initial position of generated electron, and the , the red dashed line shows an electron trajectory. The simulated transfer time is about 200ps. Figure 7 shows a 3D plot of the simulated potential. From the reslut, we comfirm that the potential gradient for high speed charge modulation is created by the bipolar-gates.

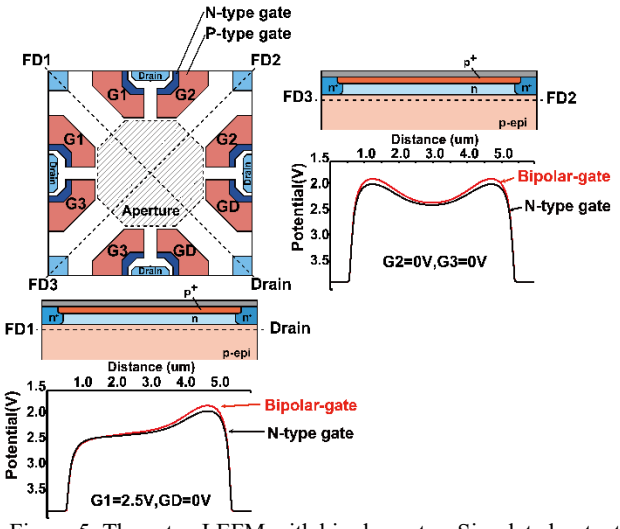

Figure 5. Three-tap LEFM with bipolar-gates. Simulated potential for FD1-FD2, and FD3-FD4 is also shown when G1 is 2.5V, and the G2, G3, and GD are 0V.

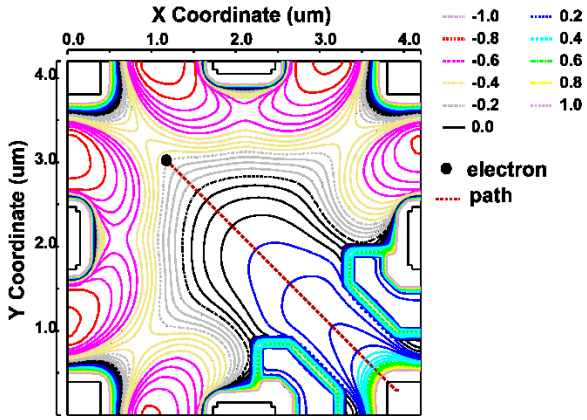

Figure 6. Simurated two dimensional potential and charge trandfer path.

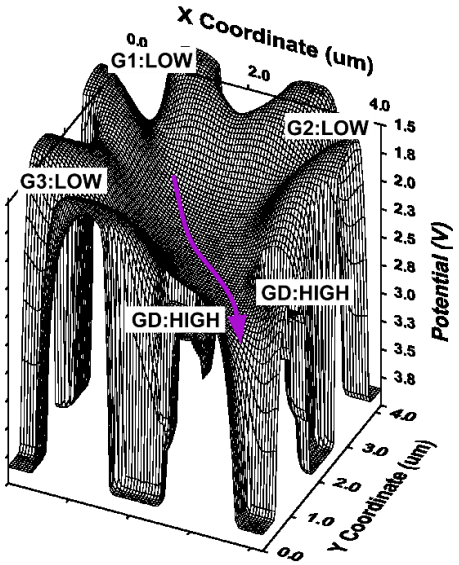

Figure 7. Simurated three dimensional potential

Measurement result

To proof the concept of the proposed 3-tap LEFM with biplolar gates, a test chip is implemented by using a 0.11um CMOS image sensor technology. The unit size of the proposed 3-tap LEFM is 4.2um x 4.2um. Each pixel has 60 LEFMs, and three channel of readout circuit. In order to increase a full well capacity, these FD nodes are connected to MOS capacitors.

Figure 10 shows the modulation method for three-tap LEFM. By using the three tap strcture, for example, TOF calculation is performed by outputs of FD1 and FD2. By subtracting the output of FD3 from FD1 and FD2, the background light and darkcurrent offset are canceled. In the measurement setup, a 448nm laser with a pulse width of 72 ps is used for the light source. The emission trigger of the laser is given by the sensor board via a digital delay generator (DDG) which can accurately control the delay time of laser trigger. The change of trigger delay is equivalent to the change in the time-of-flight. The high level for gate voltage of G1, G2, G3 and GD is set to 2.5V, and the low level is set to 0V. Figure 11 shows normalized pixel outputs: N1, N2, N3, and the differential value of N2 as a function of the trigger delay. The differential value of N2 corresponds to the photocurrent. As the delay of laser trigger increases, the output of N2 increases due to the following reason. When the delay equals zero, since the received light is earlier than the rising edge of G2 pulse, all the photocurrent flow into the FD1. As the delay increases, the falling edge of the photocurrent is first included inside G2 open time or accumulated in the FD2. The rising edge is then accumulated. The rising and falling time of photocurrent are measured to be 200 ps and 400 ps, respectively. The modulation contrast is also measured to be 97%.

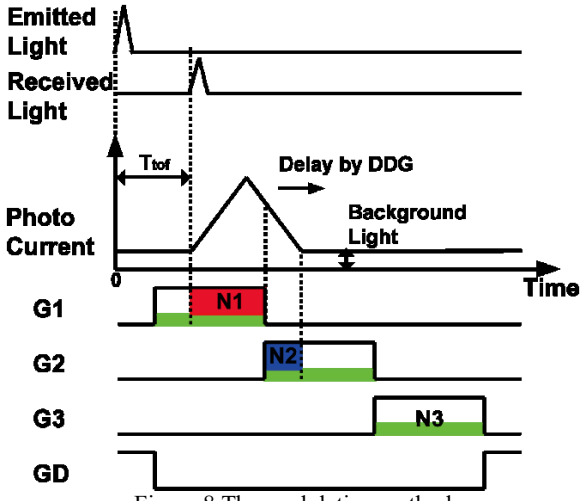

Figure 8.The modulation method

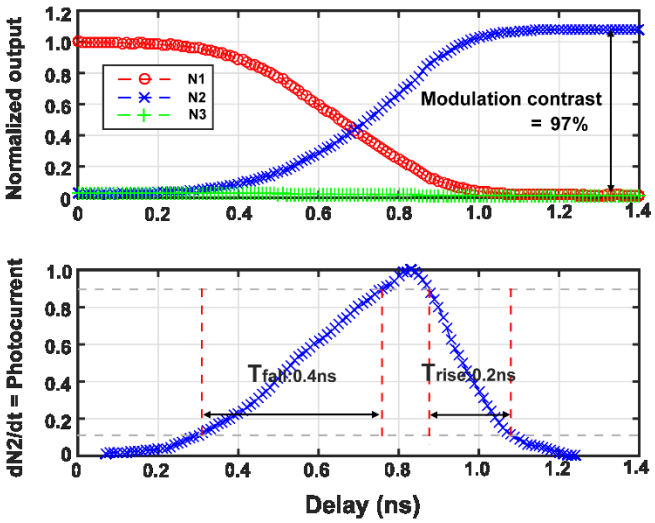

Figure 9. The modulation characteristics

Conclusion

This paper presented a new LEFM structure using bipolar-gates. The proposed structure uses negative bias effect by work function difference between the p-type gate and p-substrate. The test chip fabricated in 0.11 um CIS technology demonstrates the high-speed photocurrent response of 200ps, and the high modulation contrast of 97%. This structure is expected to improve the time resolution in fluorescence lifetime imaging and TOF range imaging.

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