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Octagonal CMOS Image Sensor for Endoscopic Applications

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Abstract

An octagonal shaped CMOS image sensor (CIS) has been developed for endoscopic applications. The octagonal shape of the outlined die is also applied to the pixel matrix which has suppressed corners, resulting in an octagonal pixel matrix of 422'640 effective pixels. The sensor die fits on a circumference of 3.2 mm diameter being this the best die cut ratio between the cut corners and the pixel placement. The missing pixels on the corners are internally compensated by the readout electronics to maintain a rectangular image output format of 680x680 pixels. This paper presents the solutions found to overcome the layout challenges of fitting both row and column logic on the same side of the diagonally cut corners. Furthermore, the sensor features an area efficient column parallel ADC converter, having on the column readout side, only 402 µm overhead total space between the utmost pixel row until the edge of the silicon die. This space is used to place CDS, ADC, column addressing, readout, additional electronics and power routing. The sensor also has a fully autonomous operation, requiring only an external clock supply to drive the internal state machine. The interface requires just 6 connections: 2 for power supply, 2 for bi-directional data and 2 for main clock supply. The frame rate and the exposure are configurable by register. The maximum frame rate is 50 frames per second (FPS) and data is delivered over LVDS serial data link. The integration time can be configured from 147 µs to 20.1 ms. The power supply is 3.3 V with internal Power-On-Reset (POR) and has a power consumption of 91 mW manufactured in 180 nm CIS process.

Key-words: CMOS Image Sensors, Round Sensor, Endoscopy, ADC, Medical Imaging.

1. Introduction

Nowadays, endoscopy techniques are widely used to achieve accurate diagnosis of internal human body diseases and perform minimally invasive surgery. The aim for minimally invasive surgery and diagnosis, drives the endoscope manufacturers and miniature image sensors suppliers to develop ever smaller devices that better fit minimal diameter body cavities. [1]

However, there are physical constraints that limit the use of common miniature CMOS Image Sensors (CISs) [2][3]: the standard endoscopic equipment with distal image sensor technology (chip-on-tip-endoscopes) use cylindrical packages [4], while the miniature image sensor dies are typically rectangular or square shaped [5][6]. These aforementioned differences result in an unused space not filled with photosensitive pixels or readout electronics. On the other hand, the semiconductor industry is not prepared for geometries other than orthogonal right angle designs (square or rectangular), being a challenge to design integrated circuits and electronics that do not match this standard.

Additionally, the lenses and micro-lenses are designed and manufactured with a spherical shape [7], resulting in aberrations and optical distortions on the corners of the rectangular captured images, especially observed with wide Field-of-View (FOV) lenses.

An octagonal shaped pixel matrix was already presented in [8]. However, in the architecture proposed on this paper, not only the pixel matrix but also the die have an octagonal shape in order to accomplish one of the initial requirements: to fit in a circular package and to have an extended photosensitive area. The outlined device aims to meet this requirement by matching the entire die to an octagonal shape. Not only the matrix but also the readout electronics in the corners, were designed at a 45º angle.

Since the semiconductor industry recommends up to 45º angle layout, the cut corner solution with this figure in mind was adopted. The ratio of suppressed pixels was selected to be the best fit between the circular shape of the package, the pixel matrix size and the space needed for readout electronics around the matrix.

2. Architecture and operation

The presented sensor is a miniature area scan sensor with octagonal shape. This sensor has a typical four transistor pixel (pixel pitch: 2.78um). In order to increase the fill factor, it has a two-shared pixel architecture. The matrix is processed with a rolling shutter, which means, one row is selected for readout while a defined number of previous rows are in reset, and all the others are in integration. The integration time can be programmed by changing the registers configuration, assuming the frame rate is 50 full frames per second, the maximum integration time is limited to 20.1 ms.

The ADC conversion is performed by a 9 bit ramp ADC full linear conversion. This ADC has the possibility to enable a dual slope ramp mode, applying a different gain to the low light level signals. This scheme helps reduce the AD conversion time without losing dynamic range.

Each column has an ADC and converts each pixel value from the selected line storing the value in a SRAM. After this process, all the values stored in the SRAM are readout sequentially by a complementary bus, and mixed between top and bottom side (Figure 1). Only after the data between both sides is mixed, it is serialized to the output. The above readout structure was implemented in a pipeline allowing for the pixel to be read while, at same time, the output data is being processed. The output data word is composed by 12 bits, adding to the 9 data bits, 3 more bits, used for start and stop signaling, and also for parity (start bit + data (9bits) + parity bit + stop bit). This bit was included to allow for error detection on the user side.

This project is a self-timed image sensor and operates in a free running master mode. After power up, the sensor performs an internal power-on reset, and then starts the integration and readout process autonomously, following a loop of 3 operation modes: synchronization mode, readout mode and interface mode. During synchronization mode the sensor transmits a training pattern to allow for sensor data synchronization. After synchronization, the sensor enters into readout mode and starts to transmit valid data information (line number, image data and also training pattern, to maintain synchronism). As soon as data is transmitted, the sensor

enters into interface mode. During this mode it is possible to write and update the register configuration.

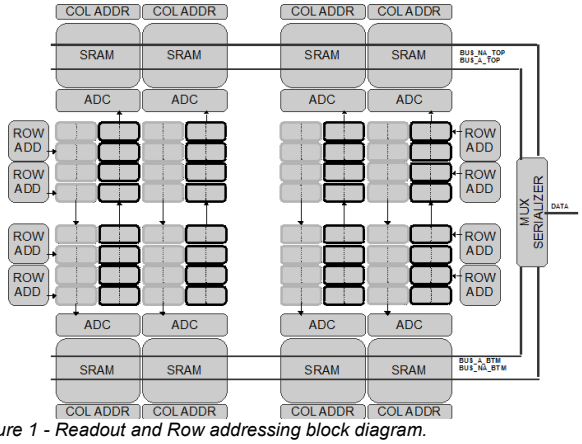

Figure 1 - Readout and Row addressing block diagram.

This sensor uses a semi duplex data interface. During readout mode, LVDS standard communication is used to transmit data downstream and during interface mode, the sensor switches to a common coupled two-wire serial interface to allow for the reception of configuration data.

To operate the sensor, the only requirement is that a power supply and an external clock be provided to drive the internal state machine. The sensor interface requires just 6 connections: 2 for power supply, 2 for bi-directional data communication and 2 for external clock (main clock). The main clock frequency can range between 25 MHz and 50 MHz.

2.1. Octagonal shape: design and layout challenges

Although the standard image format is squared, typical scope display panels show round images [4], as presented on Figure 2-*right*. Therefore for endoscopic applications, a round image sensor would be ideal. Of course, in practice, that is not feasible, however the round shape can be approximated by an octagon. This sensor was designed following this premiss.

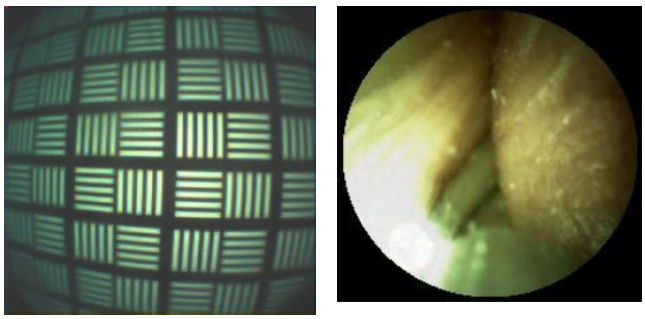

Figure 2 – Resolution test chart 120deg Lens (left side) vs scope display panel (right side).

The sensor die was designed to fit on a circumference with a diameter of 3.2 mm (Figure 3), in order to meet the commonly used endoscopes area, which is 10.3 mm^2 [10]. The octagonal shape of the outlined die is also applied to the pixel matrix, which has reduced corners, resulting in an octagonal pixel matrix of 422640 effective pixels. Even though the matrix is octagonal, the transmitted data maintains a square output format of 680x680 pixels, to maintain compatibility with image data formats used in standard displays. The missing pixels on the corners are internally compensated by the readout electronics to allow for the square output format. The digital value for those inexistent pixels corresponds to a black pixel.

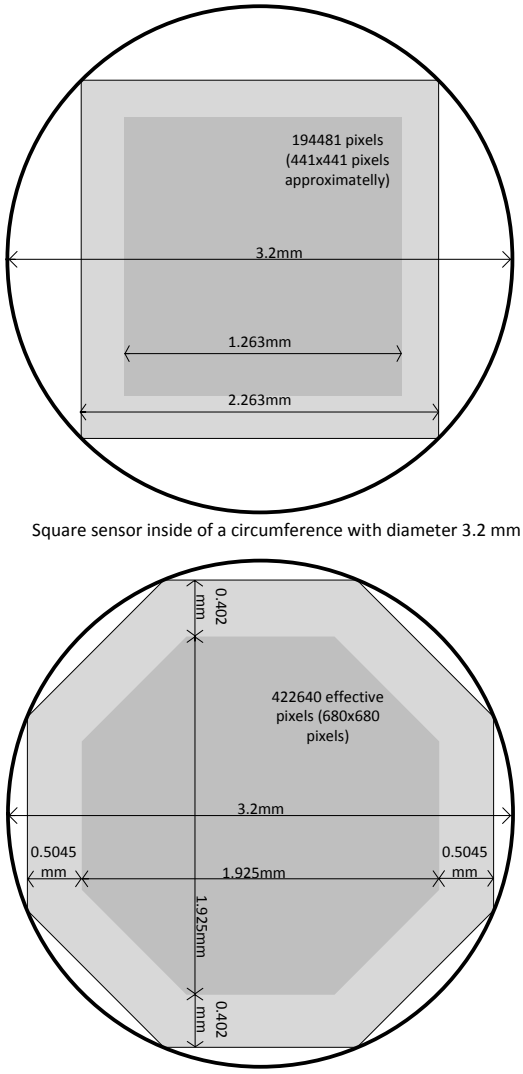

Figure 3 - Octagonal sensor (bottom side) vs same round package with square sensor (top side) with extrapolated number of pixels when assuming same pixel pitch and same row column circuitry overhead.

The sensor die area is 6.84 mm^2 and the pixel matrix represents approximately 49.6% of this area. The periphery space from the die edge to the pixel matrix on the left and right sides, is just 504.5 µm wide and includes the seal ring, and circuit area. On the top and bottom sides, the periphery space from the die edge to the pixel matrix is 402 µm. These dimensions are represented in the Figure 3. This geometry allows for a higher resolution and a better use of available space when compared with a square sensor contained inside the same circumference. On the top side of the figure a square sensor with 5.12 mm^2 is represented. Assuming a circuit area similar to the one used in the outlined device (0.5 mm per side), a typical square shaped sensor would have a pixel matrix of approximately

194481 pixels, much less than what was possible to achieve in the presented design - 422640 effective pixels.

On the other hand, the layout of the octagonal shape is challenging and strategies were implemented on this sensor to save space and take advantage of the available circuit area. Those strategies can be divided into two groups: floorplan distribution and layout orientation. For the floorplan distribution two main actions were implemented, block splitting and overlapping the row and column addressing on the corners.

As shown in Figure 4, row addressing is split, i.e., the odd rows are addressed by the left side, and the even rows by the right side (as presented on Figure 1). This allows for the cell area to be optimized. The same strategy was applied to the readout blocks (ADC, SRAM and column addressing), the odd columns are selected by the bottom side blocks and the even columns by the top side.

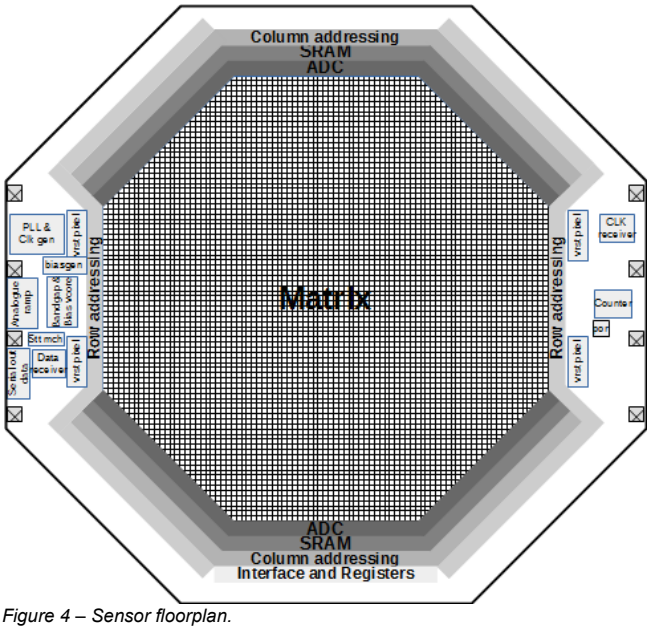

Figure 4 – Sensor floorplan.

To perform the readout of the octagonal matrix, the row addressing, column addressing, SRAM and ADC electronics extend along the corners, as shown in Figure 4. These blocks were designed at a 45º angle. To design the blocks at 45º angle was a challenge, firstly because the orientation is not the standard for the designer and second because all possible errors derived from the non-standard layout design should be considered. It was necessary to analyze the verification errors with a critical mindset, since the design tools have limitations regarding circuit layout at non-orthogonal angles. It is common to have property errors due to the device size, since in a 45º angle layout it is difficult to meet the absolute values enforced by the process rules, so the device size and the space between them are an approximation. However, this approximation comes at a cost of increased area use. This increment is reflected on the ADC size, where the ADC layout length at 45º angle is 20% longer than the equivalent block designed at 90º angle. The increased length resulted from the fact that to meet foundry design rules, contact and vias were placed with orthogonal orientation, while metal and poly extensions were kept at 45º rotation, resulting in additional contact / via extensions and thus increased the distances between them. Finally precautions had to be taken to avoid off grid errors for 45º orientation.

2.2. Lenses prototype with circular shape

For the current design a circular shape lenses stack compatible with the sensor and endoscope package, was developed. These lenses are Wafer-Level module with one central stack of lenses and a field flattener close to the pixel matrix. In Figure 5, is possible to observe a prototype lenses in a miniature CMOS image sensor for endoscope application (in the photo, a square sensor of 1x1 mm [6] was used with prototype lenses).

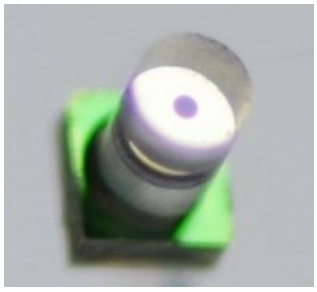

Figure 5 - Round lens prototype on a square image sensor of 1x1 mm.

2.3. Packaging

The sensors were packaged in a standard optical TSV chip scale package technology with an air cavity above the pixel area to allow for pixels with micro lens. The octagonal total form factor was realized by laser trimming the corners after diamond blade rectangular cutting.

3. Evaluation and Results

In Figure 6, the test platform used to evaluate the sensor is shown. The device is interfaced through a FPGA and data is transmitted to a PC-based viewer over a USB 3.0 interface. A system synchronous deserialization architecture is used to sample the sensor data (Figure 7).

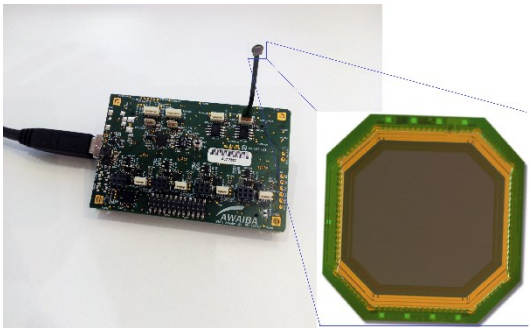

Figure 6- Sensor evaluation platform.

A synchronization state machine performs the bit and word alignment before the parallel data output is stored in memory. The memory read control re-orders the pixel data to correct for the odd/even column readout and forwards it to the USB 3.0 dedicated interface using a custom image protocol. Register control is also implemented on the FPGA logic: commands sent through the USB interface are decoded and re-transmitted to the sensor during the frame break. The clocking is provided by the internal FPGA PLL

resources. Alternatively, an additional quartz oscillator placed on the sensor module can be used to reduce the cabling, to just 4 connections.

The described CIS chip was characterized according to EMVA1288 guidelines [9]. For the displayed characterization results, preliminary prototype samples without per pixel micro lens are reported. Dark current, given in electron/second, was calculated at an ambient temperature of 25 ºC and 50 ºC based on the conversion gain obtained from the photon transfer plot seen in Figure 8.

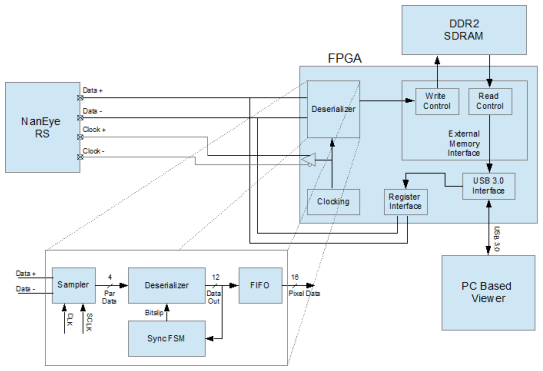

Figure 7 - Block diagram of the FPGA firmware.

Peak quantum efficiency was also determined based on the linear fit of the curve obtained when the temporal variance is plotted as a function of the dark corrected signal, in this case represented in the number of electrons. Figure 9 portrays the mean pixel value as a function of the exposure time, the resulting curve allows the extraction of the dark current as being 2076 *e-/s* at 25 ºC. Figure 10 depicts quantum efficiency against the light wavelength. The peak value was determined to be between 624 nm and 629 nm.

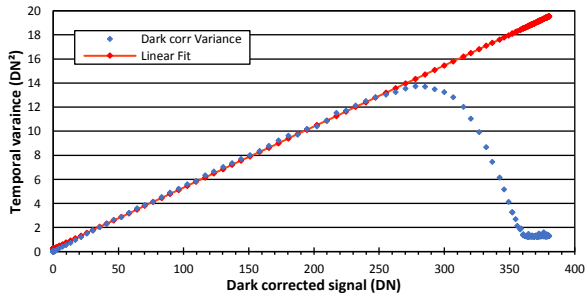

Figure 8 - Photon transfer plot.

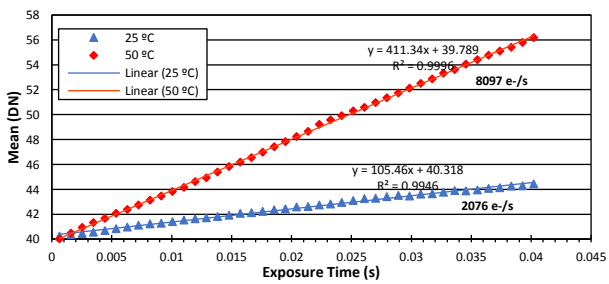

Figure 9 - Dark current measurements at 25ºC and 50ºC.

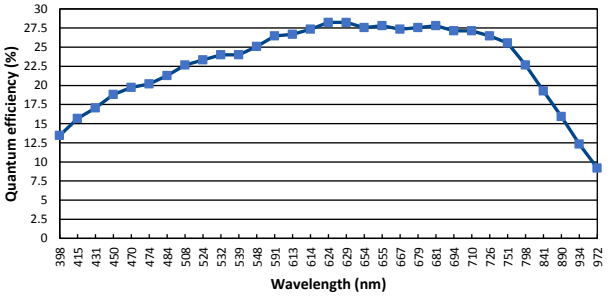

Figure 10 - Quantum efficiency measurements.

Table 1 summarizes the performance of the image sensor. The 9 bit ADC resolution plays a role on the maximum SNR and dynamic range. On the other hand, it benefits from a reduced FPN and relative low temporal noise. This noise level translates into images as the one shown in Figure 11. Even though minimal image correction was applied: image averaging and bad pixel removal.

Table 1 - Performance summary.

Parameter	***Value***
Number of effective pixels	422640
Pixel size	2.78 µm x 2.78 µm
ADC resolution	9 bit
Power Consumption	91 mW
Conversion Gain	0.0508 DN/e-
Peak QE	28.64%
Saturation Capacity	5370 e-
SNR	37.32 dB
DYN	50.94 dB
Responsivity	3.55 DN/nJ/cm^2
Linearity Error 5% - 95%	0.2%
Temporal Noise Dark	13.2 e-
DSNU$_{rms}$	44 e-
PRNU$_{rms}$	1.62%

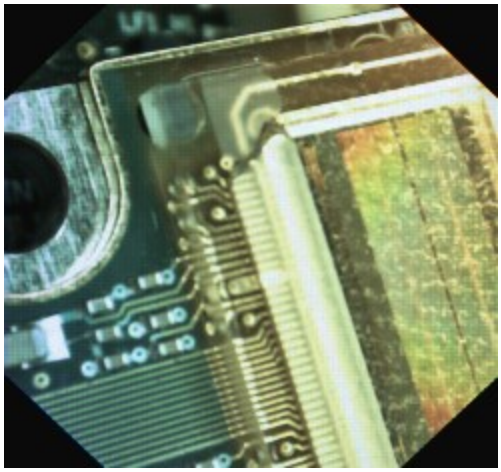

Figure 11 - Sample color image taken under uniform illumination.

A bilinear color reconstruction algorithm was used to extract color content from an RGB sample. The pixels on the cut corners are assumed to be usable data. This allows the interface to maintain

the standard square image format compatible with typical display systems. Although actually the cut corners are represented as dark pixels.

In addition to the typical characterization, the study of possible effects resulting from the 45º cut corners is of interest. A small gradual increase of the dark level was observed along the columns with 45º cut corners. The image portrayed in Figure 12 was contrast enhanced to highlight this effect. This is more clearly visible in the plot of the line and column averages shown in Figure 13. Where a gradient of 5 DN (9 bit pp) can be observed on the line/column average plot.

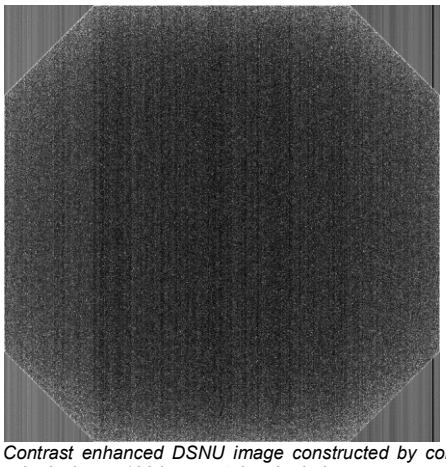

Figure 12 - Contrast enhanced DSNU image constructed by computing the average of each pixel over 100 images taken in dark.

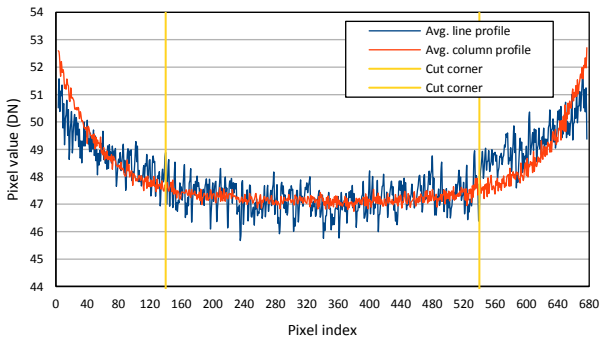

Figure 13 – Average line and column profiles over a DSNU image.

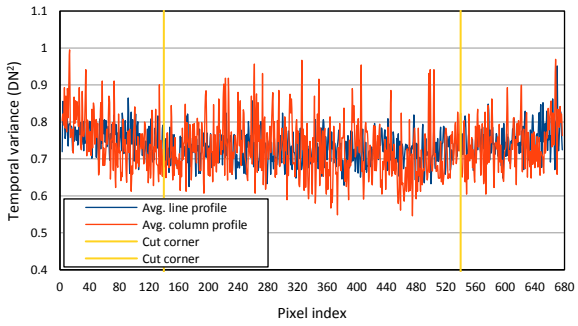

Figure 14 - Average line and column profiles over a temporal variance image in dark. Image was constructed by grabbing a single image in dark and subtracting from it the DSNU image.

This effect is also reflected in the temporal variance and PRNU where deviations for the rows and columns that contain the cut corners can be observed on the row and column averages depicted on Figure 14 and Figure 15. As the increase is gradual it however remains unnoticeable to the eye, even in uncorrected images.

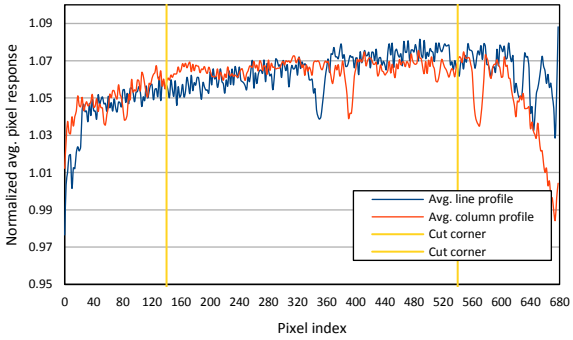

Figure 15 - Average line and column profiles over a pixel response image considering red color channel only.

The pixel response, represented on Figure 15, was obtained for each pixel (i,j),

$$Pixel_{response}(ij) = \frac{PRNU_{Image}(ij) - DSNU_{Image}(ij)}{\overline{PRNU_{Image}} - \overline{DSNU_{Image}}} \quad (1)$$

where $\overline{PRNU_{Image}}$ (a scalar) is the mean value of a PRNU image constructed by computing the average of each pixel over 100 images at peak temporal variance, and $\overline{DSNU_{Image}}$ is the mean value of the DSNU image.

The mismatch, observed on the plots, could be explained by the variation of reference voltages, temperature and routing from the middle pixel to the periphery. However, it was observed that at minimum exposure time the gradients on the cut corners were not significant in the DSNU image (Figure 17 and 18).

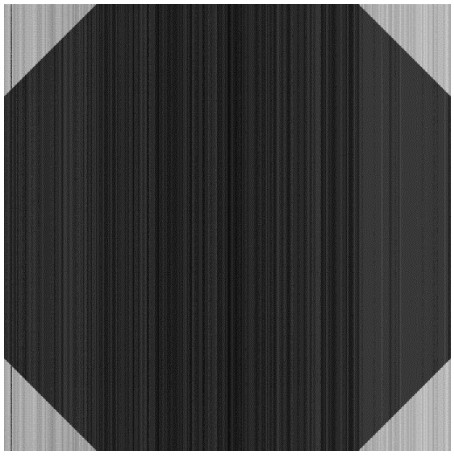

Figure 16 - Contrast enhanced DSNU image at minimum exposure time.

This could indicate that the gradient might be caused by increased dark current towards the periphery of the sensor where heat caused by the electronics increases the temperature. No other

adverse effects of the 45º tilted column and row circuitry could be observed.

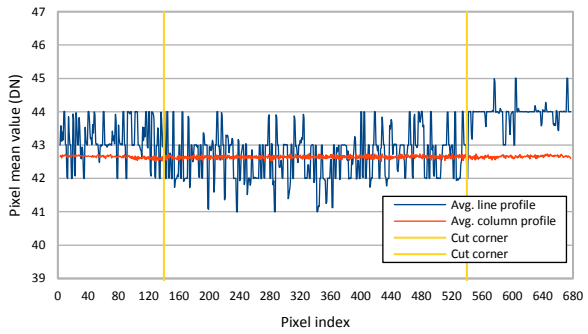

Figure 17 - Average line and column profiles over a DSNU image at minimum exposure time.

4. Conclusion

A sensor with octagonal form factor was successfully developed and manufactured in 180 nm CIS technology. The layout challenges of coincident row and column addressing and readout circuitry on the 45º cut corners were successfully managed by careful manual layout techniques. The effects on image homogeneity due to the octagonal cut remain limited to a minimal gradual shift in DSNU not noticeable to the eye even in an uncorrected image. The octagonal form factor of an image sensor allows for a larger total pixel area in a given circular inner diameter tubing, thus contributing to better total image quality in an endoscopic context. Using the reported pixel size and same minimal inner diameter, an increase in pixel number of c.a. factor 2 could be demonstrated with the given technology, pixel size and total dimensions thanks to the octagonal cut chip outline.

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Author Biography

Martin Wäny graduated in microelectronics IMT Neuchâtel, in 1997. In 1998 he worked on CMOS image sensor at IMEC. In 1999 he joined the CSEM, as PhD student in the field of digital CMOS image sensors and High dynamic range pixels. He won the Vision prize for the invention of the LINLOG Technology (2000) and the Photonics circle of excellence award of SPIE (2001). He was founder of AWAIBA Lda and co-founded Photonfocus AG. He currently works as member of the technology office in AMS and directs marketing of micro camera modules with AMS. (www.ams.com). Martin Wäny was member of the founding board of EMVA the European machine vision association and the 1288 vision standard working group. He is a member of IEEE and SPIE societies.

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